FAIRCHILD SEMICONDUCTOR®

September 1991
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74ABT245
Octal Bi-Directional Transceiver with 3-STATE Outputs

General Description

The ABT245 contains eight non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 64 mA on both the A and B ports. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A Ports to B Ports; Receive (active LOW) enables data from B Ports to A Ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition.

Features

- Bidirectional non-inverting buffers
- A and B output sink capability of 64 mA, source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch-free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Disable time is less than enable time to avoid bus contention

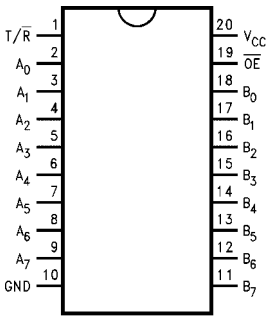
Ordering Code:

Order Number	Package Number	Package Description
74ABT245CSC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ABT245CSJ	M20D	Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ABT245CMSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74ABT245CMTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ABT245CMTCX_NL (Note 1)	MTC20	Pb-Free 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ABT245CPC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

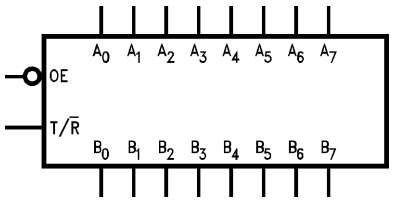
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Note 1: "_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

Connection Diagram



Logic Symbol



Pin Descriptions

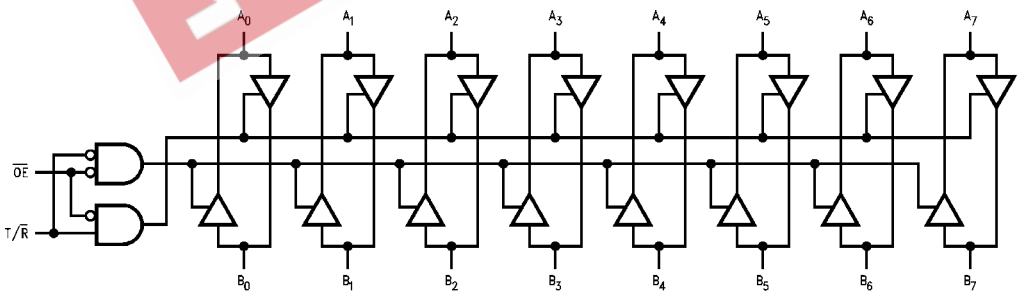
Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or 3-STATE Outputs
B_0–B_7	Side B Inputs or 3-STATE Outputs

Truth Table

Inputs		Output
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



Absolute Maximum Ratings(Note 2)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 3)	−0.5V to +7.0V
Input Current (Note 3)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or	
Power-off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	−40°C to +85°C
Supply Voltage	+4.5V to +5.5V
Minimum Input Edge Rate (ΔV/Δt)	
Data Input	50 mV/ns
Enable Input	20 mV/ns

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs

DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA ($\overline{OE}$, T/$\overline{R}$)
V_{OH}	Output HIGH Voltage		2.5			V	Min	I_{OH} = −3 mA (A_n, B_n)
			2.0			V	Min	I_{OH} = −32 mA (A_n, B_n)
V_{OL}	Output LOW Voltage				0.55	V	Min	I_{OL} = 64 mA (A_n, B_n)
I_{IH}	Input HIGH Current				1 1	μA	Max	V_{IN} = 2.7V ($\overline{OE}$, T/$\overline{R}$) V_{IN} = V_{CC} ($\overline{OE}$, T/$\overline{R}$)
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V ($\overline{OE}$, T/$\overline{R}$)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)				100	μA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input LOW Current				−1 −1	μA	Max	V_{IN} = 0.5V ($\overline{OE}$, T/$\overline{R}$) V_{IN} = 0.0V ($\overline{OE}$, T/$\overline{R}$)
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA ($\overline{OE}$, T/$\overline{R}$) All Other Pins Grounded
I_{IH} + I_{OZH}	Output Leakage Current				10	μA	0 – 5.5V	V_{OUT} = 2.7V (A_n, B_n); $\overline{OE}$ = 2.0V
I_{IL} + I_{OZL}	Output Leakage Current				−10	μA	0 – 5.5V	V_{OUT} = 0.5V (A_n, B_n); $\overline{OE}$ = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current				50	μA	Max	V_{OUT} = V_{CC} (A_n, B_n)
I_{ZZ}	Bus Drainage Test				100	μA	0.0	V_{OUT} = 5.5V (A_n, B_n); All Others GND
I_{CCH}	Power Supply Current				50	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				50	μA	Max	$\overline{OE}$ = V_{CC}, T/$\overline{R}$ = GND or V_{CC}; All Other GND or V_{CC}
I_{CCT}	Additional	Outputs Enabled			2.5	mA		V_I = V_{CC} − 2.1V
	I_{CC}/Input	Outputs 3-STATE			2.5	mA	Max	$\overline{OE}$, T/$\overline{R}$ V_I = V_{CC} − 2.1V
		Outputs 3-STATE			50	μA		Data Input V_I = V_{CC} − 2.1V All Others at V_{CC} or GND.
I_{CCD}	Dynamic I_{CC}	No Load			0.1	mA/ MHz	Max	Outputs Open $\overline{OE}$ = GND, T/$\overline{R}$ = GND or V_{CC} One Bit Toggling, 50% Duty Cycle

DC Electrical Characteristics

(SOIC package)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.7	1.0	V	5.0	T_A = 25°C (Note 4)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–1.3	–1.0		V	5.0	T_A = 25°C (Note 4)
V_{OHV}	Minimum HIGH Level Dynamic Output Voltage	2.7	3.1		V	5.0	T_A = 25°C (Note 6)
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	2.0	1.7		V	5.0	T_A = 25°C (Note 5)
V_{ILD}	Maximum LOW Level Dynamic Input Voltage		0.9	0.6	V	5.0	T_A = 25°C (Note 5)

Note 4: Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 5: Max number of data inputs (n) switching. n-1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 6: Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics

(SOIC and SSOP package)

Symbol	Parameter	T_A = +25°C, V_{CC} = +5V, C_L = 50 pF			T_A = –55°C to +125°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		T_A = –40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	1.0	2.1	3.6	1.0	4.8	1.0	3.6	ns
t_{PHL}	Data to Outputs	1.0	2.4	3.6	1.0	4.8	1.0	3.6	
t_{PZH}	Output Enable	1.5	3.2	6.0	1.0	6.7	1.5	6.0	ns
t_{PZL}	Time	1.5	3.7	6.0	2.0	7.5	1.5	6.0	
t_{PHZ}	Output Disable	1.0	3.6	6.1	1.7	7.4	1.0	6.1	ns
t_{PLZ}	Time	1.0	3.3	5.6	1.7	6.5	1.0	5.6	

Extended AC Electrical Characteristics

(SOIC package)

Symbol	Parameter	–40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF, 8 Outputs Switching (Note 7)			T_A = –40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 250 pF, 1 Output Switching (Note 8)		T_A = –40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 250 pF, 8 Outputs Switching (Note 9)		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{TOGGLE}	Max Toggle Frequency		100						MHz
t_{PLH}	Propagation Delay	1.5		5.0	1.5	6.0	2.5	8.5	ns
t_{PHL}	Data to Outputs	1.5		5.0	1.5	6.0	2.5	8.5	
t_{PZH}	Output Enable Time	1.5		6.5	2.5	7.5	2.5	9.5	ns
t_{PZL}		1.5		6.5	2.5	7.5	2.5	11.0	
t_{PHZ}	Output Disable Time	1.0		6.5	(Note 10)		(Note 10)		ns
t_{PLZ}		1.0		5.6					

Note 7: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 8: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 9: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 10: The 3-STATE delays are dominated by the RC network (500Ω, 250 pF) on the output and have been excluded from the datasheet.

Skew

(SOIC package)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 50$ pF 8 Outputs Switching (Note 13)	$T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 250$ pF 8 Outputs Switching (Note 14)	Units
		Max	Max	
t_{OSHL} (Note 11)	Pin to Pin Skew HL Transitions	1.3	2.3	ns
t_{OSLH} (Note 11)	Pin to Pin Skew LH Transitions	1.0	1.8	ns
t_{PS} (Note 15)	Duty Cycle LH–HL Skew	2.0	3.5	ns
t_{OST} (Note 11)	Pin to Pin Skew LH/HL Transitions	2.0	3.5	ns
t_{PV} (Note 12)	Device to Device Skew LH/HL Transitions	2.0	3.5	ns

Note 11: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW (t_{OSHL}), LOW-to-HIGH (t_{OSLH}), or any combination switching LOW-to-HIGH and/or HIGH-to-LOW (t_{OST}). The specification is guaranteed but not tested.

Note 12: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Note 13: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.)

Note 14: These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

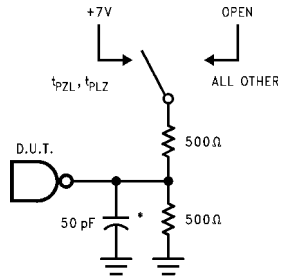
Note 15: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25°C$
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0V$ ($\overline{OE}$, $T/\overline{R}$)
$C_{I/O}$ (Note 16)	I/O Capacitance	11.0	pF	$V_{CC} = 5.0V$ (A_n, B_n)

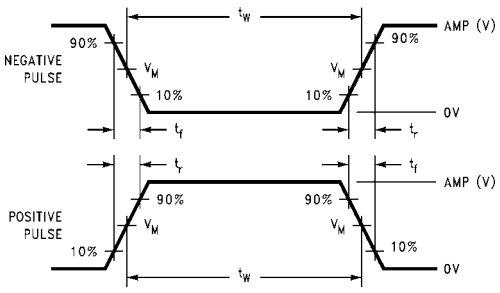
Note 16: $C_{I/O}$ is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load



V_M = 1.5V

FIGURE 2. Test Input Signal Levels

Amplitude	Rep. Rate	t_W	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

AC Waveforms

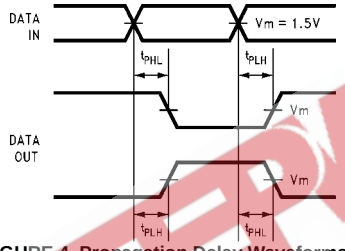


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

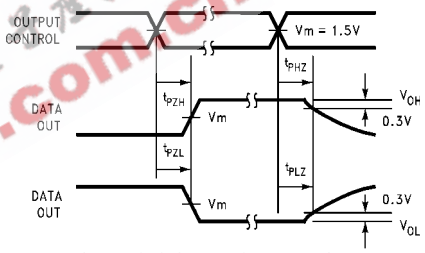


FIGURE 6. 3-STATE Output HIGH and LOW Enable and Disable Times

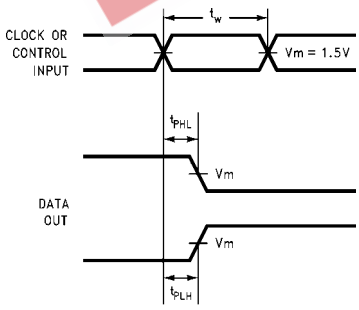


FIGURE 5. Propagation Delay, Pulse Width Waveforms

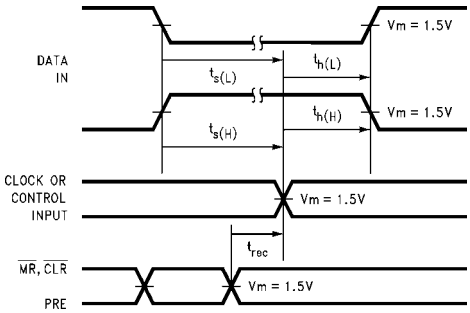
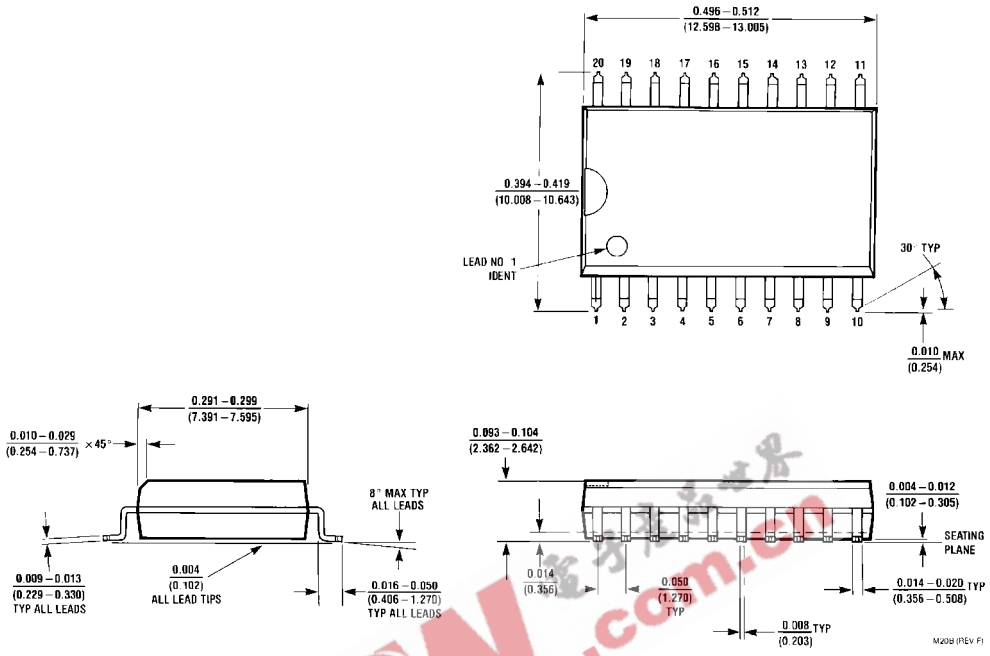


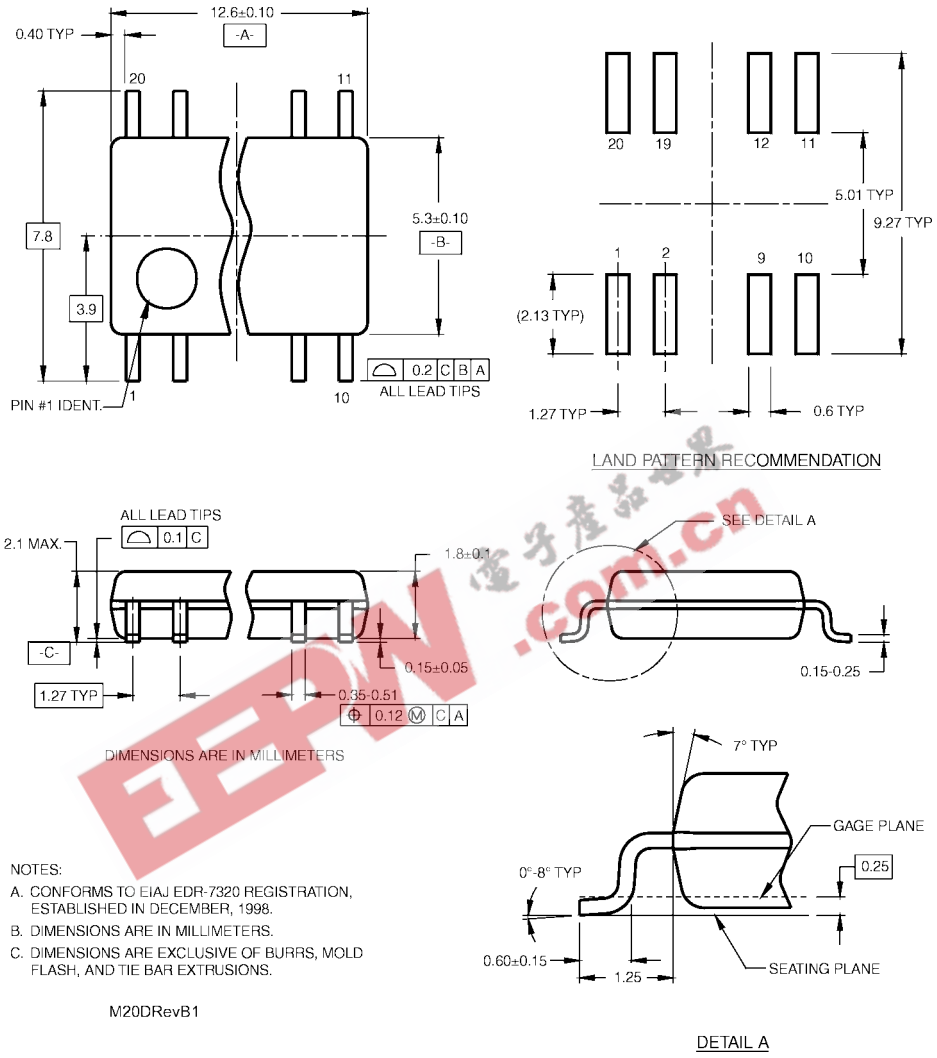
FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

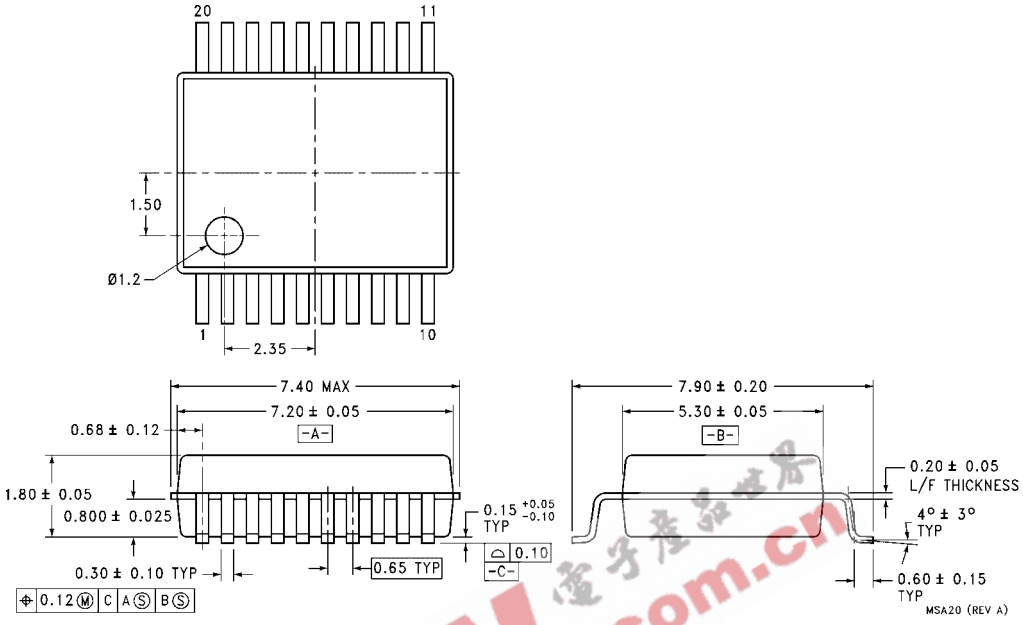
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

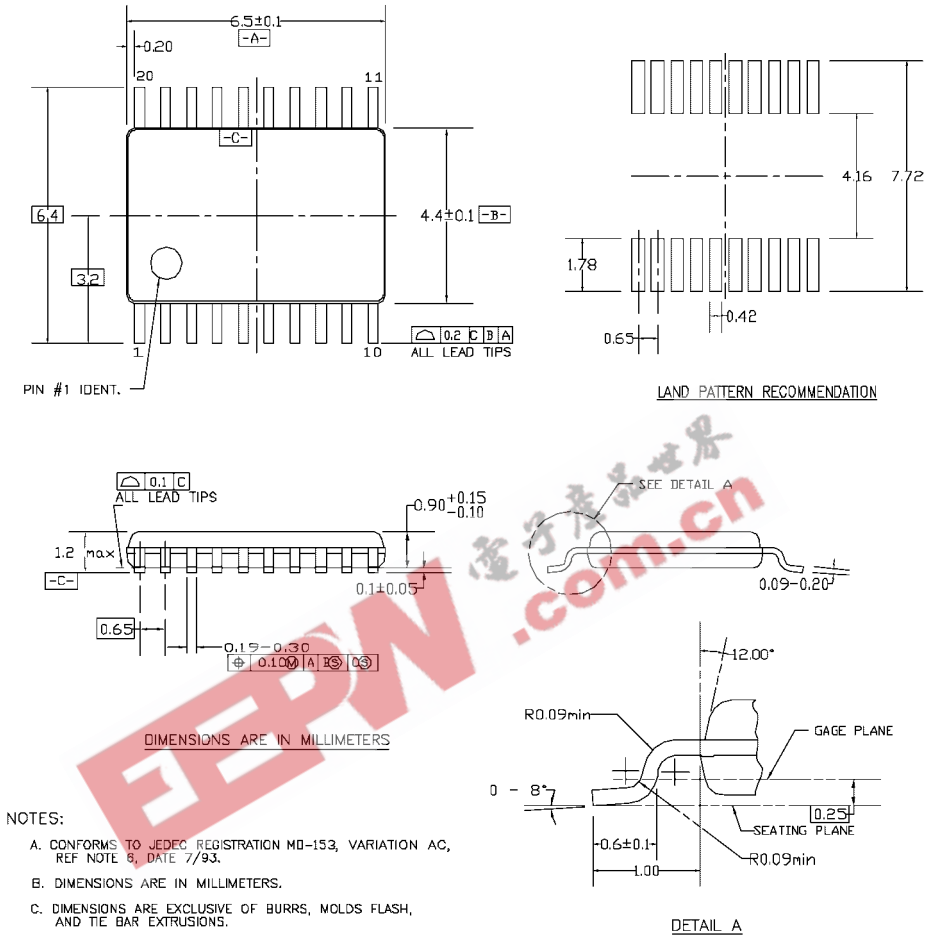
Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
Package Number MSA20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

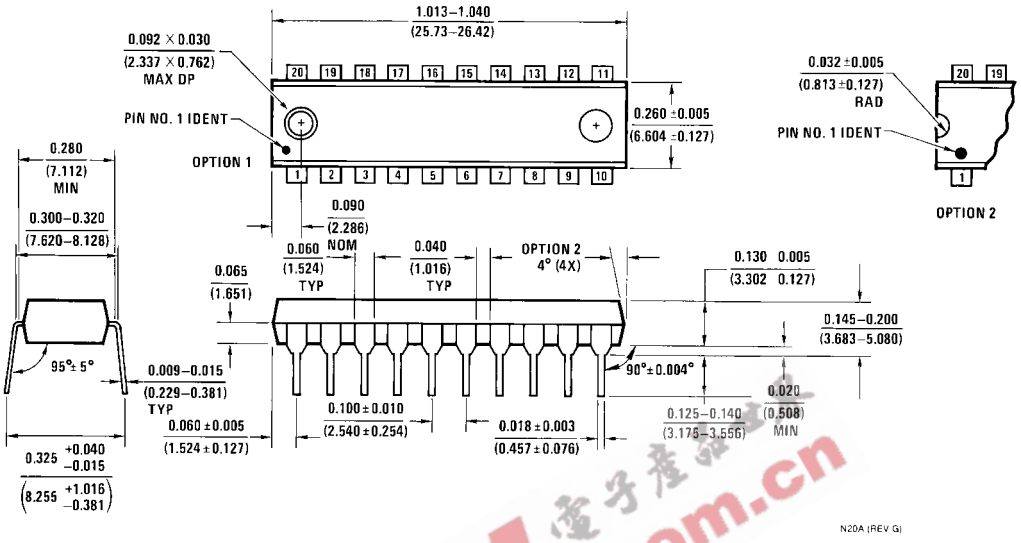
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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