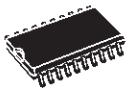
74LVQ245

LOW VOLTAGE CMOS OCTAL BUS TRANSCEIVER (3-STATE)

- HIGH SPEED: t_{PD} = 6 ns (TYP.) at V_{CC} = 3.3V
- COMPATIBLE WITH TTL OUTPUTS
- LOW POWER DISSIPATION: I_{CC} = 5 µA (MAX.) at T_A = 25 °C
- LOW NOISE: V_{OLP} = 0.5V (TYP.) at V_{CC} = 3.3V
- 75Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE: $|I_{OH}| = I_{OL}$ = 12 mA (MIN)
- PCI BUS LEVELS GUARANTEED AT 24mA
- BALANCED PROPAGATION DELAYS: $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE: V_{CC} (OPR) = 2V to 3.6V (1.2V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 245
- IMPROVED LATCH-UP IMMUNITY



M
(Micro Package)

T
(TSSOP Package)

ORDER CODES :

74LVQ245M 74LVQ245T

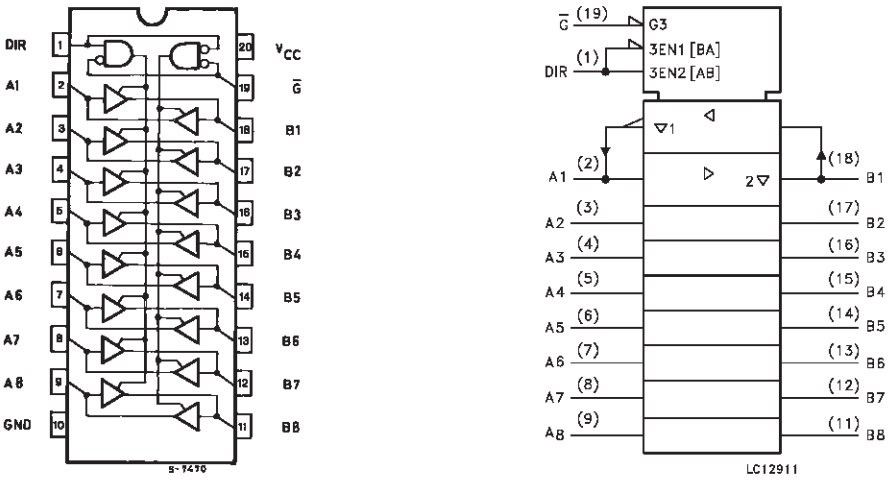
DESCRIPTION

The LVQ245 is a low voltage CMOS OCTAL BUS TRANSCEIVER (3-STATE) fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology. It is ideal for low power and low noise 3.3V applications.
It has better speed performance at 3.3V than 5V LSTTL family combined with the true CMOS low power consumption.

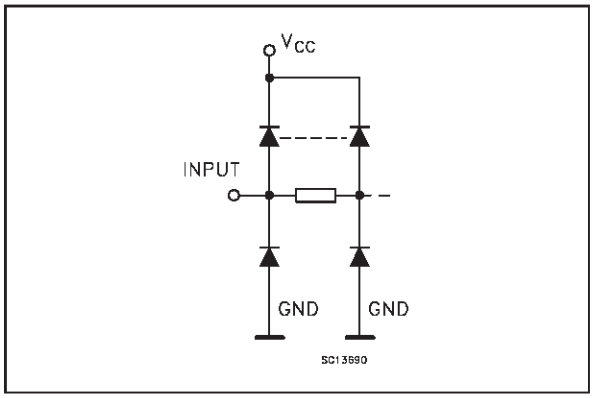
This IC is intended for two-way asynchronous communication between data buses; the direction of data trasmission is determined by DIR input. The enable input $\overline{G}$ can be used to disable the device so that the buses are effectively isolated.
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

IT IS PROHIBITED TO APPLY A SIGNAL TO A TERMINAL WHEN IT IS IN OUTPUT MODE AND WHEN A BUS TERMINAL IS FLOATING (HIGH IMPEDANCE STATE) IT IS REQUESTED TO FIX THE INPUT LEVEL BY MEANS OF EXTERNAL PULL DOWN OR PULL UP RESISTOR.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	DIR	Directional Control
2, 3, 4, 5, 6, 7, 8, 9	A1 to A8	Data Inputs/Outputs
18, 17, 16, 15, 14, 13, 12, 11	B1 to B8	Data Inputs/Outputs
19	$\overline{G}$	Output Enable Input
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

TRUTH TABLE

INPUT		FUNCTION		OUTPUT
$\overline{G}$	DIR	A BUS	B BUS	
L	L	OUTPUT	INPUT	A = B
L	H	INPUT	OUTPUT	B = A
H	X	Z	Z	Z

X: "H" or "L"
Z: High impedance

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage (DIR, $\overline{G}$)	-0.5 to V_{CC} + 0.5	V
$V_{I/O}$	DC Bus I/O Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 400	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	2 to 3.6	V
V_I	Input Voltage (DIR, $\overline{G}$)	0 to V_{CC}	V
$V_{I/O}$	Bus I/O Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature:	-40 to +85	°C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 3V) (note 2)	0 to 10	ns/V

1) Truth Table guaranteed: 1.2V to 3.6V
2) V_{IN} from 0.8V to 2V

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value					Unit
		V_{CC} (V)			T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	3.0 to 3.6	V_O = 0.1 V or V_{CC} - 0.1 V		2.0			2.0		V
V_{IL}	Low Level Input Voltage						0.8		0.8	V
V_{OH}	High Level Output Voltage	3.0	V_I(*) = V_{IH} or V_{IL}	I_O=-50 µA	2.9	2.99		2.9		V
				I_O=-12 mA	2.58			2.48		
				I_O=-24 mA				2.2		
V_{OL}	Low Level Output Voltage	3.0	V_I(*) = V_{IH} or V_{IL}	I_O=50 µA		0.002	0.1		0.1	V
				I_O=12 mA		0	0.36		0.44	
				I_O=24 mA					0.55	
I_I	Input Leakage Current	3.6	V_I = V_{CC} or GND				±0.1		±1	µA
I_{OZ}	3 State Output Leakage Current	3.6	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.3		±3	µA
I_{CC}	Quiescent Supply Current	3.6	V_I = V_{CC} or GND				4		40	µA
I_{OLD}	Dynamic Output Current (note 1, 2)	3.6	V_{OLD} = 0.8 V max					36		mA
I_{OHD}			V_{OHD} = 2 V min					-25		mA

1) Maximum test duration 2ms, one output loaded at time
2) Incident wave switching is guaranteed on transmission lines with impedances as low as 75 Ω.
(*) All outputs loaded.

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Conditions		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
V_{OLP}	Dynamic Low Voltage Quiet Output (note 1, 2)	3.3	C_L = 50 pF		0.5	0.8			V
V_{OLV}				-0.8	-0.5				
V_{IHD}	Dynamic High Voltage Input (note 1, 3)	3.3				2			
V_{ILD}	Dynamic Low Voltage Input (note 1, 3)	3.3		0.8					

1) Worst case package
2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V, (n -1) outputs switching and one output at GND
3) max number of data inputs (n) switching. (n-1) switching 0V to 3.3V. Inputs under test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). f=1MHz

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, R_L = 500 Ω, Input t_r = t_f =3 ns)

Symbol	Parameter	Test Condition		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time	2.7			7.5	14.0		15.0	ns
		3.3(*)			6.0	10.0		10.5	
t_{PZL} t_{PZH}	Output Enable Time	2.7			9.5	18.0		19.0	ns
		3.3(*)			7.5	13.0		13.5	
t_{PLZ} t_{PHZ}	Output Disable Time	2.7			10	20.0		21.0	ns
		3.3(*)			7.5	14.5		15.0	
t_{OSLH} t_{OSHL}	Output to Output Skew Time (note 1, 2)	2.7			0.5	1.0		1.5	ns
		3.3(*)			0.5	1.0		1.5	

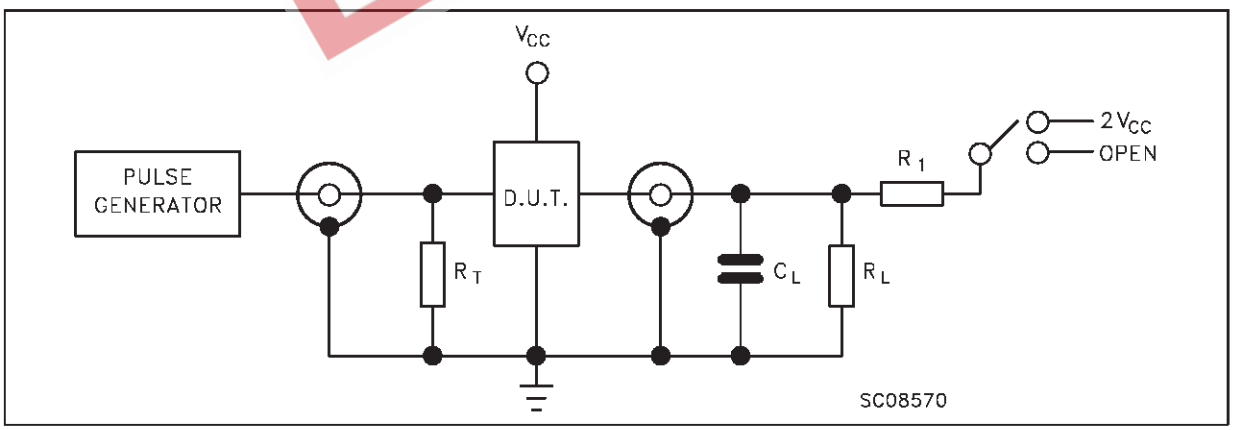
1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$)
2) Parameter guaranteed by design
(*) Voltage range is 3.3V ± 0.3V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
C_{IN}	Input Capacitance	3.3			5				pF
$C_{i/o}$	Input/Output Capacitance	3.3			10				pF
C_{PD}	Power Dissipation Capacitance (note 1)	3.3			16				pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}/8$ (per circuit)

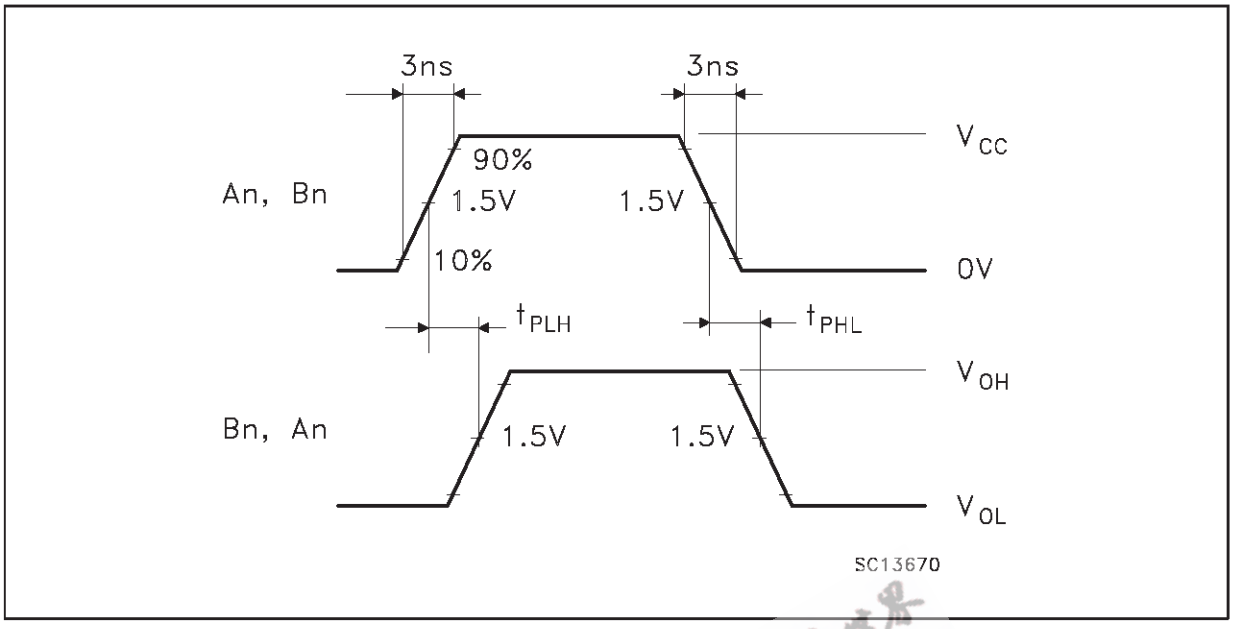
TEST CIRCUIT



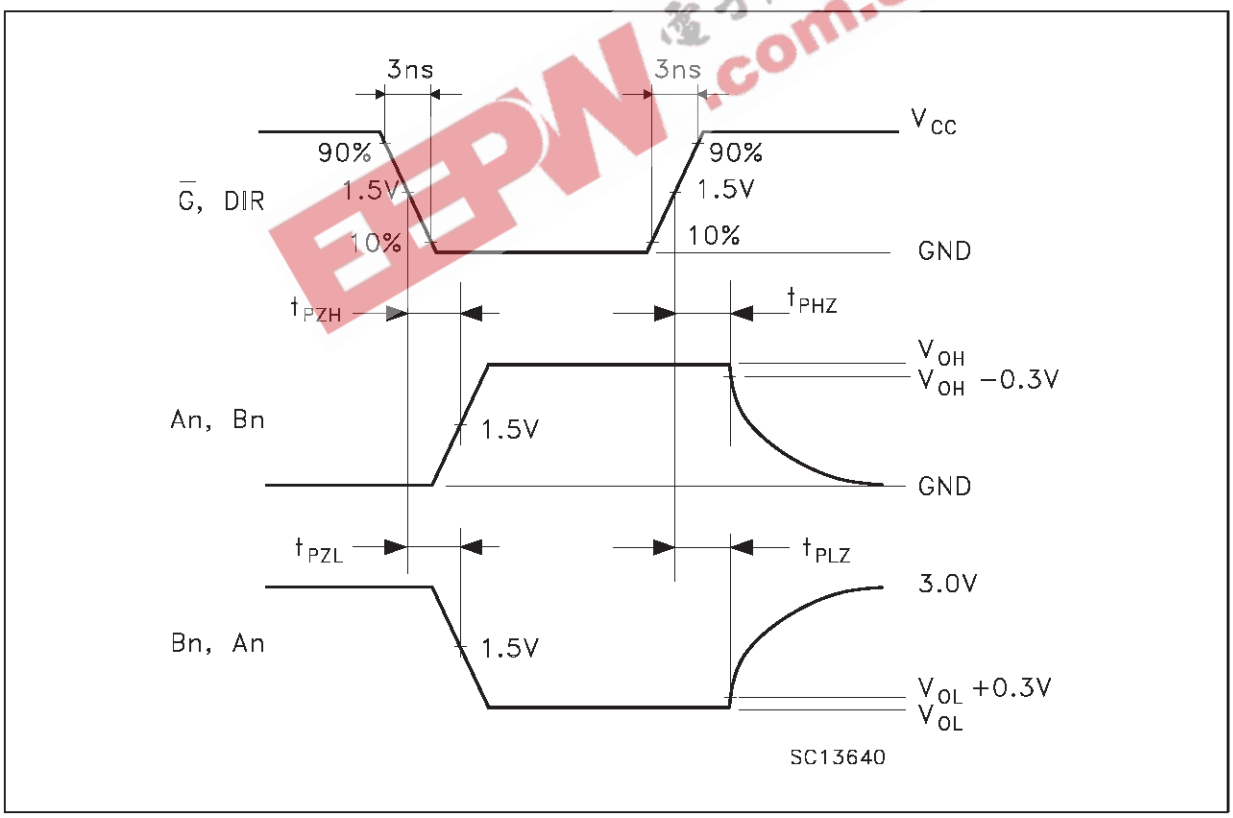
TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	$2V_{CC}$
t_{PZH}, t_{PHZ}	Open

C_L = 50 pF or equivalent (includes jig and probe capacitance)
R_L = R_1 = 500Ω or equivalent
R_T = Z_{OUT} of pulse generator (typically 50Ω)

WAVEFORM 1: PROPAGATION DELAYS (f=1MHz; 50% duty cycle)

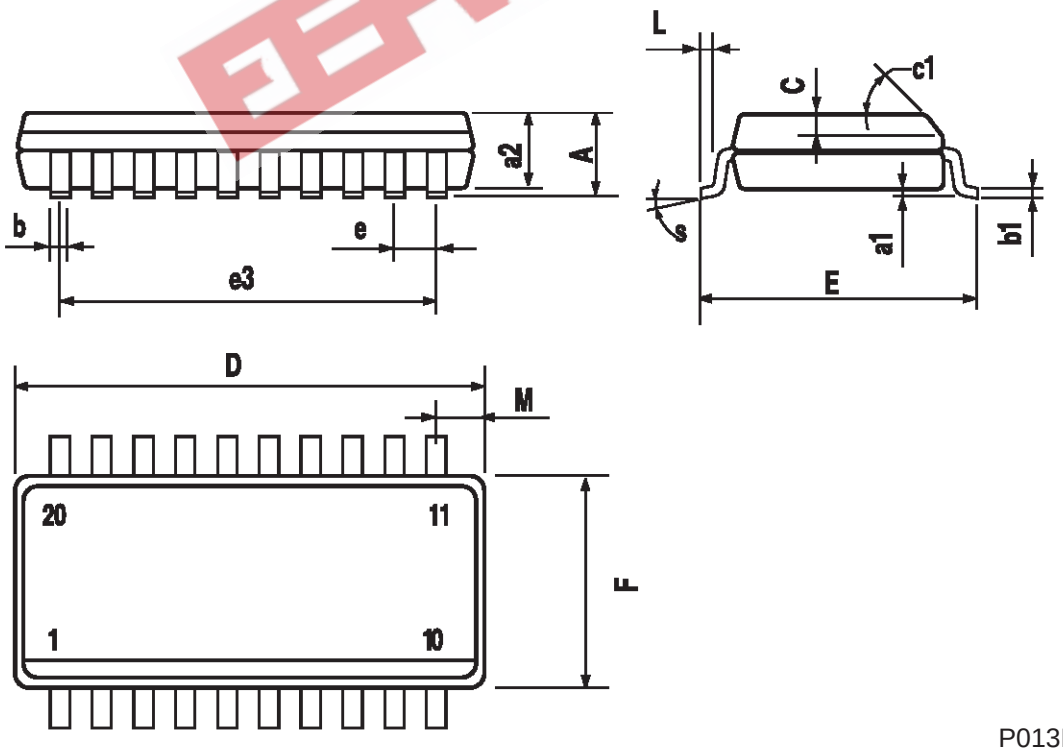


WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIME (f=1MHz; 50% duty cycle)



SO-20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45 (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
M			0.75			0.029
S	8 (max.)					



P013L

TSSOP20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.2	0.0035		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0^o	4^o	8^o	0^o	4^o	8^o
L	0.50	0.60	0.70	0.020	0.024	0.028