DATA SHEET

74F598

8-bit shift register with input storage registers (3-State)

Product specification

1991 Oct 21

IC15 Data Handbook

Philips
Semiconductors

PHILIPS

8-bit shift register with input storage registers (3-State) 74F598

FEATURES

- High impedance PNP base input for reduced loading (20µA in High and Low states)
- 8–bit parallel storage register
- Shift register has asynchronous direct overriding reset
- Shift load $\overline{SHLD}$ is functional when SHCP is Low and locked out when SHCP is High.
- Guaranteed shift frequency DC to 105MHz
- Parallel 3–State I/O storage register inputs and shift register parallel outputs

DESCRIPTION

The 74F598 consists of an 8–bit storage register feeding a parallel–in/serial–in, parallel–out/serial–out 8–bit shift register. Both the storage register and shift register have positive edge–triggered clocks. The shift register has asynchronous reset and when SHCP is Low, it has asynchronous load.

The shift register load function has been modified to load when both $\overline{SHLD}$ and SHCP are Low. When SHCP is High the shift register load operation is not performed. Data will be properly shifted on the rising edge of SHCP when $\overline{SHLD}$ is High.

TYPE	TYPICAL SHCP f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F598	100MHz	75mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	
20–pin plastic DIP	N74F598N	SOT146-1
20–pin plastic SOL	N74F598D	SOT163-1

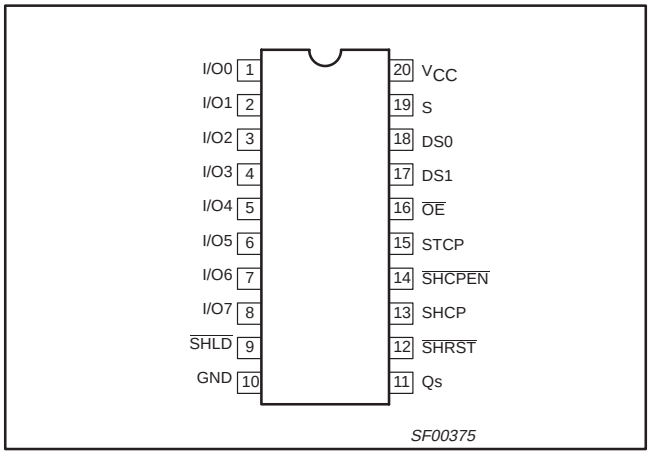
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) High/ Low	LOAD VALUE High/Low
I/On	Parallel data input	1.0/0.033	20µA/20µA
Ds0, Ds1	Serial data inputs	1.0/0.033	20µA/20µA
SHCP	Shift register clock pulse input	1.0/0.033	20µA/20µA
STCP	Storage register clock pulse input	1.0/0.033	20µA/20µA
$\overline{SHCPEN}$	Shift register clock pulse enable input	1.0/0.033	20µA/20µA
$\overline{SHLD}$	Shift register load input (active Low)	1.0/0.033	20µA/20µA
$\overline{SHRST}$	Shift register reset input (active Low)	1.0/0.033	20µA/20µA
S	Serial data select input	1.0/0.033	20µA/20µA
$\overline{OE}$	Output enable input	1.0/0.033	20µA/20µA
Qs	Serial data output	50/33	1.0mA/20mA
I/On	Parallel data outputs	150/40	3.0mA/24mA

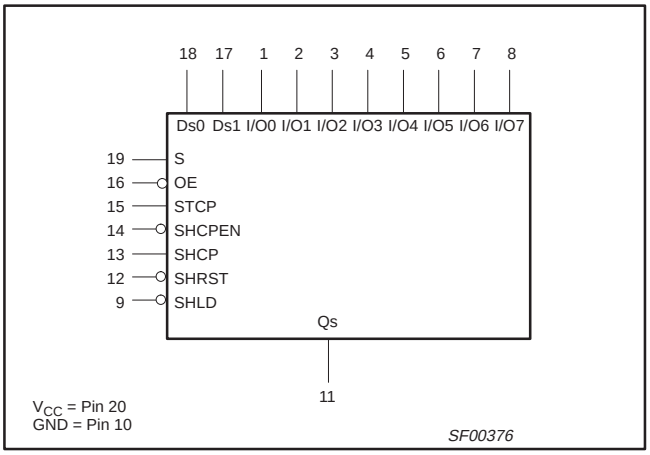
Note to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

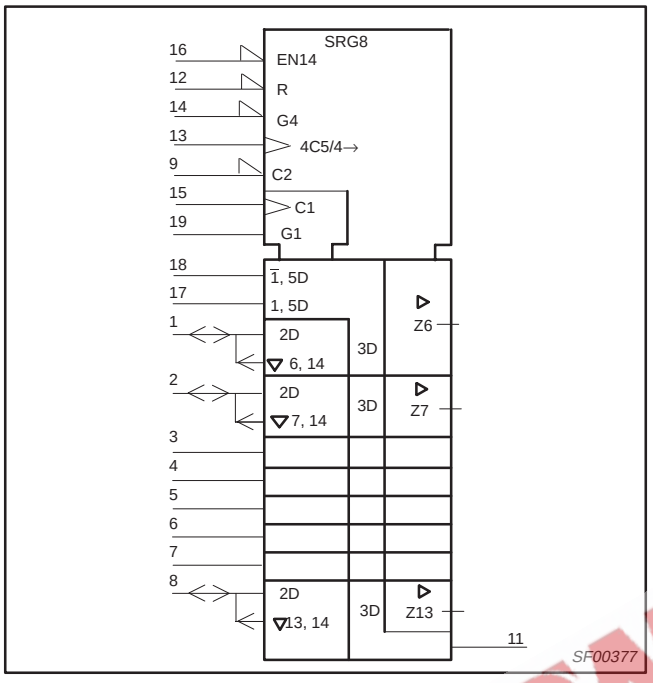
PIN CONFIGURATION



LOGIC SYMBOL



IEC/IEEE SYMBOL



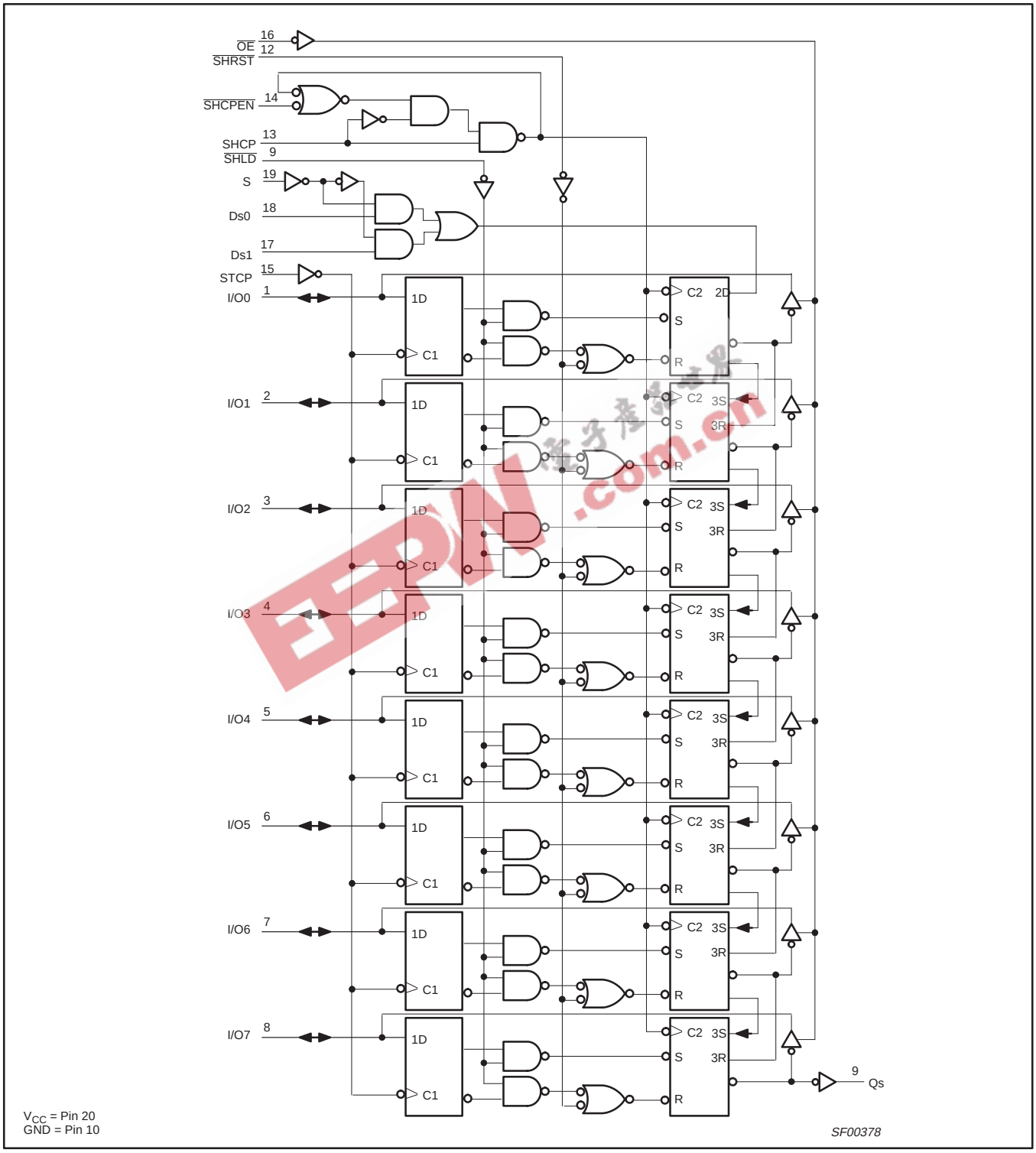
FUNCTION TABLE

INPUTS						INPUTS/OUTPUTS									OPERATING MODE
$\overline{SHRST}$	STCP	SHCP	$\overline{SHLD}$	S	$\overline{OE}$*	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7	Q7	
L	X	L	H	X	L	L	L	L	L	L	L	L	L	L	Clear shift register
L	X	L	L	X	L										Invalid, state of shift register indeterminate when signal is removed
X	↑	X	X	X	H	I0	I1	I2	I3	I4	I5	I6	I7	O7	Load data to storage register
H	X	↑	H	L	L	Ds0	O0	O1	O2	O3	O4	O5	O6	O6	Shift right
H	X	↑	H	H	L	Ds1	O0	O1	O2	O3	O4	O5	O6	O6	
H	↑	L	L	X	H	I0	I1	I2	I3	I4	I5	I6	I7	O7	Load data directly to shift register
H	↥	L	L	X	X	O0	O1	O2	O3	O4	O5	O6	O7	O7	Data transferred from storage register to shift register
X	X	X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z	NC	3–State
H	↥	X	H	X	X	NC	NC	NC	NC	NC	NC	NC	NC	NC	Hold
H	↥	H	X	X	X	NC	NC	NC	NC	NC	NC	NC	NC	NC	Hold (no storage or shift register load

Notes to function table

D0 – D7 = The level of the steady state inputs to the serial multiplexer.
H = High voltage level
I0 – I7 = The level of the steady state input at the respective I/O terminal is loaded into the flip–flop while the flip–flop outputs (except Q7) are isolated from the I/O terminal.
L = Low voltage level
NC= No change
O0 – O7 = The level of the respective Qn flip–flop prior to the last clock Low–to–High transition
X = Don't care
Z = High impedance "off" state
* = When the $\overline{OE}$ input is High, all I/O terminals are at the High impedance state, sequential operation or cleaning of the register is not affected.
↑ = Low–to–High clock transition
↥ = Not Low–to–High clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	Qs	40	mA
		I/O0 – I/O7	48	mA
T_{amb}	Operating free air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current	Qs			–1	mA
		I/O0 – I/O7			–3	mA
I_{OL}	Low–level output current	Qs			20	mA
		I/O0 – I/O7			24	mA
T_{amb}	Operating free air temperature range		0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	Qs	V_{CC} = MIN, V_{IL} = MAX, V_{IL} = MAX,	I_{OH} = –1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/On	V_{IH} = MIN, V_{IL} = MAX,	I_{OH} = –3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX,		±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX		±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = MAX, V_I = 7.0V					100	µA
		I/On	V_{CC} = MAX, V_I = 5.5V					1	mA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{OZH} + I_{IH}	Off–state output current, High–level voltage applied	I/On only	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{OZL} + I_{IL}	Off–state output current, Low–level voltage applied		V_{CC} = MAX, V_O = 0.5V					–70	µA
I_{OS}	Short–circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				68	100	mA
		I_{CCL}					80	110	mA
		I_{CCZ}					73	105	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

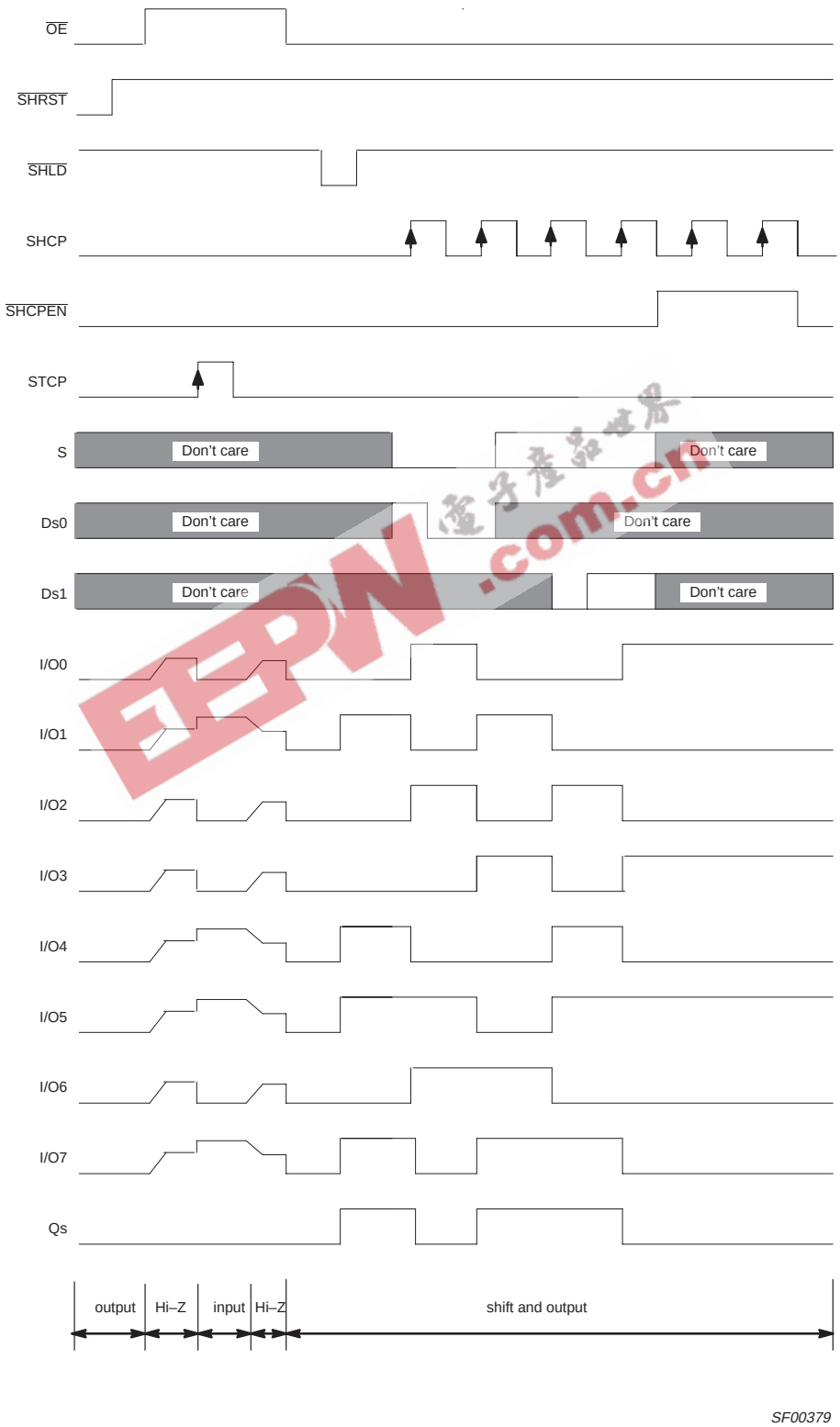
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	SHCP	Waveform 1	85	100		70		MHz
		STCP		140	160		130		
t_{PLH} t_{PHL}	Propagation delay SHCP to Qs		Waveform 1	9.5 6.5	11.5 8.5	14.0 11.5	8.5 6.0	16.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay STCP to Qs ($\overline{SHLD}$ = Low)		Waveform 1	10.0 7.0	11.5 8.5	14.5 11.5	9.0 6.5	16.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SHLD}$ to Qs		Waveform 1	9.0 6.0	11.0 8.0	13.5 10.5	8.0 5.5	15.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay SHCP to I/On		Waveform 1	8.5 5.0	10.5 7.0	13.5 9.5	7.0 4.5	15.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SHLD}$ to I/On		Waveform 1	7.5 6.0	9.5 8.0	12.5 11.0	6.5 6.0	14.5 11.5	ns
t_{PHL}	Propagation delay, $\overline{SHRST}$ to I/On		Waveform 2	6.5	9.0	12.0	6.0	12.5	ns
t_{PHL}	Propagation delay, $\overline{SHRST}$ to Qs		Waveform 2	6.0	7.5	10.5	5.0	11.0	ns
t_{PZH} t_{PZL}	Output enable time to High or Low		Waveform 5 Waveform 6	3.5 3.0	5.5 5.0	8.5 7.5	3.0 2.5	9.5 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time to High or Low		Waveform 5 Waveform 6	1.5 4.0	3.5 6.0	6.5 9.0	1.5 4.0	7.5 9.5	ns

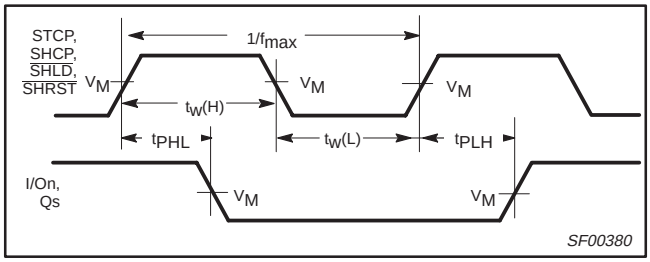
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L= 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_s (H) t_s (L)	Setup time, High or Low Dsn to SHCP	Waveform 3	0.0 3.5			1.5 4.5		ns
t_h (H) t_h (L)	Hold time, High or Low DSn to SHCP	Waveform 3	0.0 2.5			0.0 3.0		ns
t_s (H) t_s (L)	Setup time, High or Low I/On to STCP	Waveform 3	2.5 2.5			2.5 3.0		ns
t_h (H) t_h (L)	Hold time, High or Low I/On to STCP	Waveform 3	0.0 0.0			1.5 2.0		ns
t_s (H) t_s (L)	Setup time, High or Low S to SHCP	Waveform 3	3.5 3.0			4.0 3.5		ns
t_h (H) t_h (L)	Hold time, High or Low S to SHCP	Waveform 3	2.5 3.0			3.0 3.0		ns
t_s (H)	Setup time, High, STCP to $\overline{SHLD}$	Waveform 4	7.0			8.0		ns
t_h (L)	Hold time, Low, STCP to $\overline{SHLD}$ (hold mode)	Waveform 4	0.0			0.0		ns
t_s (H) t_s (L)	Setup time, High or Low, $\overline{SHCPEN}$ to SHCP	Waveform 3	0.0 2.0			0.0 2.0		ns
t_h (H) t_h (L)	Hold time, High or Low, $\overline{SHCPEN}$ to SHCP	Waveform 3	0.0 4.5			0.0 5.5		ns
t_s (H)	Setup time, High, $\overline{SHLD}$ to SHCP↑	Waveform 3	7.5			8.5		ns
t_w (H) t_w (L)	SHCP Pulse width, High or Low	Waveform 1	5.5 4.0			6.5 4.0		ns
t_w (H) t_w (L)	STCP Pulse width, High or Low	Waveform 1	4.5 4.0			5.5 4.0		ns
t_w (L)	$\overline{SHRST}$ Pulse width, Low	Waveform 1	4.0			4.0		ns
t_w (L)	$\overline{SHLD}$ Pulse width, Low	Waveform 1	4.0			5.0		ns
t_{rec}	Recovery time, $\overline{SHRST}$ to SHCP	Waveform 2	0.0			0.0		ns

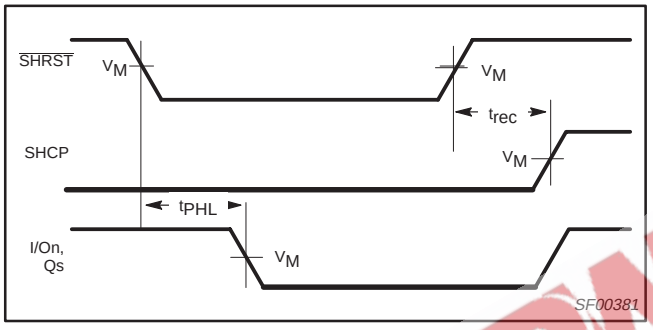
TYPICAL TIMING DIAGRAM



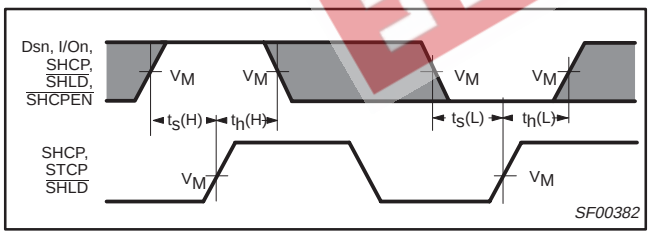
AC WAVEFORMS



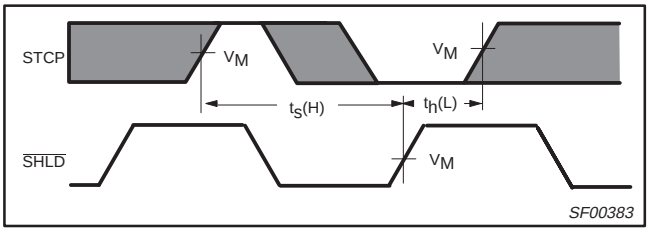
Waveform 1. Propagation delay for clock input to output, clock pulse widths, and maximum clock frequency, shift register reset and load inputs to serial data output



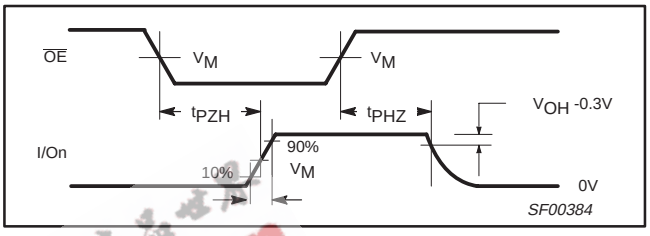
Waveform 2. Propagation delay for shift register reset to serial data output, shift register reset to shift register, shift register input recovery time



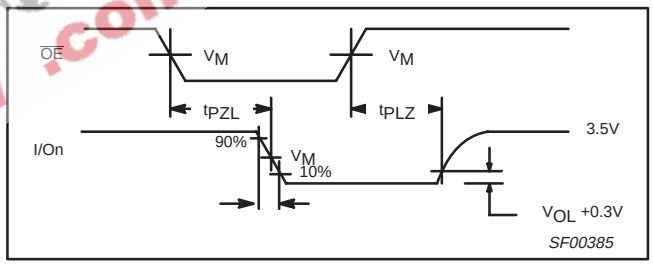
Waveform 3. Setup time and hold times



Waveform 4. Setup time and hold time



Waveform 5. 3-State output enable time to High level, output disable time from High level and transition time to High level

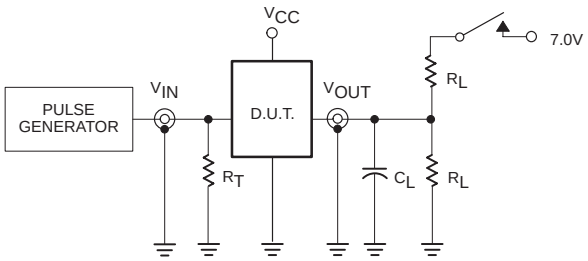


Waveform 6. 3-State output enable time to Low level, output disable time from Low level and transition time to Low level

Notes to AC waveforms

1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs

SWITCH POSITION

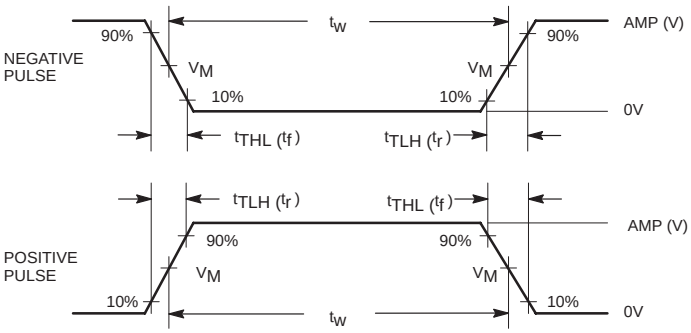
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

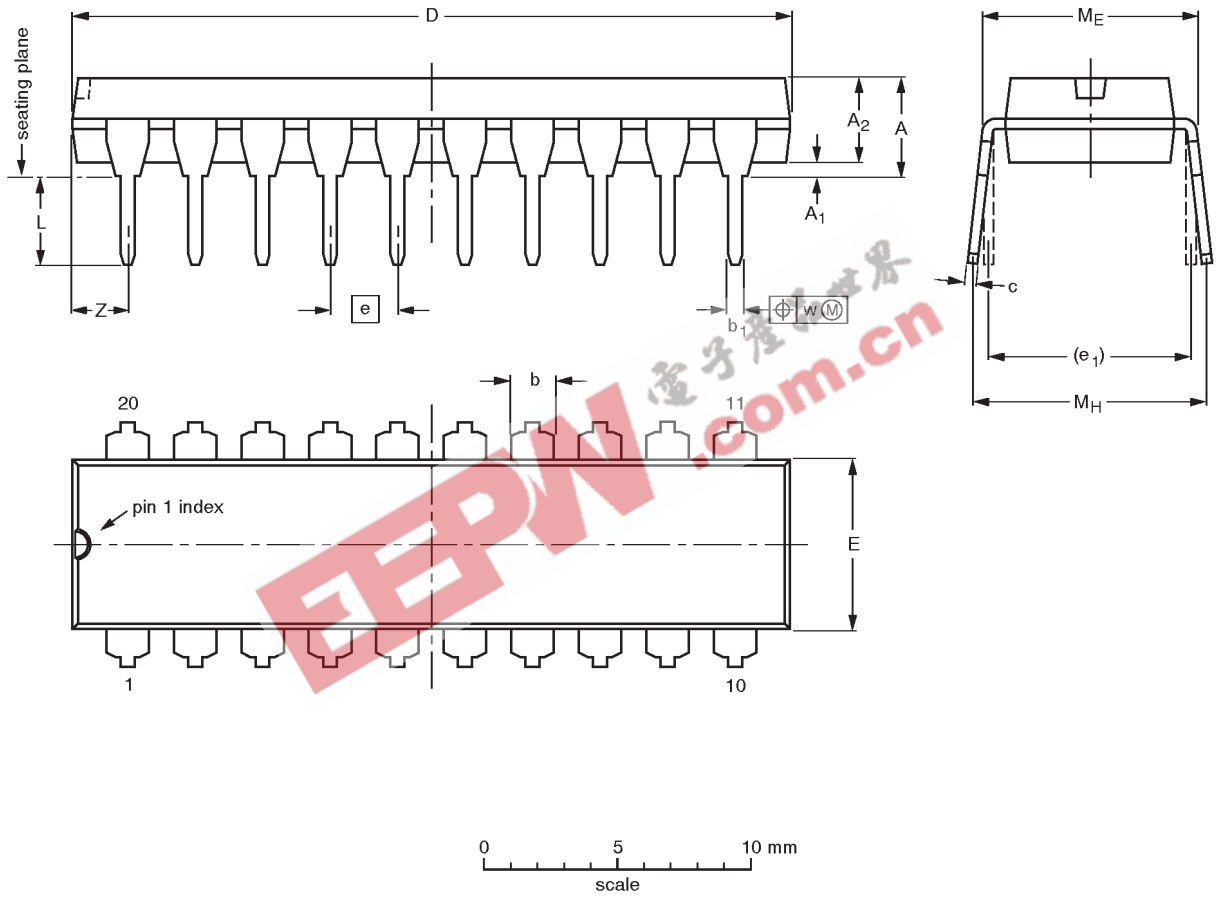


Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

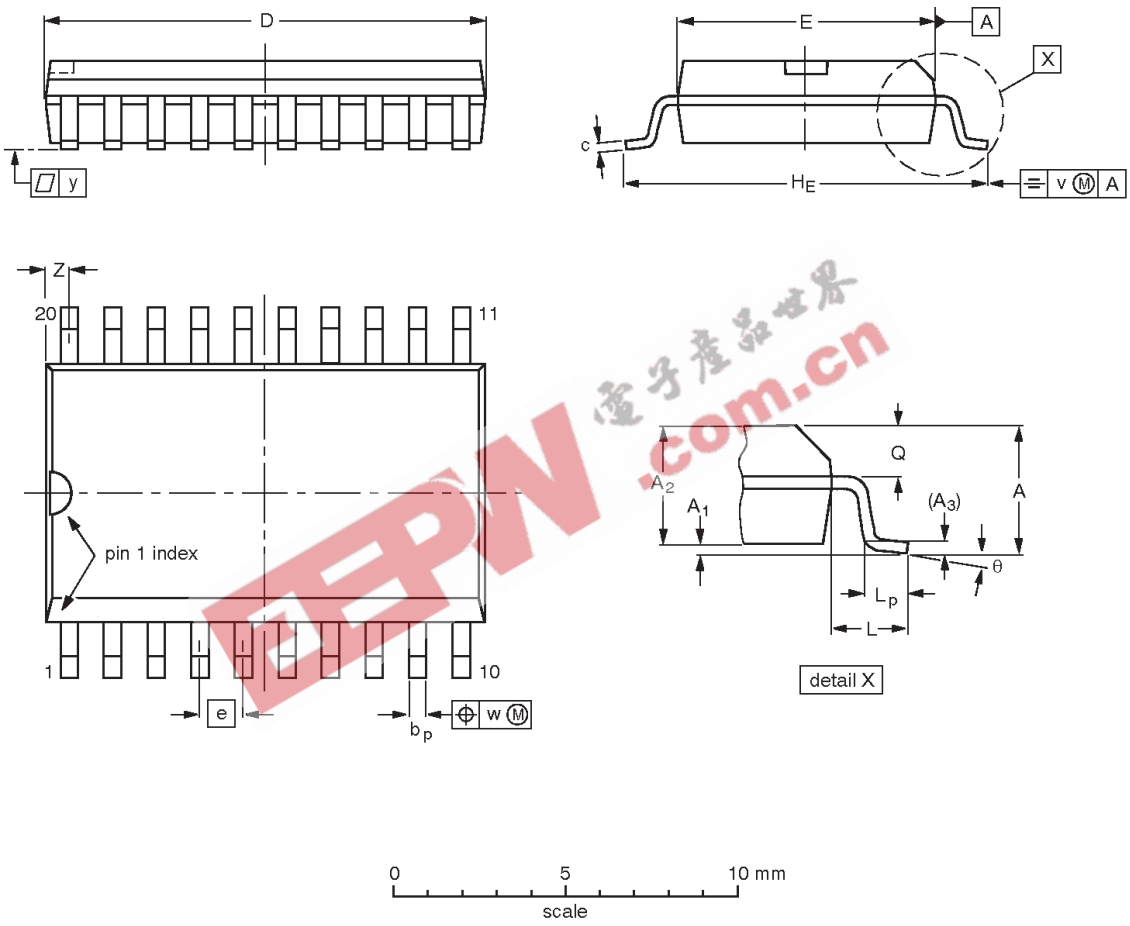
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~95-01-24~~ 97-05-22

8-bit shift register with input storage registers (3-State) 74F598

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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