FAIRCHILD SEMICONDUCTOR™

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# 74ACTQ16240
# 16-Bit Inverting Buffer/Line Driver with 3-STATE Outputs

## General Description

The ACTQ16240 contains sixteen inverting buffers with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver. The device is nibble controlled. Each nibble has separate 3-STATE control inputs which can be shorted together for full 16-bit operation.

The ACTQ16240 utilizes Fairchild's Quiet Series™ technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series™ features GTO™ output control for superior performance.

## Features

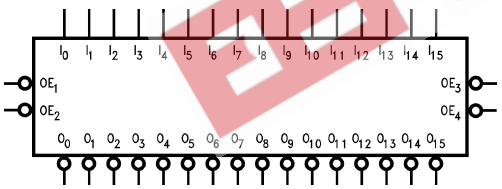
- Utilizes Fairchild's FACT Quiet Series technology
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin output skew
- Separate control logic for each byte
- 16-bit version of the ACTQ240
- Outputs source/sink 24 mA
- Additional specs for multiple output switching
- Output loading specs for both 50 pF and 250 pF loads

## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| 74ACTQ16240SSC | MS48A | 48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide |
| 74ACTQ16240MTD | MTD48 | 48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide |

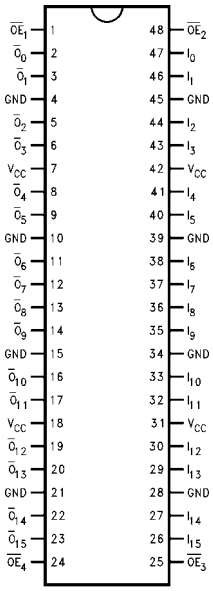
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

## Logic Symbol




## Connection Diagram

**Pin Assignment for SSOP and TSSOP**




## Pin Descriptions

| Pin Names | Description |
|---|---|
| $\overline{OE}_n$ | Output Enable Inputs (Active Low) |
| $I_0$–$I_{15}$ | Inputs |
| $\overline{O}_0$–$\overline{O}_{15}$ | Outputs |

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## Truth Tables

| Inputs | | Outputs |
|---|---|---|
| $\overline{OE}_1$ | $I_0$–$I_3$ | $\overline{O}_0$–$\overline{O}_3$ |
| L | L | H |
| L | H | L |
| H | X | Z |

| Inputs | | Outputs |
|---|---|---|
| $\overline{OE}_2$ | $I_4$–$I_7$ | $\overline{O}_4$–$\overline{O}_7$ |
| L | L | H |
| L | H | L |
| H | X | Z |

| Inputs | | Outputs |
|---|---|---|
| $\overline{OE}_3$ | $I_8$–$I_{11}$ | $\overline{O}_8$–$\overline{O}_{11}$ |
| L | L | H |
| L | H | L |
| H | X | Z |

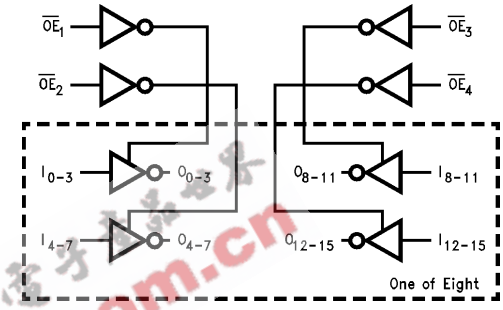
| Inputs | | Outputs |
|---|---|---|
| $\overline{OE}_4$ | $I_{12}$–$I_{15}$ | $\overline{O}_{12}$–$\overline{O}_{15}$ |
| L | L | H |
| L | H | L |
| H | X | Z |

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

## Functional Description

The ACTQ16240 contains sixteen inverting buffers with 3-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independently of the other. The control pins may be shorted together to obtain full 16-bit operation. The 3-STATE outputs are controlled by an Output Enable ($\overline{OE}_n$) input for each nibble. When $\overline{OE}_n$ is LOW, the outputs are in 2-state mode. When $\overline{OE}_n$ is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

## Logic Diagram

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## Absolute Maximum Ratings(Note 1)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5V to +7.0V |
| DC Input Diode Current ($I_{IK}$) | |
| $V_I$ = −0.5V | −20 mA |
| $V_I$ = $V_{CC}$ + 0.5V | +20 mA |
| DC Output Diode Current ($I_{OK}$) | |
| $V_O$ = −0.5V | −20 mA |
| $V_O$ = $V_{CC}$ + 0.5V | +20 mA |
| DC Output Voltage ($V_O$) | −0.5V to $V_{CC}$ + 0.5V |
| DC Output Source/Sink Current ($I_O$) | ± 50 mA |
| DC $V_{CC}$ or Ground Current per Output Pin | ± 50 mA |
| Junction Temperature | +140°C |
| Storage Temperature | −65°C to +150°C |

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | 4.5V to 5.5V |
| Input Voltage ($V_I$) | 0V to $V_{CC}$ |
| Output Voltage ($V_O$) | 0V to $V_{CC}$ |
| Operating Temperature ($T_A$) | −40°C to +85°C |
| Minimum Input Edge Rate (ΔV/Δt) | 125 mV/ns |
| $V_{IN}$ from 0.8V to 2.0V | |
| $V_{CC}$ @ 4.5V, 5.5V | |

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

## DC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ (V) | $T_A$ = +25°C Typ | $T_A$ = −40°C to +85°C Guaranteed Limits | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Minimum High Input Voltage | 4.5 | 1.5 | 2.0 | 2.0 | V | $V_{OUT}$ = 0.1V or $V_{CC}$ − 0.1V |
| | | 5.5 | 1.5 | 2.0 | 2.0 | | |
| $V_{IL}$ | Maximum Low Input Voltage | 4.5 | 1.5 | 0.8 | 0.8 | V | $V_{OUT}$ = 0.1V or $V_{CC}$ − 0.1V |
| | | 5.5 | 1.5 | 0.8 | 0.8 | | |
| $V_{OH}$ | Minimum High Output Voltage | 4.5 | 4.49 | 4.4 | 4.4 | V | $I_{OUT}$ = −50 µA |
| | | 5.5 | 5.49 | 5.4 | 5.4 | | |
| | | | | | | | $V_{IN}$ = $V_{IL}$ or $V_{IH}$ |
| | | 4.5 | | 3.86 | 3.76 | V | $I_{OH}$ = −24 mA |
| | | 5.5 | | 4.86 | 4.76 | | $I_{OH}$ = −24 mA (Note 2) |
| $V_{OL}$ | Maximum Low Output Voltage | 4.5 | 0.001 | 0.1 | 0.1 | V | $I_{OUT}$ = 50 µA |
| | | 5.5 | 0.001 | 0.1 | 0.1 | | |
| | | | | | | | $V_{IN}$ = $V_{IL}$ or $V_{IH}$ |
| | | 4.5 | | 0.36 | 0.44 | V | $I_{OL}$ = 24 mA |
| | | 5.5 | | 0.36 | 0.44 | | $I_{OL}$ = 24 mA (Note 2) |
| $I_{OZ}$ | Maximum 3-STATE Leakage Current | 5.5 | | ±0.5 | ±5.0 | µA | $V_I$ = $V_{IL}$, $V_{IH}$ $V_O$ = $V_{CC}$, GND |
| $I_{IN}$ | Maximum Input Leakage Current | 5.5 | | ± 0.1 | ± 1.0 | µA | $V_I$ = $V_{CC}$, GND |
| $I_{CCT}$ | Maximum $I_{CC}$/Input | 5.5 | 0.6 | | 1.5 | mA | $V_I$ = $V_{CC}$ − 2.1V |
| $I_{CC}$ | Max Quiescent Supply Current | 5.5 | | 8.0 | 80.0 | µA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{OLD}$ | Minimum Dynamic | 5.5 | | | 75 | mA | $V_{OLD}$ = 1.65V Max |
| $I_{OHD}$ | Output Current (Note 3) | | | | −75 | mA | $V_{OHD}$ = 3.85V Min |
| $V_{OLP}$ | Quiet Output Maximum Dynamic $V_{OL}$ | 5.0 | 0.5 | 0.8 | | V | Figure 1Figure 2 (Note 5)(Note 6) |
| $V_{OLV}$ | Quiet Output Minimum Dynamic $V_{OL}$ | 5.0 | −0.5 | −1.0 | | V | Figure 1Figure 2 (Note 5)(Note 6) |
| $V_{OHP}$ | Maximum Overshoot | 5.0 | $V_{OH}$ + 1.0 | $V_{OH}$ + 1.5 | | V | Figure 1Figure 2 (Note 4)(Note 6) |
| $V_{OHV}$ | Minimum $V_{CC}$ Droop | 5.0 | $V_{OH}$ − 1.0 | $V_{OH}$ − 1.8 | | V | Figure 1Figure 2 (Note 4)(Note 6) |
| $V_{IHD}$ | Minimum High Dynamic Input Voltage Level | 5.0 | 1.7 | 2.0 | | V | (Note 4)(Note 7) |
| $V_{ILD}$ | Maximum Low Dynamic Input Voltage Level | 5.0 | 1.2 | 0.8 | | V | (Note 4)(Note 7) |

**Note 2:** All outputs loaded; thresholds associated with output under test.

**Note 3:** Maximum test duration 2.0 ms; one output loaded at a time.

**Note 4:** Worst case package.

**Note 5:** Maximum number of outputs that can switch simultaneously is n. (n − 1) outputs are switched LOW and one output held LOW.

**Note 6:** Maximum number of outputs that can switch simultaneously is n. (n − 1) outputs are switched HIGH and one output held HIGH.

**Note 7:** Maximum number of data inputs (n) switching. (n − 1) input switching 0V to 3V. Input under test switching 3V to threshold ($V_{ILD}$).

## AC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ (V) (Note 8) | $T_A = +25°C$, $C_L = 50$ pF | | | $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$ | Propagation Delay | 5.0 | 2.7 | 4.8 | 7.3 | 2.7 | 7.8 | ns |
| $t_{PHL}$ | Data to Output | | 3.0 | 5.1 | 7.3 | 3.0 | 7.8 | |
| $t_{PZH}$ | Output Enable Time | 5.0 | 2.5 | 4.5 | 7.4 | 2.5 | 7.9 | ns |
| $t_{PZL}$ | | | 2.7 | 4.7 | 7.5 | 2.7 | 8.0 | |
| $t_{PHZ}$ | Output Disable Time | 5.0 | 2.3 | 5.0 | 7.9 | 2.3 | 8.2 | ns |
| $t_{PLZ}$ | | | 2.0 | 4.6 | 7.4 | 2.0 | 7.9 | |

**Note 8:** Voltage Range 5.0 is 5.0V ±0.5V.

## Extended AC Electrical Characteristics

| Symbol | Parameter | $T_A = -40°C$ to $+85°C$, $V_{CC}$ = Com, $C_L = 50$ pF, 16 Outputs Switching (Note 10) | | | $T_A = -40°C$ to $+85°C$, $V_{CC}$ = Com, $C_L = 250$ pF (Note 11) | | Units |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$ | Propagation Delay | 4.0 | | 11.2 | 5.6 | 13.8 | ns |
| $t_{PHL}$ | Data to Output | 4.0 | | 10.0 | 5.6 | 13.6 | |
| $t_{PZH}$ | Output Enable Time | 3.5 | | 10.1 | (Note 12) | | ns |
| $t_{PZL}$ | | 3.4 | | 10.0 | | | |
| $t_{PHZ}$ | Output Disable Time | 3.6 | | 8.9 | (Note 13) | | ns |
| $t_{PLZ}$ | | 3.1 | | 8.1 | | | |
| $t_{OSHL}$ (Note 9) | Pin to Pin Skew HL Data to Output | | | 1.2 | | | ns |
| $t_{OSLH}$ (Note 9) | Pin to Pin Skew LH Data to Output | | | 2.5 | | | ns |
| $t_{OST}$ (Note 9) | Pin to Pin Skew LH/HL Data to Output | | | 4.3 | | | ns |

**Note 9:** Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW ($t_{OSHL}$), LOW to HIGH ($t_{OSLH}$), or any combination switching LOW to HIGH and/or HIGH to LOW ($t_{OST}$).

**Note 10:** This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

**Note 11:** This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

**Note 12:** 3-STATE delays are load dominated and have been excluded from the datasheet.

**Note 13:** The Output Disable Time is dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

## Capacitance

| Symbol | Parameter | Typ | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Pin Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ |
| $C_{PD}$ | Power Dissipation Capacitance | 30 | pF | $V_{CC} = 5.0V$ |

## FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

Hewlett Packard Model 8180A Word Generator

PC-163A Test Fixture

Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the HFS generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. It is important to deskew the HFS generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set the HFS generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.

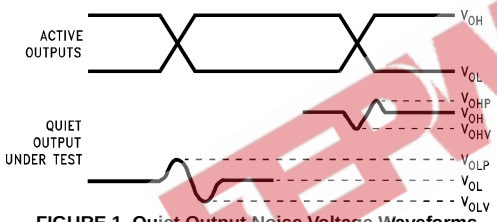



**FIGURE 1. Quiet Output Noise Voltage Waveforms**

**Note 14:** $V_{OHV}$ and $V_{OLP}$ are measured with respect to ground reference.

**Note 15:** Input pulses have the following characteristics: f = 1 MHz, $t_r$ = 3 ns, $t_f$ = 3 ns, skew < 150 ps.

5. Set the HFS generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with an oscilloscope.

$V_{OLP}/V_{OLV}$ and $V_{OHP}/V_{OHV}$:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure $V_{OLP}$ and $V_{OLV}$ on the quiet output during the worst case transition for active and enable. Measure $V_{OHP}$ and $V_{OHV}$ on the quiet output during the worst case active and enable transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

$V_{ILD}$ and $V_{IHD}$:

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, $V_{IL}$, until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds $V_{IL}$ limits, or on output HIGH levels that exceed $V_{IH}$ limits. The input LOW voltage level at which oscillation occurs is defined as $V_{ILD}$.
- Next decrease the input HIGH voltage level on the, $V_{IH}$, until the output begins to oscillate or steps out a mins of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds $V_{IL}$ limits, or on output HIGH levels that exceed $V_{IH}$ limits. The input HIGH voltage level at which oscillation occurs is defined as $V_{IHD}$.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

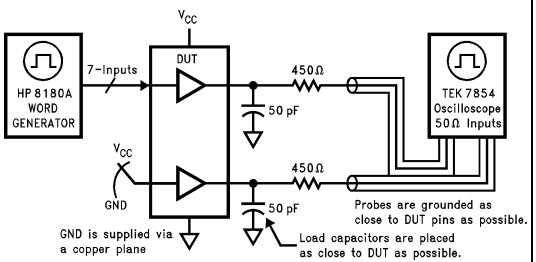
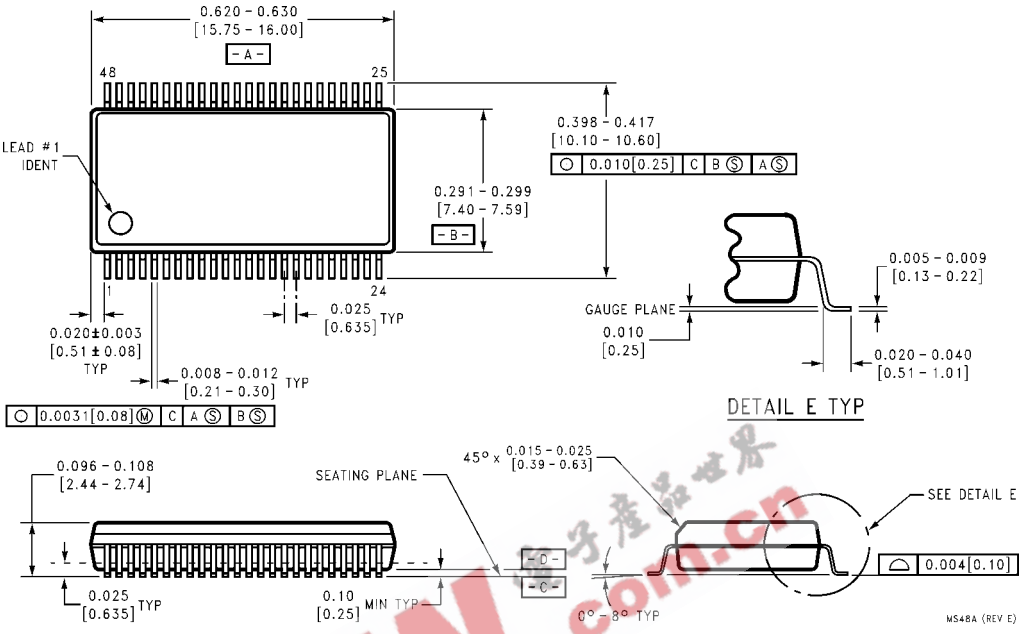



**FIGURE 2. Simultaneous Switching Test Circuit**

## Physical Dimensions inches (millimeters) unless otherwise noted




**48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide**
**Package Number MS48A**

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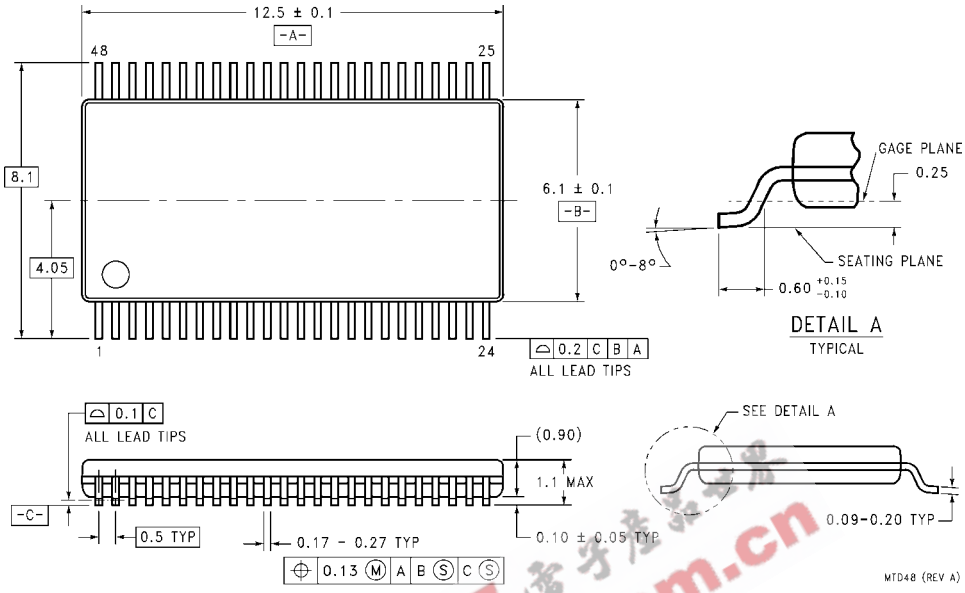
## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**48-Lead Think Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide**
**Package Number MTD48**

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