DATA SHEET

74F569

4-bit bidirectional binary synchronous counter (3-State)

Product specification

IC15 Data Handbook

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Philips
Semiconductors

PHILIPS

4-bit bidirectional binary synchronous counter (3-State) 74F569

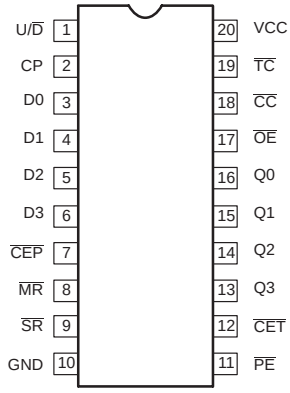
FEATURES

- 4-bit bidirectional counting – binary counter
- Synchronous counting and loading
- Look ahead carry capability for easy cascading
- Preset capability for programmable operation
- Master Reset ($\overline{MR}$) overrides all other inputs
- Synchronous Reset ($\overline{SR}$) overrides counting and parallel loading
- Clock Carry ($\overline{CC}$) output to be used as a clock for flip-flops, register and counters
- 3-State outputs for bus organized systems

DESCRIPTION

The 74F569 is a fully synchronous Up/Down binary counter. It features preset capabilities for programmable operation, carry look ahead for programmable operation, carry look ahead for easy cascading, and U/$\overline{D}$ input to control the direction of counting. For maximum flexibility there are both Synchronous and Master Reset inputs as well as both Clocked Carry ($\overline{CC}$) and Terminal Count ($\overline{TC}$) outputs. All state changes except Master Reset are initiated by rising edge of the clock. A High signal on the Output Enable ($\overline{OE}$) input forces the output buffers into the high impedance state but does not prevent counting, resetting or parallel loading.

PIN CONFIGURATION

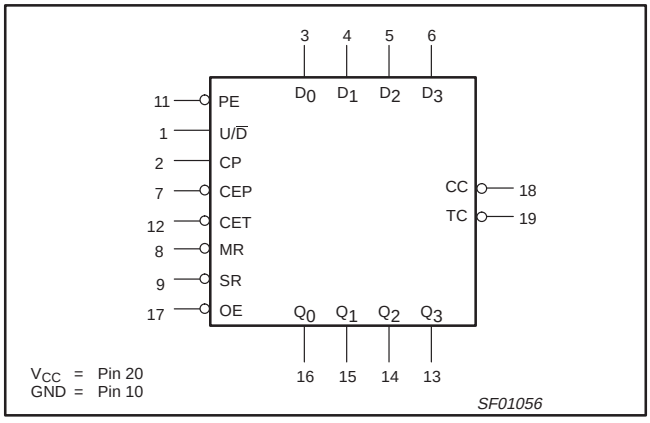


TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F569	115MHz	40mA

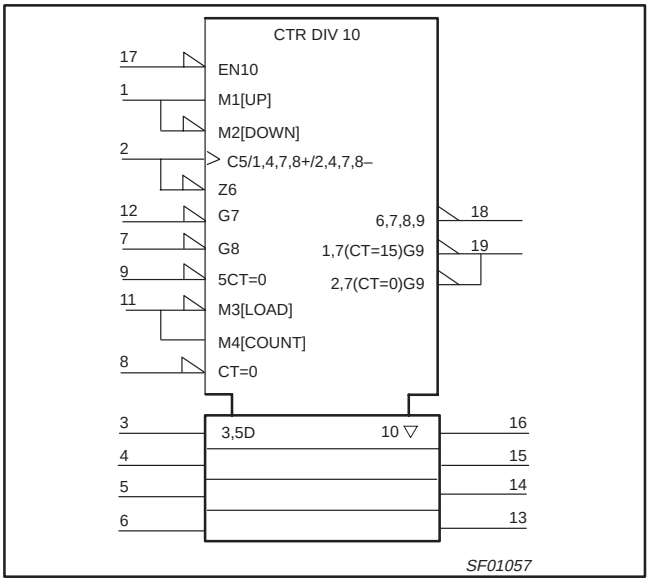
ORDERING INFORMATION

DESCRIPTION	ORDER CODE: COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG. DWG. #
20-pin plastic DIP	N74F569N	SOT146-1
20-pin plastic SO	N74F569D	SOT163-1

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 - D3	Parallel data inputs	1.0/1.0	20µA/0.6mA
$\overline{CEP}$	Count Enable parallel input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CET}$	Count Enable Trickle input (active Low)	1.0/2.0	20µA/1.2mA
CP	Clock input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{PE}$	Parallel Enable input (active Low)	1.0/2.0	20µA/1.2mA
U/$\overline{D}$	Up/Down count control input	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{SR}$	Synchronous Reset (active Low)	1.0/1.0	20µA/0.6mA
$\overline{TC}$	Terminal count output (active Low)	50/33	1.0mA/20mA
$\overline{CC}$	Clocked carry output (active Low)	50/33	1.0mA/20mA
Q0 - Q3	Data outputs	150/40	3.0mA/24mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

FUNCTIONAL DESCRIPTION

The 74F569 counts in the modulo-16 binary sequence. From state 0 (LLLL) it will increment to 15 in the up mode; in the down mode it will decrement from 15 to 0. The clock inputs of all flip-flops are driven parallel through a clock buffer. All state changes (except due to Master Reset) occur synchronously with the Low-to-High transition of the Clock Pulse ($\overline{CP}$) input.

The circuit has five fundamental modes of operation, in order of precedence: asynchronous reset, synchronous reset, parallel load, count and hold. Six control inputs–Master Reset ($\overline{MR}$), Synchronous Reset ($\overline{SR}$), Count Enable Trickle ($\overline{CET}$), Parallel Enable ($\overline{PE}$), Count Enable Parallel ($\overline{CEP}$), and the Up/Down (U/$\overline{D}$) input – determine the mode of operation, as shown in the Function Table.

A Low signal on $\overline{MR}$ overrides all other inputs and asynchronously forces the flip-flop Q outputs Low. A Low signal on $\overline{SR}$ overrides counting and parallel loading and allows the Q output to go Low on the next rising edge of CP. A Low signal on $\overline{PE}$ overrides counting and allows information on the parallel data (Dn) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{MR}$, $\overline{SR}$, and $\overline{PE}$ High, $\overline{CEP}$ and $\overline{CET}$ permit counting when both are Low. Conversely, a High signal on either $\overline{CEP}$ and $\overline{CET}$ inhibits counting.

The 74F569 uses edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, $\overline{CEP}$, $\overline{CET}$ or U/$\overline{D}$ inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed. Two types of outputs are provided as overflow/underflow indicators. The Terminal Count ($\overline{TC}$) output is normally High and goes Low provided $\overline{CET}$ is Low, when the counter reaches zero in the down mode, or reaches maximum 15 in the up mode

$\overline{TC}$ will then remain Low until a state change occurs by counting or presetting, or until U/$\overline{D}$ or $\overline{CET}$ is changed.

To implement synchronous multistage counters, the connections between the $\overline{TC}$ output and the $\overline{CEP}$ and $\overline{CET}$ inputs can provide either slow or fast carry propagation. Figure 1 shows the connections for a simple ripple carry, in which the clock period must be longer than the CP to $\overline{TC}$ delay of the first stage, plus the cumulative $\overline{CET}$ to $\overline{TC}$ delays of the intermediate stages, plus the $\overline{CET}$ to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry look ahead connections in Figure 2 are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from Max to Min in the up mode, or Min to Max in the down mode, to start its final cycle. Since this takes 16 clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock period is the CP to $\overline{TC}$ delay of the first stage plus the $\overline{CEP}$ to CP setup time of the last stage. The $\overline{TC}$ output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, register or counters.

For such applications, the Clocked Carry ($\overline{CC}$) output is provided. The $\overline{CC}$ output is normally High. When $\overline{CEP}$, $\overline{CET}$, and $\overline{TC}$ are Low, the $\overline{CC}$ output will go Low, when the clock next goes Low and will stay Low until the clock goes High again; as shown in the $\overline{CC}$ Function Table. When the Output Enable ($\overline{OE}$) is Low, the parallel data outputs Q0–Q3 are active and follow the flip-flop Q outputs. A High signal on $\overline{OE}$ forces Q0–Q3 to the High impedance state but does not prevent counting, loading or resetting.

LOGIC EQUATIONS:
Count Enable=$\overline{CEP}\times\overline{CET}\times\overline{PE}$
Up: $\overline{TC}=Q0\times Q1\times Q2\times Q3\times(Up)\times\overline{CET}$
Down: $\overline{TC}=\overline{Q}0\times\overline{Q}1\times\overline{Q}2\times\overline{Q}3\times(Down)\times\overline{CET}$

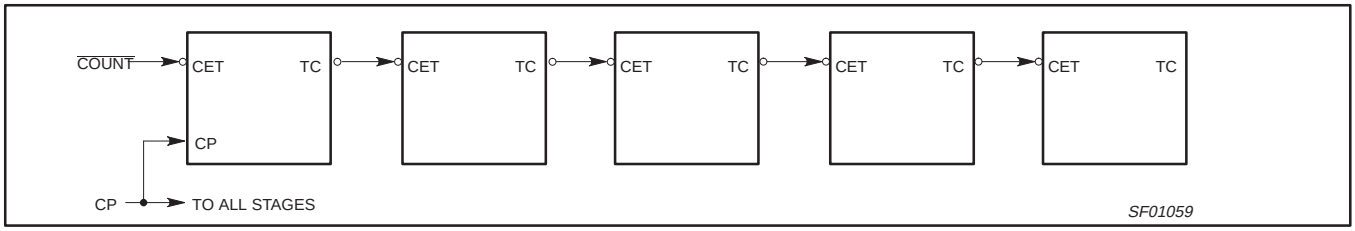


Figure 1. Multistage Counter with Ripple Carry

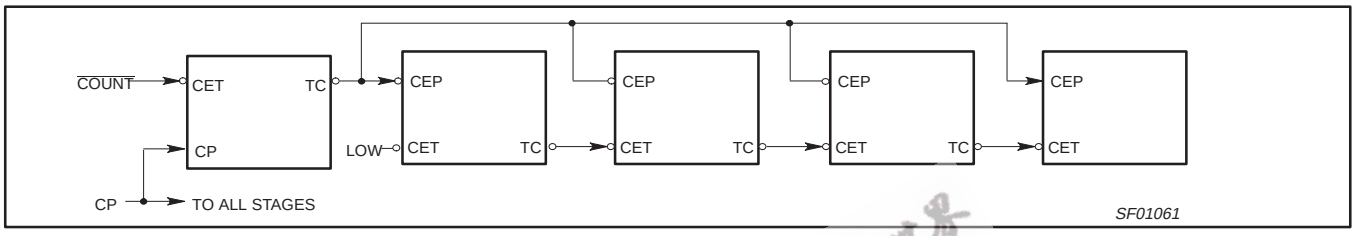
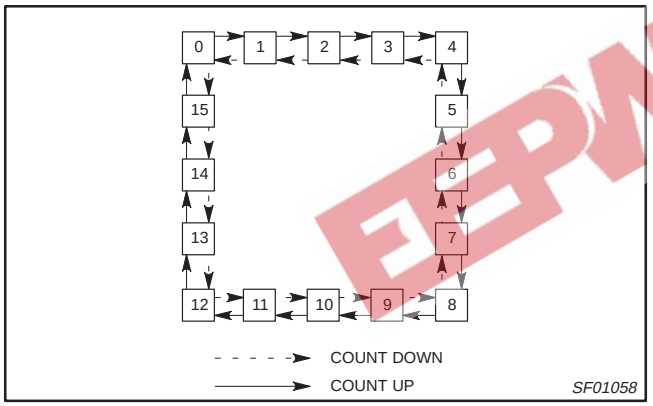


Figure 2. Multistage Counter with Look-Ahead Carry

STATE DIAGRAM



$\overline{CC}$ FUNCTION TABLE

INPUTS						OUTPUT
$\overline{SR}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	$\overline{TC}$*	CP	$\overline{CC}$
L	X	X	X	X	X	H
X	L	X	X	X	X	H
X	X	H	X	X	X	H
X	X	X	H	X	X	H
X	X	X	X	H	X	H
H	H	L	L	L	⊓	⊓

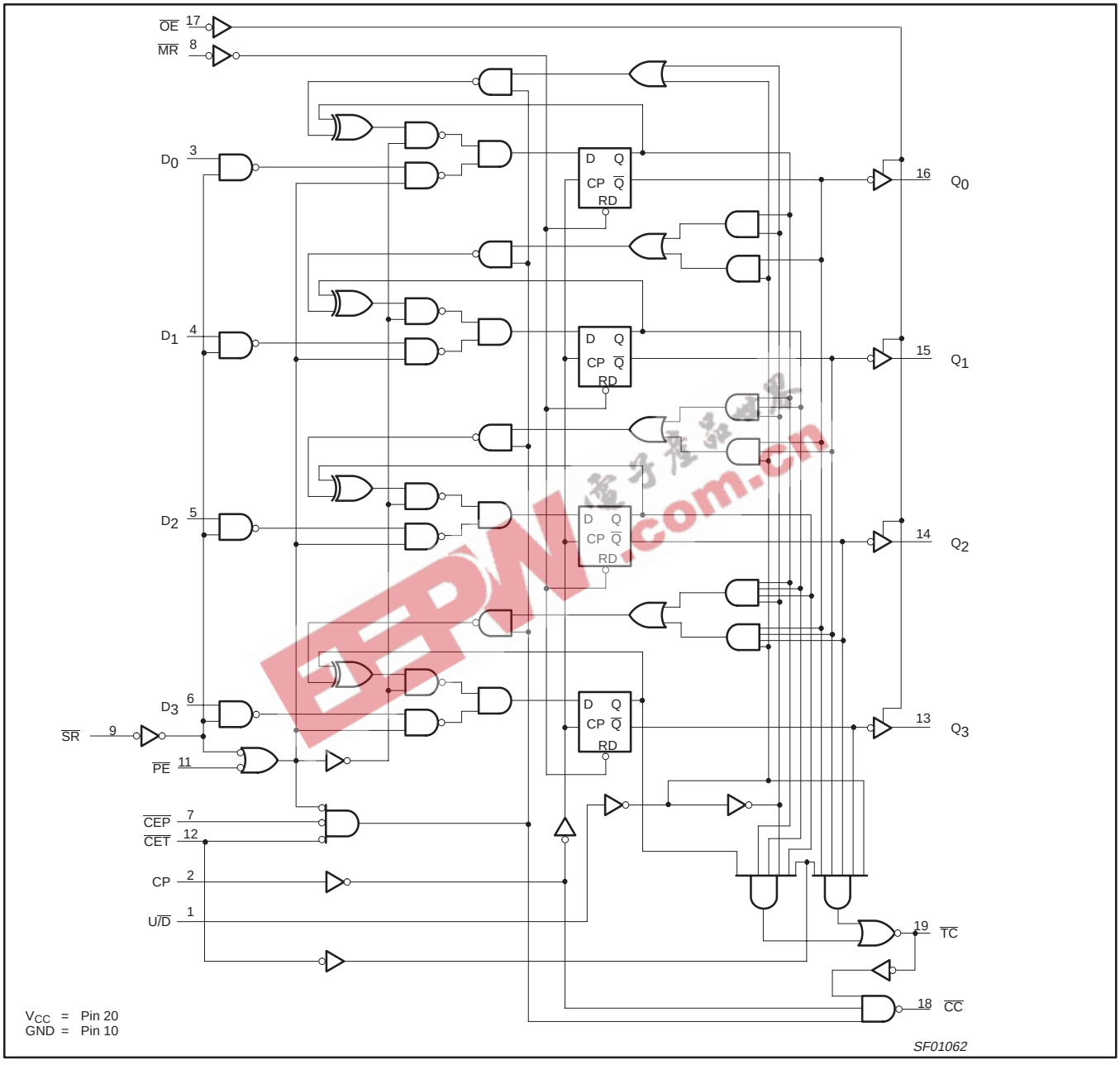
* = $\overline{TC}$ is generated internally
H = High voltage level
L = Low voltage level
X = Don't care
⊓ = Low Pulse

FUNCTION TABLE

INPUTS							OPERATING MODE
$\overline{MR}$	$\overline{SR}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	CP	
L	X	X	X	X	X	X	Asynchronous reset
h	l	X	X	X	X	↑	Synchronous reset
h	h	l	X	X	X	↑	Parallel load
h	h	h	l	l	h	↑	Count Up (increment)
h	h	h	l	l	l	↑	Count Down (decrement)
h	H	H	H	X	X	X	Hold (do nothing)
h	H	H	X	H	X	X	

H = High voltage level
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	$\overline{TC}$, $\overline{CC}$	40	mA
		Qn	48	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	$\overline{TC}$, $\overline{CC}$			–1	mA
		Qn			–3	mA
I_{OL}	Low-level output current	$\overline{TC}$, $\overline{CC}$			20	mA
		Qn			24	mA
T_{amb}	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[NO TAG]		LIMITS MIN	LIMITS TYP NO TAG	LIMITS MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	Others	V_{CC} = MAX, V_I = 0.5V				–0.6	mA
		$\overline{CET}$, $\overline{PE}$					–1.2	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 0.5V				–50	µA
I_{OS}	Short-circuit output current[NO TAG]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			38	60	mA
		I_{CCL}				43	62	mA
		I_{CCZ}				40	60	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = +5.V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.V ± 10%, C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Qn	Waveform 1	100	115		90		MHz
		$\overline{CC}$, $\overline{TC}$	Waveform 2	50	65		45		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$, High or Low)		Waveform 1	3.0 4.0	6.0 7.5	9.5 11.0	3.0 4.0	10.0 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$		Waveform 2	5.5 4.0	10.0 7.5	15.0 11.0	5.5 4.0	16.0 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$		Waveform 3	1.5 2.5	3.0 5.0	6.0 8.0	1.0 2.5	7.0 9.0	ns ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$		Waveform 4	4.0 4.0	7.5 6.5	11.0 11.0	4.0 4.0	12.0 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{CC}$		Waveform 2	2.5 2.0	4.5 4.0	7.5 6.6	2.0 2.0	6.0 7.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CEP}$, $\overline{CET}$ to $\overline{CC}$		Waveform 2	2.0 3.5	4.0 5.5	7.0 9.0	1.5 3.0	7.5 10.0	ns ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn		Waveform 5	6.0	8.0	11.0	5.5	12.0	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{CC}$		Waveform 4	4.5 5.0	9.0 11.0	12.0 16.0	4.0 5.0	13.5 17.0	ns ns
t_{PHL}	Propagation delay MR to $\overline{TC}$, $\overline{CC}$		Waveform 5	8.0	11.0	15.0	7.5	16.0	ns ns
t_{PLH} t_{PHL}	Propagation delay SR to $\overline{CC}$		Waveform 3	5.5 7.5	8.0 9.5	11.0 12.0	5.0 7.0	12.0 13.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PE}$ to $\overline{CC}$		Waveform 3	3.0 4.0	5.0 6.0	8.0 8.5	2.5 4.0	8.5 9.5	ns ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level $\overline{OE}$ to Qn		Waveform 10 Waveform 11	2.0 4.5	4.0 6.5	7.0 9.5	2.0 4.0	7.5 10.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level $\overline{OE}$ to Qn		Waveform 10 Waveform 11	1.5 1.5	3.5 3.5	6.5 6.0	1.5 1.5	7.5 6.5	ns ns

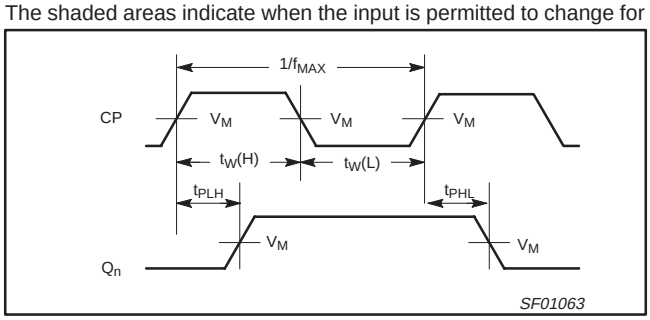
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS				UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω		T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 6	4.0 4.0		4.5 4.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 6	2.0 2.0		2.5 2.5		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 7	5.0 5.0		6.0 6.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 7	0 0		0 0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ to CP	Waveform 6	8.0 8.0		9.0 9.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP	Waveform 6	0 0		0 0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low U/$\overline{D}$ to CP	Waveform 8	10.0 8.0		12.5 8.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low U/$\overline{D}$ to CP	Waveform 8	0 0		0 0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{SR}$ to CP	Waveform 9	8.0 8.0		9.0 9.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{SR}$ to CP	Waveform 9	0 0		0 0		ns ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	7.0 5.0		8.0 6.0		ns ns
$t_w(H)$	$\overline{MR}$ Pulse width, Low	Waveform 5	4.5		5.0		ns
t_{REC}	Recovery time, $\overline{MR}$ to CP	Waveform 5	6.0		7.0		ns

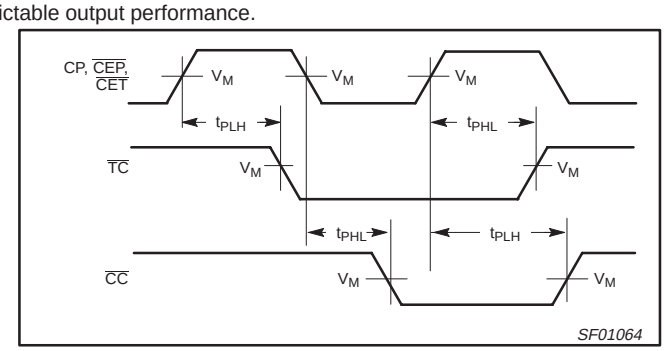
AC WAVEFORMS

For all waveforms, V_M = 1.5V

The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

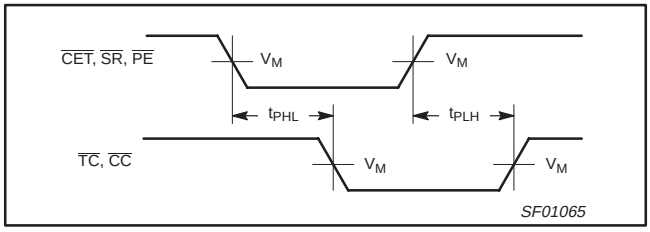


Waveform 2. Propagation Delay, CP, $\overline{CET}$, and $\overline{CEP}$ to $\overline{CC}$ and CP to $\overline{TC}$

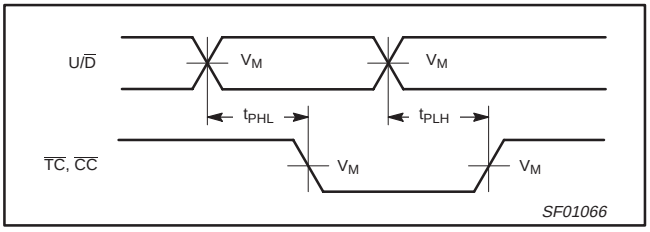
AC WAVEFORMS (Continued)

For all waveforms, V_M = 1.5V

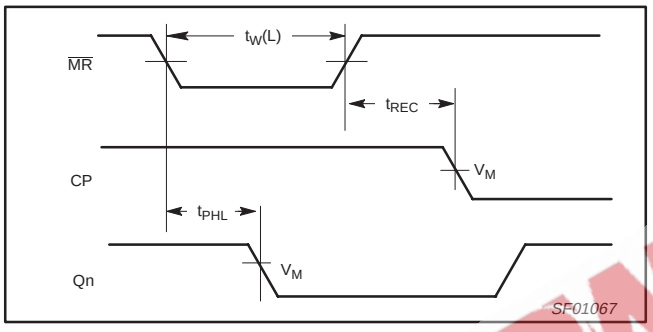
The shaded areas indicate when the input is permitted to change for predictable output performance.



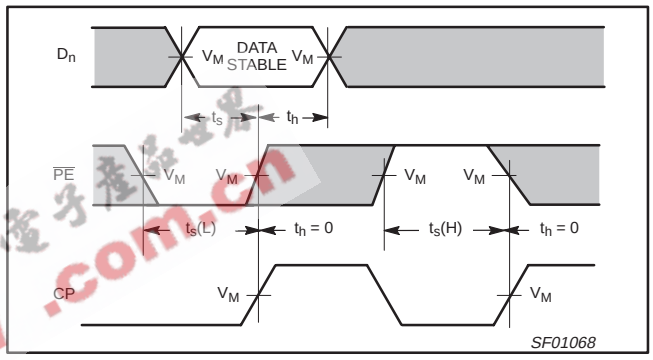
Waveform 3. Propagation Delays $\overline{CET}$ to $\overline{TC}$ and $\overline{SR}$ or $\overline{PE}$ to $\overline{CC}$



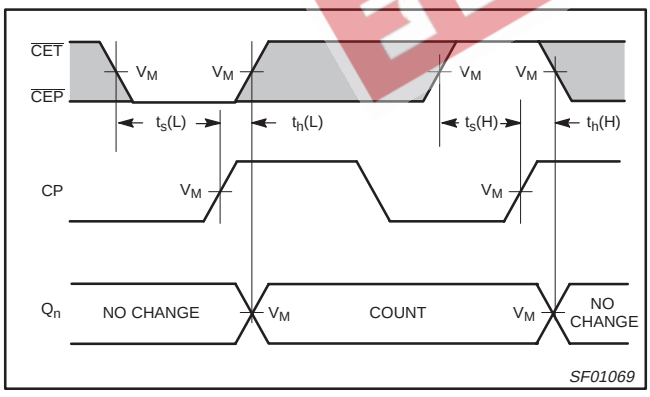
Waveform 4. Propagation Delays U/D to $\overline{TC}$ and $\overline{CC}$



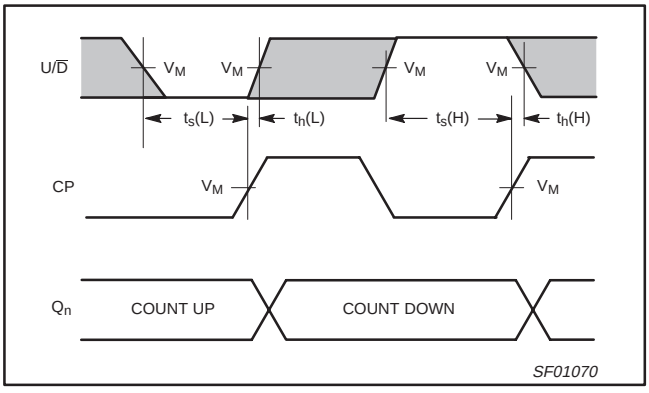
Waveform 5. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



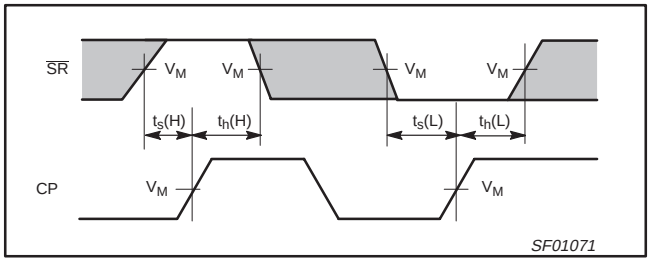
Waveform 6. Parallel Data and Parallel Enable Setup and Hold Times



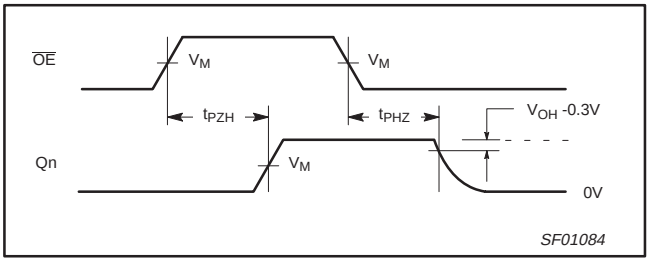
Waveform 7. Count Enable Data Setup and Hold Times



Waveform 8. Up/Down Control Setup and Hold Times



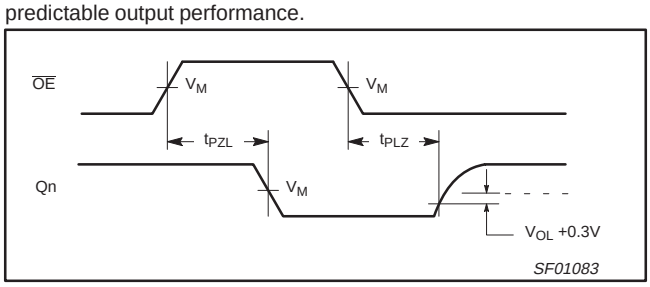
Waveform 9. Synchronous Reset Setup and Hold Times



Waveform 10. 3-State Output Enable Time to High Level and Output Disable Time from High Level

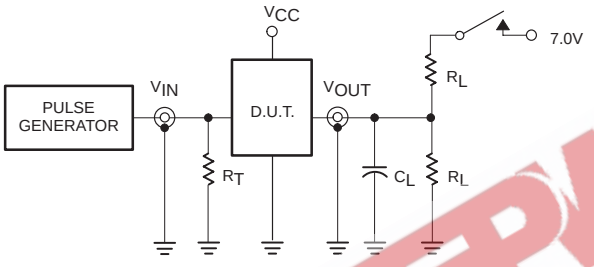
AC WAVEFORMS (Continued)

For all waveforms, V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance.

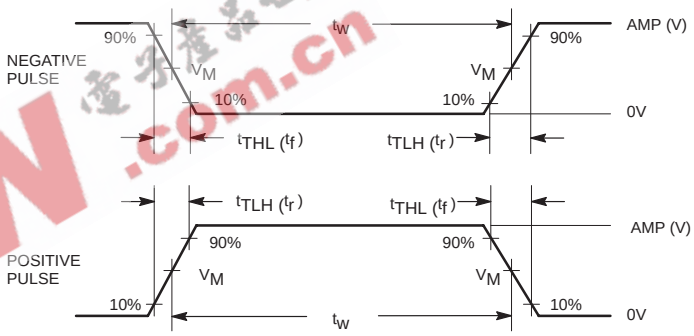


Waveform 11. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

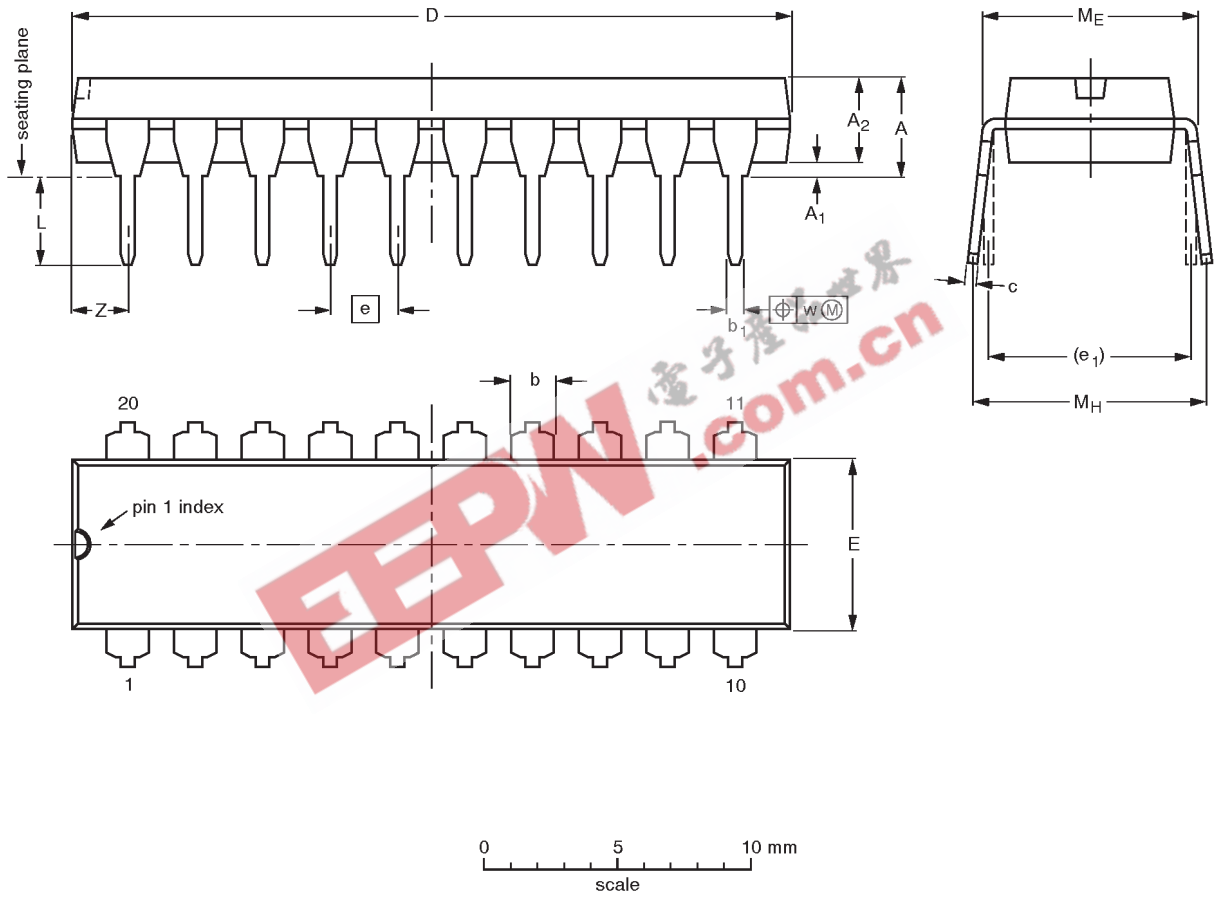
DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

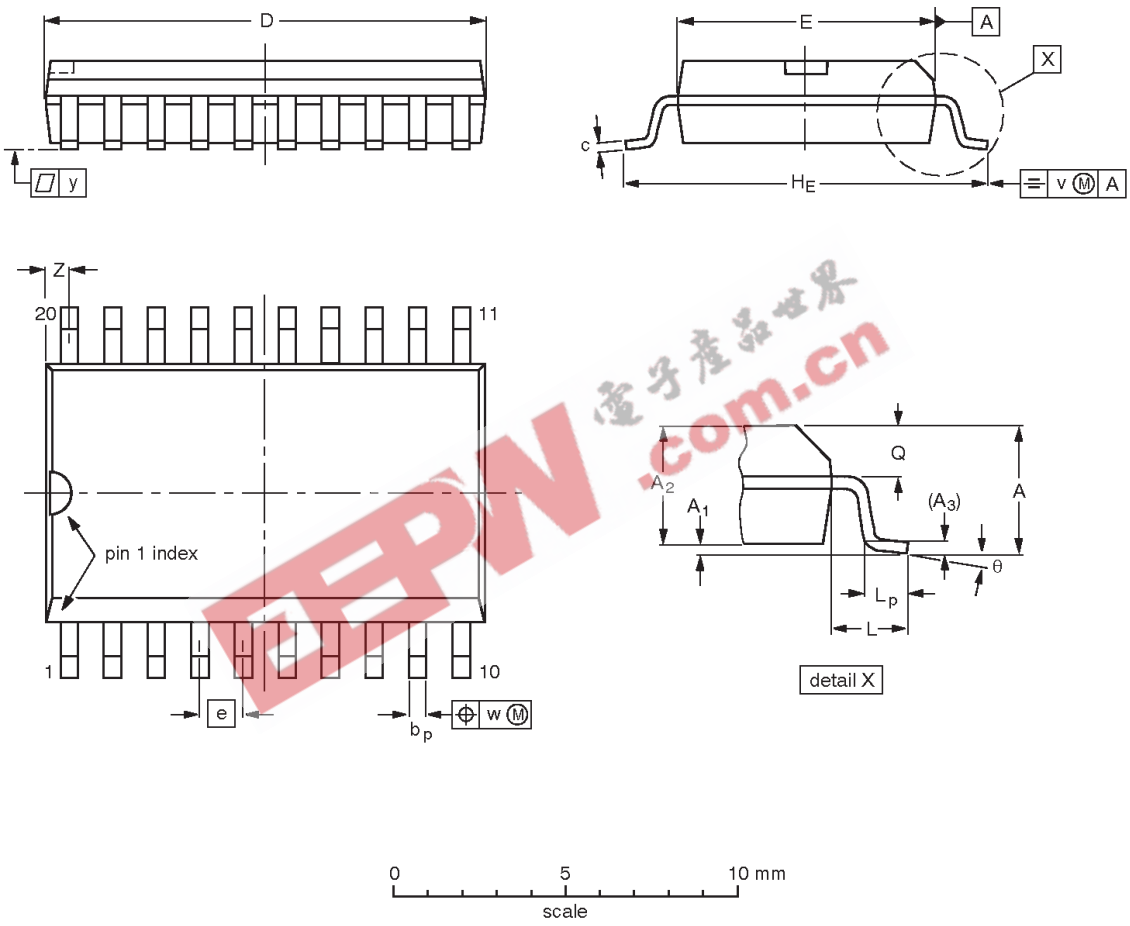
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~95-01-24~~ 97-05-22

NOTES

4-bit bidirectional binary synchronous counter (3-State) 74F569

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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