

March 1999 Revised June 2005

74LVT16240 • 74LVTH16240 Low Voltage 16-Bit Inverting Buffer/Line Driver with 3-STATE Outputs

General Description

The LVT16240 and LVTH16240 contain sixteen inverting buffers with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver. The device is nibble controlled.

Individual 3-STATE control inputs can be shorted together for 8-bit or 16-bit operation.

The LVTH16240 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs

These buffers and line drivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16240 and LVTH16240 are fabricated with an advanced BiCMOS technology to achieve high speed operation similar to $5\mathrm{V}$ ABT while maintaining a low power dissipation.

Features

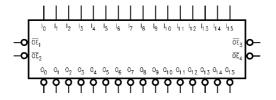
- Input and output interface capability to systems at 5V Voc
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH16240), also available without bushold feature (74LVT16240)
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- Functionally compatible with the 74 series 16240
- Latch-up performance exceeds 500 mA
- ESD performance:
- Human-body model > 2000V
- Machine model > 200V
- Charged-device model > 1000V

Ordering Code:

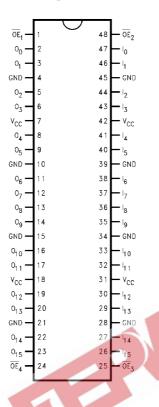
Order Number	Package Number	Package Description
74LVT16240MEA	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LVT16240MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
74LVTH16240MEA	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LVTH16240MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
OE n	Output Enable Inputs (Active LOW)
I ₀ -I ₁₅	Inputs
\overline{O}_0 – \overline{O}_{15}	3-STATE Outputs

Truth Table

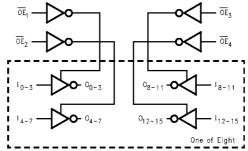
Inp	outs	Outputs
OE ₁	I ₀ –I ₃	O ₀ -O ₃
L	L	Н
L	Н	L
Н	X	Z
Inp	outs	Outputs
OE ₂	I ₄ –I ₇	$\overline{O}_4 - \overline{O}_7$
L		Н
L	- % H	L
Н 🚜 "	X	Z
dnp	outs	Outputs
OE ₃	I ₈ -I ₁₁	O ₈ -O ₁₁
		Н
O.	Н	L
Н	X	Z
Inp	outs	Outputs
OE ₄	I ₁₂ –I ₁₅	0 ₁₂ -0 ₁₅
L	L	Н
L	Н	L
Н	X	Z

- H = HIGH Voltage Leve
- L = LOW Voltage Level X = Immaterial
- Z = High Impedance

Functional Description

The LVT16240 and LVTH16240 contain sixteen inverting buffers with 3-STATE standard outputs. The device is nibble (4-bits) controlled with each nibble functioning identically, but independent of the other. The control pins may be shorted together to obtain full 16-bit operation. The 3-STATE outputs are controlled by an Output Enable (\overline{OE}_{n}) input for each nibble. When $\overline{\text{OE}}_n$ is LOW, the outputs are in 2-state mode. When $\overline{\text{OE}}_n$ is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Symbol	Parameter	Value	Conditions	Units
V _{CC}	Supply Voltage	-0.5 to +4.6		V
VI	DC Input Voltage	-0.5 to +7.0		V
Vo	DC Output Voltage	-0.5 to +7.0	Output in 3-STATE	V
		-0.5 to V _{CC} + 0.5	Output in HIGH or LOW State (Note 2)	1
I _{IK}	DC Input Diode Current	-50	V _I < GND	mA
I _{OK}	DC Output Diode Current	-50	V _O < GND	mA
Io	DC Output Current	64	V _O > V _{CC} Output at HIGH State	mA
		128	V _O > V _{CC} Output at LOW State	IIIA
I _{CC}	DC Supply Current per Supply Pin	±64		mA
I _{GND}	DC Ground Current per Ground Pin	±128		mA
T _{STG}	Storage Temperature	-65 to +150		°C

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units	
V _{CC}	Supply Voltage	-	2.7	3.6	V
VI	Input Voltage	- 44	0	5.5	V
I _{OH}	HIGH Level Output Current	4 XE 34		-32	mA
I _{OL}	LOW Level Output Current	40 0		64	mA
T _A	Free-Air Operating Temperature	4 132	-40	85	°C
Δt/ΔV	Input Edge Rate, V _{IN} = 0.8V–2.0V, V _{CC} = 3.0V	A	0	10	ns/V

Note 1: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

Note 2: I_O Absolute Maximum Rating must be observed.

DC Electrical Characteristics

				TA	=-40°C to +	85°C		
Symbol	Parame	eter	V _{CC} (V)	Min	Typ (Note 10)	Max	Units	Conditions
V _{IK}	Input Clamp Diode Vo	oltage	2.7			-1.2	V	I _I = -18 mA
V _{IH}	Input HIGH Voltage	·	2.7-3.6	2.0			V	$V_0 \le 0.1V$ or
V _{IL}	Input LOW Voltage		2.7-3.6			0.8	V	$V_O \ge V_{CC} - 0.1V$
V _{OH}	Output HIGH Voltage		2.7-3.6	V _{CC} - 0.2				I _{OH} = -100 μA
			2.7	2.4			V	I _{OH} = -8 mA
			3.0	2.0				I _{OH} = -32 mA
V _{OL}	Output LOW Voltage		2.7			0.2		I _{OL} = 100 μA
			2.7			0.5		I _{OL} = 24 mA
			3.0			0.4	V	I _{OL} = 16 mA
			3.0			0.5		I _{OL} = 32 mA
			3.0			0.55		I _{OL} = 64 mA
I _{I(HOLD)}	Bushold Input Minimu	m Drive	3.0	75			μА	$V_{I} = 0.8V$
(Note 4)				-75			μΛ	V _I = 2.0V
I _{I(OD)}	Bushold Input Over-D	rive	3.0	500			μА	(Note 5)
(Note 4)	Current to Change Sta	ate		-500			μ.Λ.	(Note 6)
I _I	Input Current		3.6			10		V _I = 5.5V
		Control Pins	3.6			±1	μА	V _I = 0V or V _{CC}
		Data Pins	3.6			- 5	μ.Λ.	$V_I = 0V$
		Data Filis	3.0			1		$V_I = V_{CC}$
I _{OFF}	Power Off Leakage C	urrent	0			±100	μА	$0V \le V_I \text{ or } V_O \le 5.5V$
I _{PU/PD}	Power Up/Down 3-ST	ATE	0-1.5V			±100	μА	V _O = 0.5V to 3.0V
	Output Current		U-1.5V			±100	μΑ	V _I = GND or V _{CC}
I _{OZL}	3-STATE Output Leak	age Current	3.6			- 5	μА	V _O = 0.5V
I _{OZH}	3-STATE Output Leak	age Current	3.6			5	μА	V _O = 3.0V

DC Electrical Characteristics (Continued)

-		.,	T _A =-40°C to +85°C					
Symbol	Parameter	V _{CC} (V)	Min	Typ (Note 10)	Max	Units	Conditions	
I _{OZH} +	3-STATE Output Leakage Current	3.6			10	μА	$V_{CC} < V_O \le 5.5V$	
I _{CCH}	Power Supply Current	3.6			0.19	mA	V _I = GND or V _{CC} , Outputs HIGH	
I _{CCL}	Power Supply Current	3.6			5	mA	V _I = GND or V _{CC} , Outputs LOW	
I _{CCZ}	Power Supply Current	3.6			0.19	mA	V _I = GND or V _{CC} , Outputs Disabled	
I _{CCZH} +	Power Supply Current	3.6			0.19	mA	$V_I = \text{GND or } V_{CC},$ $V_{CC} \le V_O \le 5.5 V,$ Outputs Disabled	
Δl _{CC}	Increase in Power Supply Current (Note 7)	3.6			0.2	mA	One Input at V _{CC} – 0.6V Other Inputs at V _{CC} or GND	

Note 3: All typical values are at $V_{CC} = 3.3V$, $T_A = 25$ °C.									
Note 4: Applies to bushold versions only (LVTH16240).									
Note 5: An external driver must source at least the specified current to switch from LOW-to-HIGH.									
Note 6: An	external driver must sink at least the specified	current to sw	tch from HIG	H-to-LOW.	7.3	- 4/1			
Note 7: This	s is the increase in supply current for each inp	ut that is at th	e specified vo	oltage level rat	ner than V _{CC}	or GND.	•		
Dynamic Switching Characteristics (Note 8)									
Dynai	mic Switching Charac	teristi	CS (Note	e 8)	140				
		teristic	CS (Note	e 8) T _A = 25°C	W.	Unite	Conditions		
Symbol	mic Switching Charac	1	CS (Note		Max	Units	$\label{eq:conditions} \begin{split} & \text{Conditions} \\ & \text{C}_{L} = \text{50 pF, R}_{L} = \text{500}\Omega \end{split}$		
		V _{CC}		T _A = 25°C	Max	Units V			

Note 8: Characterized in SSOP package. Guaranteed parameter, but not tested.

Note 9: Max number of outputs defined as (n), n-1 data inputs are driven 0V to 3V. Output at LOW.

AC Electrical Characteristics

		$T_A = -40$ °C to $+85$ °C, $C_L = 50$ pF, $R_L = 500$ Ω						
Symbol	Parameter		$V_{CC} = 3.3V \pm 0.3V$	V _{CC}	Units			
	r al allietei	Min	Тур	Max	Min	Max	Units	
			(Note 10)					
t _{PLH}	Propagation Delay Data to Output	1.0		3.5	1.0	4.2	ns	
t _{PHL}		1.0		3.5	1.0	4.0	115	
t _{PZH}	Output Enable Time	1.0		4.0	1.0	4.9		
t_{PZL}		1.2		4.8	1.2	6.1	ns	
t _{PHZ}	Output Disable Time	1.7		4.7	1.7	5.2		
t _{PLZ}		1.7		4.2	1.7	4.4	ns	
toshl	Output to Output Skew			1.0		1.0	ns	
toslh	(Note 11)							

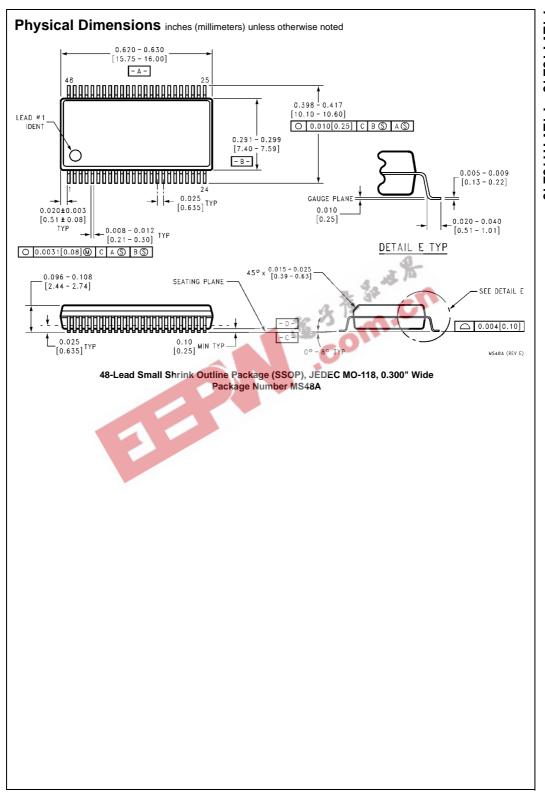
Note 10: All typical values are at $V_{CC} = 3.3V$, $T_A = 25$ °C.

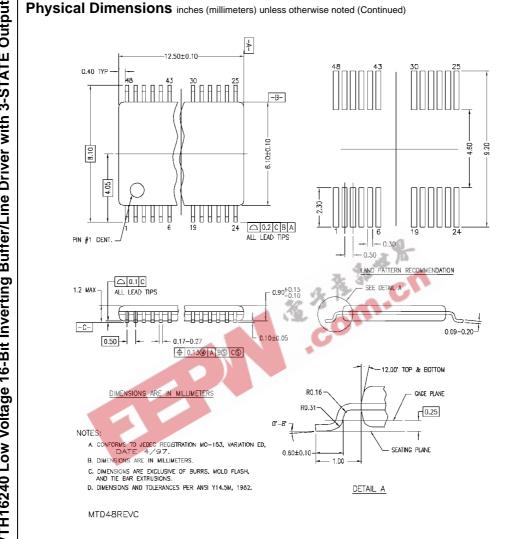
Note 11: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Capacitance (Note 12)

Symbol	Parameter	Conditions	Typical	Units
C _{IN}	Input Capacitance	$V_{CC} = 0V$, $V_I = 0V$ or V_{CC}	4	pF
C _{OUT}	Output Capacitance	$V_{CC} = 3.0V$, $V_{O} = 0V$ or V_{CC}	8	pF

Note 12: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.





48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48

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