

# DATA SHEET

EEPW 电子产品世界  
.com.cn

**74LVC11**

Triple 3-input AND gate

Product specification

1998 Apr 28

## Triple 3-input AND gate

74LVC11

## FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Output capability: standard
- $I_{CC}$  category: SSI

## DESCRIPTION

The 74LVC11 is a high-performance, low power, low-voltage Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC11 provides the 3-input AND function.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25^{\circ}\text{C}$ ;  $t_r = t_f \leq 2.5 \text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	Propagation delay nA, nB, nC to nY	$C_L = 50 \text{ pF}$ ; $V_{CC} = 3.3 \text{ V}$	3.7	ns
$C_I$	Input capacitance		5.0	pF
$C_{PD}$	Power dissipation capacitance per gate	Notes 1 and 2	26	pF

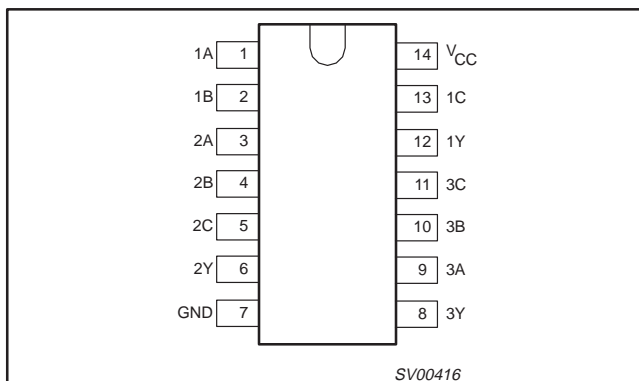
## NOTES:

- $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ )  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacity in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.
- The condition is  $V_I = \text{GND to } V_{CC}$ .

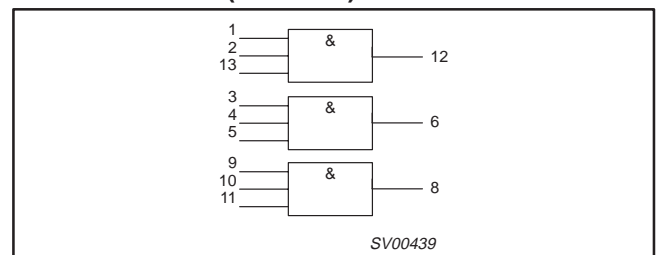
## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	$-40^{\circ}\text{C to } +85^{\circ}\text{C}$	74LVC11 D	74LVC11 D	SOT108-1
14-Pin Plastic SSOP Type II	$-40^{\circ}\text{C to } +85^{\circ}\text{C}$	74LVC11 DB	74LVC11 DB	SOT337-1
14-Pin Plastic TSSOP Type I	$-40^{\circ}\text{C to } +85^{\circ}\text{C}$	74LVC11 PW	74LVC11PW DH	SOT402-1

## PIN CONFIGURATION



## LOGIC SYMBOL (IEEE/IEC)



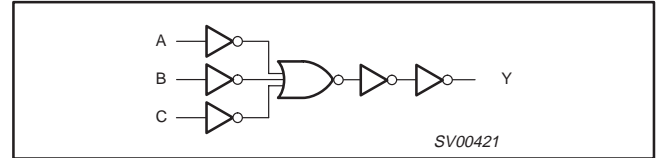
# Triple 3-input AND gate

74LVC11

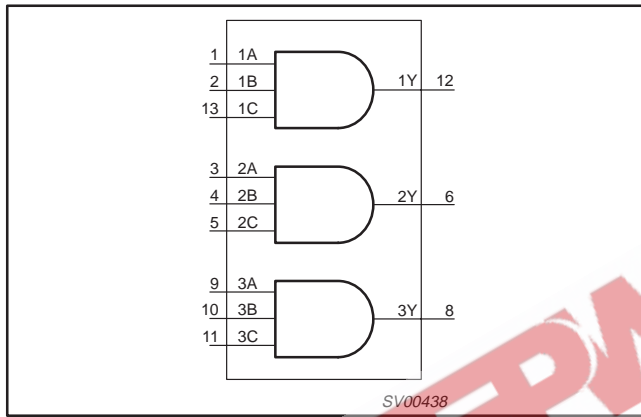
## PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A – 3A	Data inputs
2, 4, 10	1B – 3B	Data inputs
7	GND	Ground (0 V)
12, 6, 8	1Y – 3Y	Data outputs
13, 5, 11	1C – 3C	Data inputs
14	V <sub>CC</sub>	Positive supply voltage

## LOGIC DIAGRAM (ONE GATE)



## LOGIC SYMBOL



## FUNCTION TABLE

INPUTS			OUTPUTS
nA	nB	nC	nY
L	L	L	L
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H

### NOTES:

H = HIGH voltage level  
L = LOW voltage level

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V <sub>CC</sub>	DC supply voltage (for max. speed performance)		2.7	3.6	V
V <sub>CC</sub>	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V <sub>I</sub>	DC input voltage range		0	5.5	V
V <sub>O</sub>	DC output voltage range		0	V <sub>CC</sub>	V
T <sub>amb</sub>	Operating free-air temperature range		-40	+85	°C
t <sub>r</sub> , t <sub>f</sub>	Input rise and fall times	V <sub>CC</sub> = 1.2 to 2.7V V <sub>CC</sub> = 2.7 to 3.6V	0	20 10	ns/V

## Triple 3-input AND gate

74LVC11

**ABSOLUTE MAXIMUM RATINGS<sup>1</sup>**

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +6.5	V
$I_{IK}$	DC input diode current	$V_I < 0$	-50	mA
$V_I$	DC input voltage	Note 2	-0.5 to +5.5	V
$I_{OK}$	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
$V_O$	DC output voltage	Note 2	-0.5 to $V_{CC} + 0.5$	V
$I_O$	DC output source or sink current	$V_O = 0$ to $V_{CC}$	±50	mA
$I_{GND}, I_{CC}$	DC $V_{CC}$ or GND current		±100	mA
$T_{stg}$	Storage temperature range		-65 to +150	°C
$P_{TOT}$	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	500 500	mW

**NOTES:**

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

**DC ELECTRICAL CHARACTERISTICS**

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
$V_{IH}$	HIGH level Input voltage	$V_{CC} = 1.2V$	$V_{CC}$			V
		$V_{CC} = 2.7$ to $3.6V$	2.0			
$V_{IL}$	LOW level Input voltage	$V_{CC} = 1.2V$			GND	V
		$V_{CC} = 2.7$ to $3.6V$			0.8	
$V_{OH}$	HIGH level output voltage	$V_{CC} = 2.7V; V_I = V_{IH}$ or $V_{IL}; I_O = -12mA$	$V_{CC} - 0.5$			V
		$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; I_O = -100\mu A$	$V_{CC} - 0.2$	$V_{CC}$		
		$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; I_O = -12mA$	$V_{CC} - 0.6$			
		$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; I_O = -24mA$	$V_{CC} - 1.0$			
$V_{OL}$	LOW level output voltage	$V_{CC} = 2.7V; V_I = V_{IH}$ or $V_{IL}; I_O = 12mA$			0.40	V
		$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; I_O = 100\mu A$		GND	0.20	
		$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; I_O = 24mA$			0.55	
$I_I$	Input leakage current	$V_{CC} = 3.6V; V_I = 5.5V$ or GND		±0.1	±5	μA
$I_{CC}$	Quiescent supply current	$V_{CC} = 3.6V; V_I = V_{CC}$ or GND; $I_O = 0$		0.1	10	μA
$\Delta I_{CC}$	Additional quiescent supply current per input pin	$V_{CC} = 2.7V$ to $3.6V; V_I = V_{CC} - 0.6V; I_O = 0$		5	500	μA

**NOTE:**

- All typical values are at  $V_{CC} = 3.3V$  and  $T_{amb} = 25^\circ C$ .

# Triple 3-input AND gate

74LVC11

## AC CHARACTERISTICS

GND = 0 V;  $t_r = t_f \leq 2.5$  ns;  $C_L = 50$  pF;  $R_L = 500\Omega$ ;  $T_{amb} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		
			MIN	TYP <sup>1</sup>	MAX	MIN	MAX	
$t_{PHL}/t_{PLH}$	Propagation delay nA, nB, nC to nY	1, 2	-	3.7	6.2	-	7.0	ns

**NOTE:**

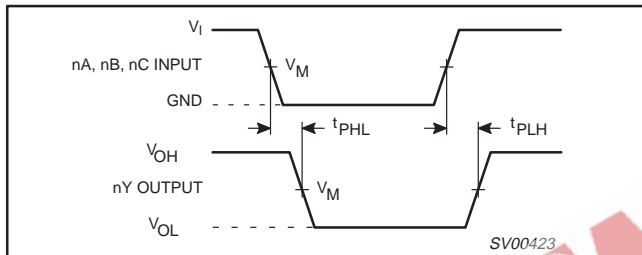
1. These typical values are at  $V_{CC} = 3.3V$  and  $T_{amb} = 25^\circ\text{C}$ .

## AC WAVEFORMS

$V_M = 1.5$  V at  $V_{CC} \geq 2.7$  V

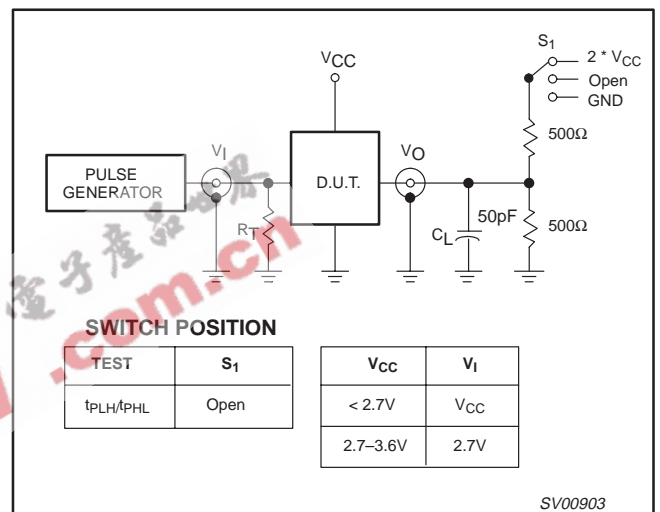
$V_M = 0.5 \cdot V_{CC}$  at  $V_{CC} < 2.7$  V

$V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.



**Waveform 1. Input (nA, nB, nC) to output (nY) propagation delays.**

## TEST CIRCUIT



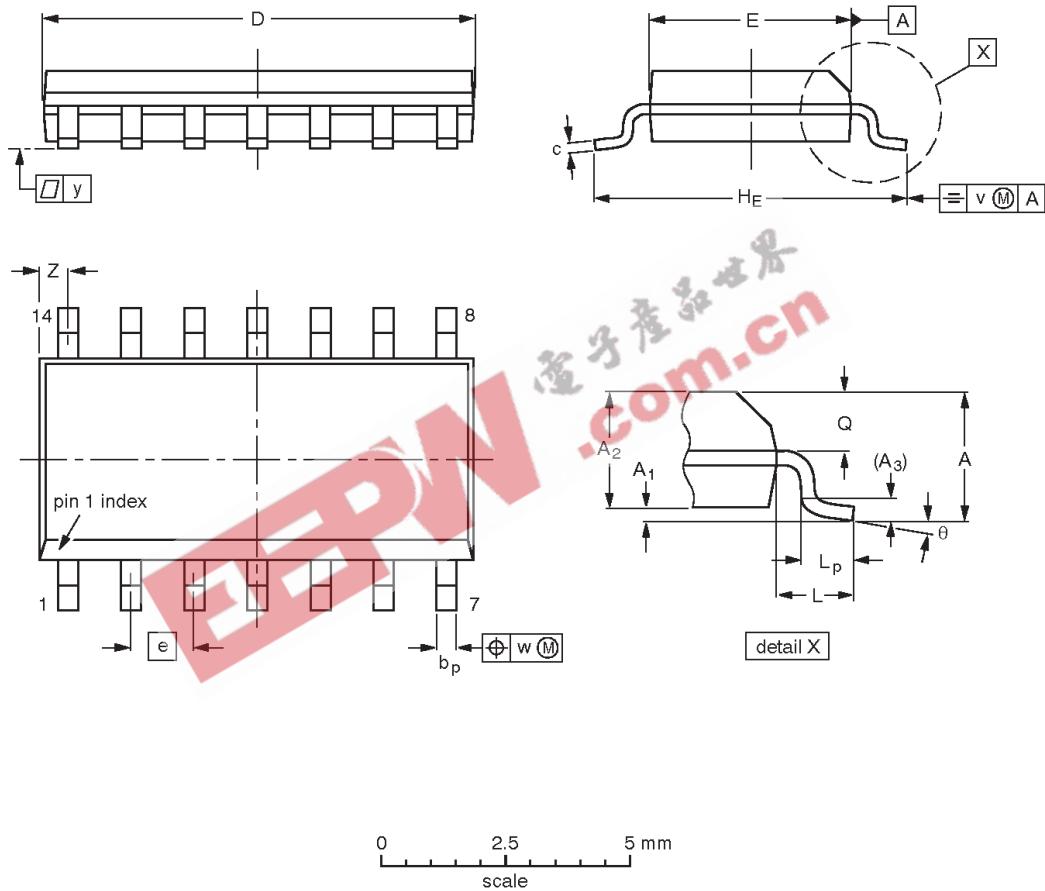
**Waveform 2. Load circuitry for switching times.**

Triple 3-input AND gate

74LVC11

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

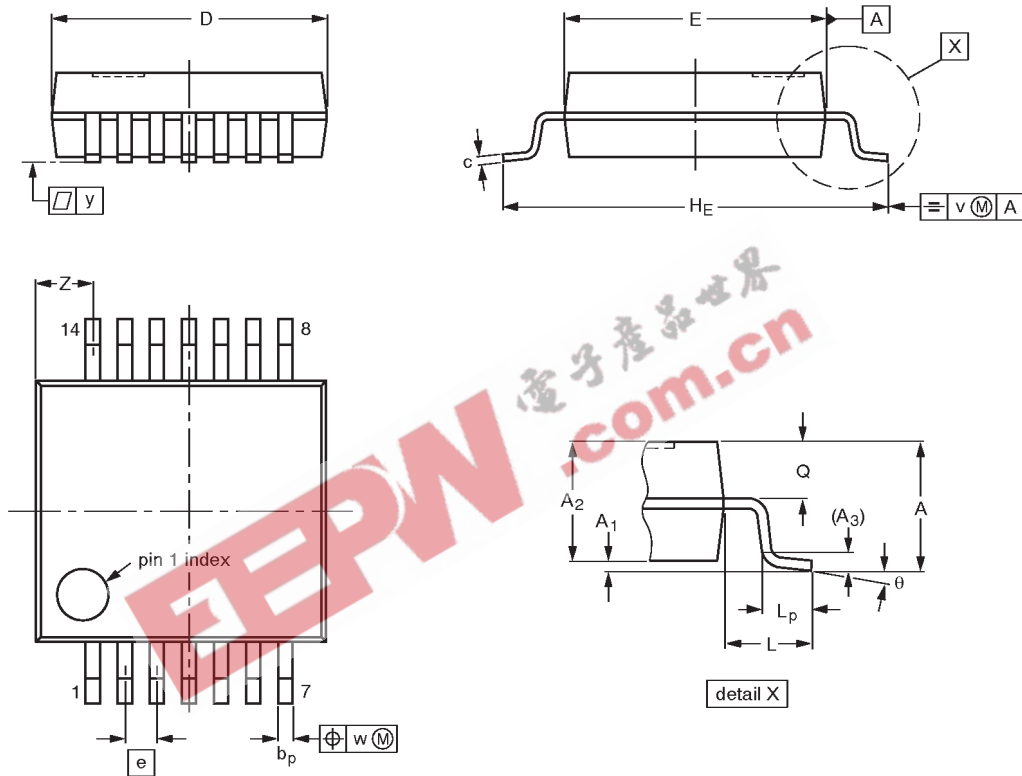
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				95-01-20 97-05-22

Triple 3-input AND gate

74LVC11

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



**DIMENSIONS** (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

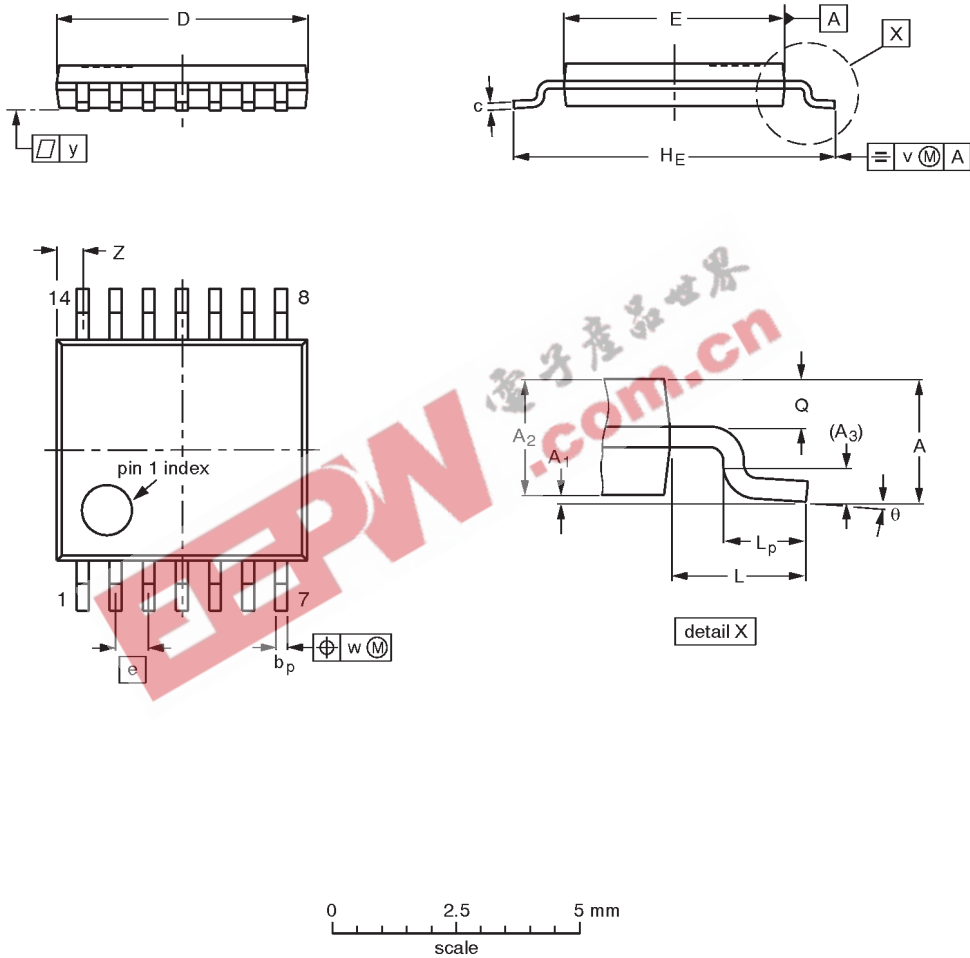
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT337-1		MO-150AB				<del>95-02-04</del> 96-01-18

Triple 3-input AND gate

74LVC11

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				-94-07-12- 95-04-04



---

Triple 3-input AND gate

74LVC11

---

NOTES



## Triple 3-input AND gate

74LVC11

## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

## Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information** — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

## Disclaimers

**Life support** — These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

**Right to make changes** — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Philips Semiconductors  
811 East Arques Avenue  
P.O. Box 3409  
Sunnyvale, California 94088-3409  
Telephone 800-234-7381

© Copyright Philips Electronics North America Corporation 1998  
All rights reserved. Printed in U.S.A.

print code

Date of release: 08-98

Document order number:

9397-750-04483

*Let's make things better.*