FAIRCHILD

SEMICONDUCTOR™

October 1996
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74VCX16245

Low Voltage 16-Bit Bidirectional Transceiver with 3.6V Tolerant Inputs and Outputs

General Description

The VCX16245 contains sixteen non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. Each byte has separate 3-STATE control inputs which can be shorted together for full 16-bit operation. The T/$\overline{R}$ inputs determine the direction of data flow through the device. The $\overline{OE}$ inputs disable both the A and B ports by placing them in a high impedance state.

The 74VCX16245 is designed for low voltage (1.2V to 3.6V) V_{CC} applications with I/O compatibility up to 3.6V.

The 74VCX16245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

■ 1.2V to 3.6V V_{CC} supply operation

■ 3.6V tolerant inputs and outputs

■ t_{PD}
   2.5 ns max for 3.0V to 3.6V V_{CC}

■ Power-off high impedance inputs and outputs

■ Supports live insertion/withdrawal (Note 1)

■ Static Drive (I_{OH}/I_{OL})
   ±24 mA @ 3.0V V_{CC}

■ Uses patented noise/EMI reduction circuitry

■ Latchup performance exceeds 300 mA

■ ESD performance:
   Human body model > 2000V
   Machine model >200V

■ Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

Note 1: To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.
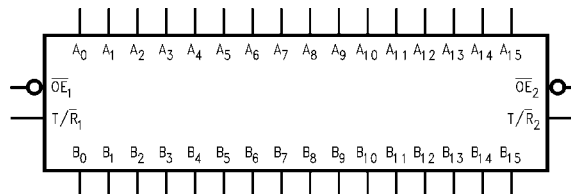
Ordering Code:

Order Number	Package Number	Package Description
74VCX16245G (Note 2)(Note 3)	BGA54A	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
74VCX16245MTD (Note 3)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

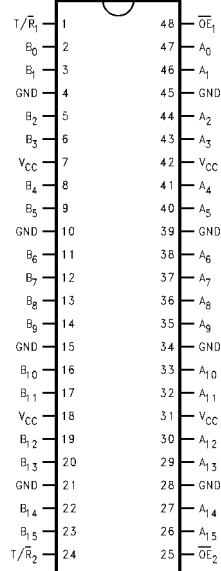**Note 2:** Ordering code "G" indicates Trays.

Note 3: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
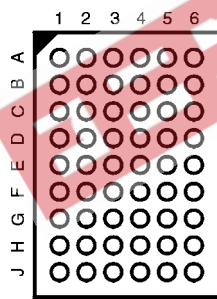
Logic Symbol

Connection Diagrams

Pin Assignment of TSSOP

$T/\overline{R}_1$	1	48	$\overline{OE}_1$
B_0	2	47	A_0
B_1	3	46	A_1
GND	4	45	GND
B_2	5	44	A_2
B_3	6	43	A_3
V_{CC}	7	42	V_{CC}
B_4	8	41	A_4
B_5	9	40	A_5
GND	10	39	GND
B_6	11	38	A_6
B_7	12	37	A_7
B_8	13	36	A_8
B_9	14	35	A_9
GND	15	34	GND
B_{10}	16	33	A_{10}
B_{11}	17	32	A_{11}
V_{CC}	18	31	V_{CC}
B_{12}	19	30	A_{12}
B_{13}	20	29	A_{13}
GND	21	28	GND
B_{14}	22	27	A_{14}
B_{15}	23	26	A_{15}
$T/\overline{R}_2$	24	25	$\overline{OE}_2$

Pin Assignment for FBGA

(Top Thru View)

Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$T/\overline{R}_n$	Transmit/Receive Input
A_0–A_{15}	Side A Inputs or 3-STATE Outputs
B_0–B_{15}	Side B Inputs or 3-STATE Outputs
NC	No Connect

FBGA Pin Assignments

	1	2	3	4	5	6
A	B_0	NC	$T/\overline{R}_1$	$\overline{OE}_1$	NC	A_0
B	B_2	B_1	NC	NC	A_1	A_2
C	B_4	B_3	V_{CC}	V_{CC}	A_3	A_4
D	B_6	B_5	GND	GND	A_5	A_6
E	B_8	B_7	GND	GND	A_7	A_8
F	B_{10}	B_9	GND	GND	A_9	A_{10}
G	B_{12}	B_{11}	V_{CC}	V_{CC}	A_{11}	A_{12}
H	B_{14}	B_{13}	NC	NC	A_{13}	A_{14}
J	B_{15}	NC	$T/\overline{R}_2$	$\overline{OE}_2$	NC	A_{15}

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$T/\overline{R}_1$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH Z State on A_0–A_7, B_0–B_7

Inputs		Outputs
$\overline{OE}_2$	$T/\overline{R}_2$	
L	L	Bus B_8–B_{15} Data to Bus A_8–A_{15}
L	H	Bus A_8–A_{15} Data to Bus B_8–B_{15}
H	X	HIGH Z State on A_8–A_{15}, B_8–B_{15}

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial (HIGH or LOW, inputs and I/O's may not float)
Z = High Impedance

Logic Diagram

1 of 16

Absolute Maximum Ratings(Note 4)

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage (V_I)	−0.5V to +4.6V
Output Voltage (V_O)	
Outputs 3-STATE	−0.5V to +4.6V
Outputs Active (Note 5)	−0.5 to V_{CC} + 0.5V
DC Input Diode Current (I_{IK}) $V_I < 0V$	−50 mA
DC Output Diode Current (I_{OK})	
$V_O < 0V$	−50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current	
(I_{OH}/I_{OL})	±50 mA
DC V_{CC} or Ground Current per	
Supply Pin (I_{CC} or Ground)	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C

Recommended Operating Conditions (Note 6)

Power Supply	
Operating	1.2V to 3.6V
Input Voltage	−0.3V to 3.6V
Output Voltage (V_O)	
Output in Active States	0V to V_{CC}
Output in 3-STATE	0.0V to 3.6V
Output Current in I_{OH}/I_{OL}	
V_{CC} = 3.0V to 3.6V	±24 mA
V_{CC} = 2.3V to 2.7V	±18 mA
V_{CC} = 1.65V to 2.3V	±6 mA
V_{CC} = 1.4V to 1.6V	±2 mA
V_{CC} = 1.2V	±100 μA
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10 ns/V

Note 4: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The Recommended Operating Conditions tables will define the conditions for actual device operation.

Note 5: I_O Absolute Maximum Rating must be observed.

Note 6: Floating or unused pin (inputs or I/O's) must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.7 - 3.6	2.0		
			2.3 - 2.7	1.6		
			1.65 - 2.3	0.65 x V_{CC}		V
			1.4 - 1.6	0.65 x V_{CC}		
			1.2	0.65 x V_{CC}		
V_{IL}	LOW Level Input Voltage		2.7 - 3.6		0.8	
			2.3 - 2.7		0.7	
			1.65 - 2.3		0.35 x V_{CC}	V
			1.4 - 1.6		0.35 x V_{CC}	
			1.2		0.05 x V_{CC}	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.7 - 3.6	V_{CC} - 0.2		
		I_{OH} = −12 mA	2.7	2.2		
		I_{OH} = −18 mA	3.0	2.4		
		I_{OH} = −24 mA	3.0	2.2		
		I_{OH} = −100 μA	2.3 - 2.7	V_{CC} - 0.2		
		I_{OH} = −6 mA	2.3	2.0		
		I_{OH} = −12 mA	2.3	1.8		V
		I_{OH} = −18 mA	2.3	1.7		
		I_{OH} = −100 μA	1.65 - 2.3	V_{CC} - 0.2		
		I_{OH} = −6 mA	1.65	1.25		
		I_{OH} = −100 μA	1.4 - 1.6	V_{CC} - 0.2		
		I_{OH} = −2 mA	1.4	1.05		
		I_{OH} = −100 μA	1.2	V_{CC} - 0.2		

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_CC (V)	Min	Max	Units
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.7 - 3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	
		I_{OL} = 18 mA	3.0		0.4	
		I_{OL} = 24 mA	3.0		0.55	
		I_{OL} = 100 μA	2.3 - 2.7		0.2	
		I_{OL} = 12 mA	2.3		0.4	
		I_{OL} = 18 mA	2.3		0.6	
		I_{OL} = 100 μA	1.65 - 2.3		0.2	
		I_{OL} = 6 mA	1.65		0.3	
		I_{OL} = 100 μA	1.4 - 1.6		0.2	
		I_{OL} = 2 mA	1.4		0.35	
		I_{OL} = 100 μA	1.2		V_{CC} - 0.1	
I_I	Input Leakage Current	$0V \leq V_I \leq 3.6V$	1.2 - 3.6		±5.0	μA
I_{OZ}	3-STATE Output Leakage	$0V \leq V_O \leq 3.6V$ $V_I = V_{IH}$ or V_{IL}	1.2 - 3.6		±10	μA
I_{OFF}	Power Off Leakage Current	$0V \leq (V_I, V_O) \leq 3.6V$	0		10	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	1.2 - 3.6		20	μA
		$V_{CC} \leq (V_I, V_O) \leq 3.6V$ (Note 7)	1.2 - 3.6		±20	
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.7 - 3.6		750	μA

Note 7: Outputs disabled or 3-STATE only.

AC Electrical Characteristics (Note 8)

Symbol	Parameter	Conditions	V_CC (V)	T_A = −40°C to +85°C Min	T_A = −40°C to +85°C Max	Units	Figure Number
t_{PHL} t_{PLH}	Propagation Delay	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	0.8	2.5	ns	Figures 1, 2
			2.5 ± 0.2	1.0	3.0		
			1.8 ± 0.15	1.0	6.0		
		C_L = 15 pF, R_L = 2kΩ	1.5 ± 0.1	1.0	12.0		Figures 5, 6
			1.2	1.5	30		
t_{PZL} t_{PZH}	Output Enable Time	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	0.8	3.8	ns	Figures 1, 3, 4
			2.5 ± 0.2	1.0	4.9		
			1.8 ± 0.15	1.5	9.3		
		C_L = 15 pF, R_L = 2kΩ	1.5 ± 0.1	1.0	18.6		Figures 5, 7, 8
			1.2	1.5	46.5		
t_{PLZ} t_{PHZ}	Output Disable Time	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	0.8	3.7	ns	Figures 1, 3, 4
			2.5 ± 0.2	1.0	4.2		
			1.8 ± 0.15	1.5	7.6		
		C_L = 15 pF, R_L = 2kΩ	1.5 ± 0.1	1.0	15.2		Figures 5, 7, 8
			1.2	1.5	38		
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 9)	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3		0.5	ns	
			2.5 ± 0.2		0.5		
			1.8 ± 0.15		0.75		
		C_L = 15 pF, R_L = 2kΩ	1.5 ± 0.1		1.5		
			1.2		1.5		

Note 8: For C_L = 50pF, add approximately 300ps to the AC maximum specification.

Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = +25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8	0.25	V
			2.5	0.6	
			3.3	0.8	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8	−0.25	V
			2.5	−0.6	
			3.3	−0.8	
V_{OHV}	Quiet Output Dynamic Valley V_{OH}	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0V$	1.8	1.5	V
			2.5	1.9	
			3.3	2.2	

Capacitance

Symbol	Parameter	Conditions	$T_A = +25°C$ Typical	Units
C_{IN}	Input Capacitance	$V_{CC} = 1.8V$, 2.5V, or 3.3V, $V_I = 0V$ or V_{CC}	6	pF
$C_{I/O}$	Output Capacitance	$V_I = 0V$, or V_{CC}, $V_{CC} = 1.8V$, 2.5V or 3.3V	7	pF
C_{PD}	Power Dissipation Capacitance	$V_I = 0V$ or V_{CC}, $F = 10$ MHz, $V_{CC} = 1.8V$, 2.5V or 3.3V	20	pF

AC Loading and Waveforms (V$_{CC}$ 3.3V $\pm$ 0.3V to 1.8V $\pm$ 0.15V)

FIGURE 1. AC Test Circuit

TEST	SWITCH
t$_{PLH}$, t$_{PHL}$	Open
t$_{PZL}$, t$_{PLZ}$	6V at V$_{CC}$ = 3.3 $\pm$ 0.3V; V$_{CC}$ x 2 at V$_{CC}$ = 2.5 $\pm$ 0.2V; 1.8V $\pm$ 0.15V
t$_{PZH}$, t$_{PHZ}$	GND

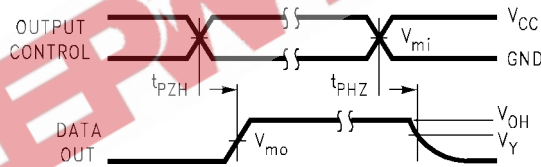**FIGURE 2. Waveform for Inverting and Non-inverting Functions**

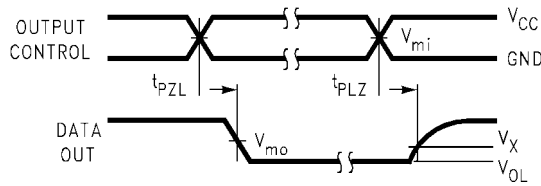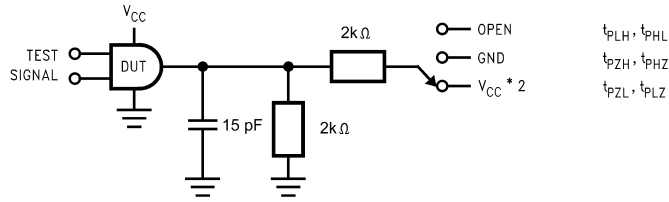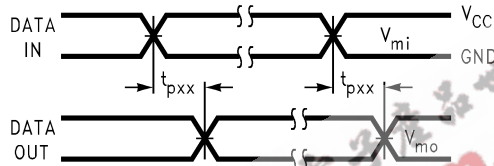**FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic**

FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Symbol	V$_{CC}$		
	3.3V $\pm$ 0.3V	2.5V $\pm$ 0.2V	1.8V $\pm$ 0.15V
V$_{mi}$	1.5V	V$_{CC}$/2	V$_{CC}$/2
V$_{mo}$	1.5V	V$_{CC}$/2	V$_{CC}$/2
V$_X$	V$_{OL}$ + 0.3V	V$_{OL}$ + 0.15V	V$_{OL}$ + 0.15V
V$_Y$	V$_{OH}$ − 0.3V	V$_{OH}$ − 0.15V	V$_{OH}$ − 0.15V

AC Loading and Waveforms (V$_{CC}$ 1.5V $\pm$ 0.1V to 1.2V)

TEST	SWITCH
t$_{PLH}$, t$_{PHL}$	Open
t$_{PZL}$, t$_{PLZ}$	V$_{CC}$ x 2 at V$_{CC}$ = 1.5 $\pm$ 0.1V

FIGURE 5. AC Test Circuit

FIGURE 6. Waveform for Inverting and Non-Inverting Functions

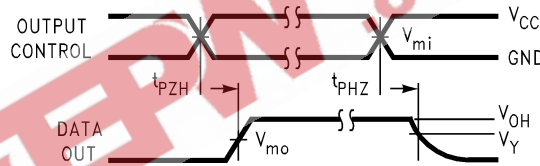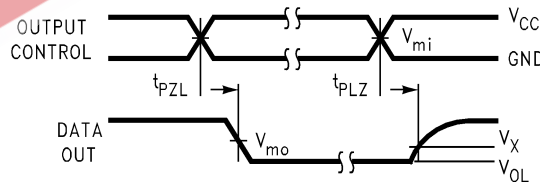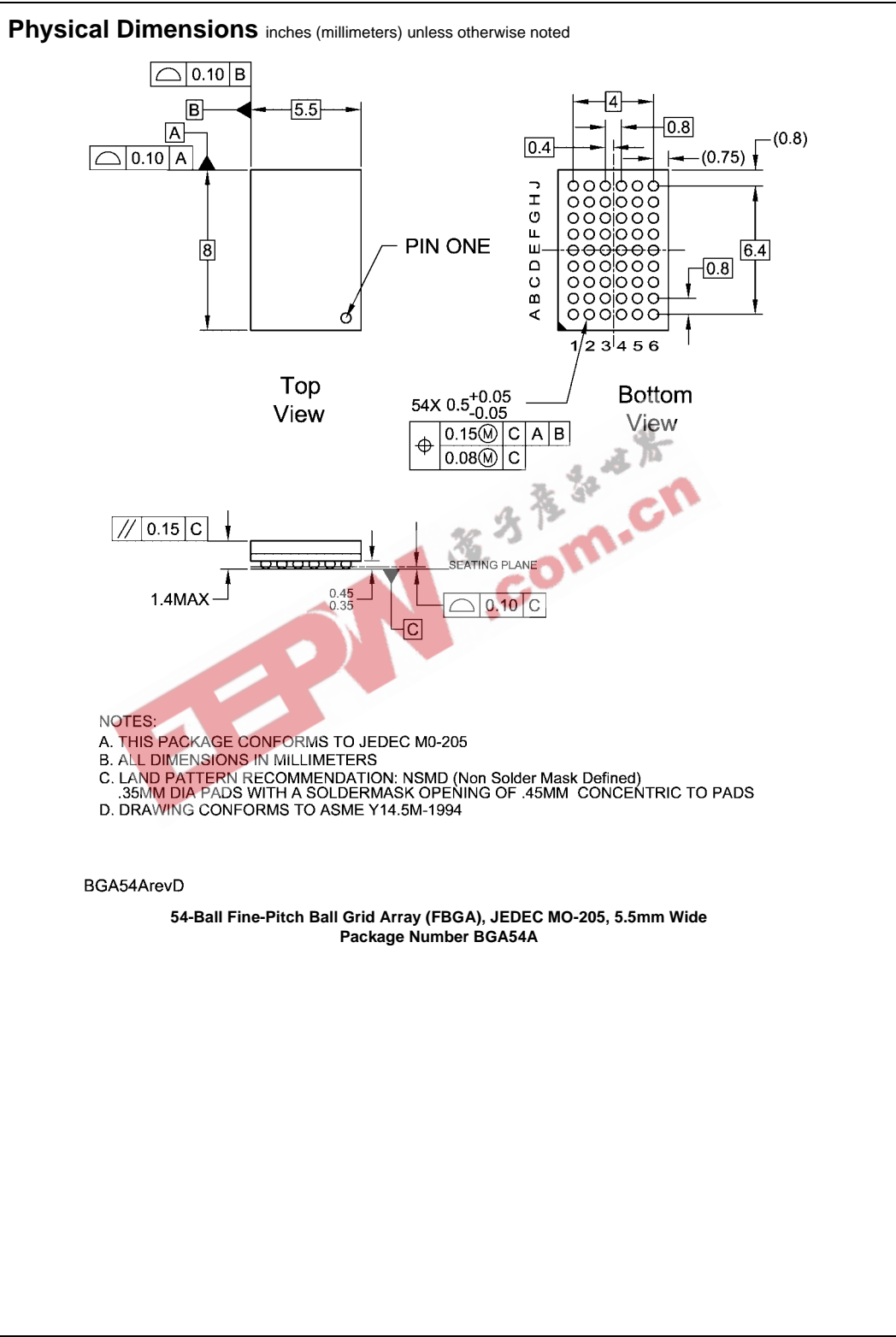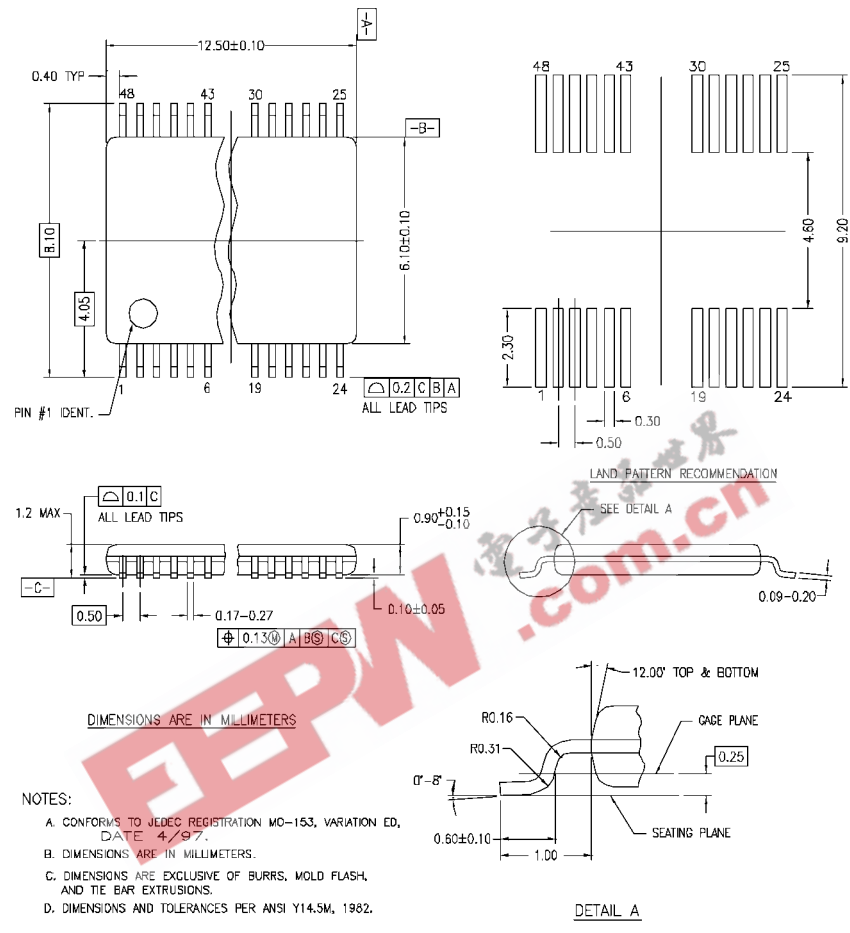**FIGURE 7. 3-STATE Output High Enable and Disable Times for Low Voltage Logic**

FIGURE 8. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Symbol	V$_{CC}$
	1.5V $\pm$ 0.1V
V$_{mi}$	V$_{CC}$/2
V$_{mo}$	V$_{CC}$/2
V$_X$	V$_{OL}$ + 0.1V
V$_Y$	V$_{OH}$ − 0.1V

Physical Dimensions inches (millimeters) unless otherwise noted

Top View

PIN ONE

Bottom View

54X 0.5$^{+0.05}_{-0.05}$

NOTES:
A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
   .35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA54A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

DIMENSIONS ARE IN MILLIMETERS

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION ED, DATE 4/97.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48REVC

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

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