DATA SHEET

74LVC162373A; 74LVCH162373A

16-bit D-type transparent latch; 30 Ω series termination resistors; 5 V tolerant inputs/outputs; 3-state

Product specification
Supersedes data of 1999 Aug 05

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Philips Semiconductors

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16-bit D-type transparent latch; 30 Ω series termination resistors; 5 V tolerant inputs/outputs; 3-state

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FEATURES

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 to 3.6 V
- CMOS low power consumption
- MULTIBYTE flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bushold (74LVCH162373A only)
- High-impedance when V_{CC} = 0 V
- Complies with JEDEC standard no. 8-1A
- ESD protection:
  HBM EIA/JESD22-A114-A exceeds 2000 V
  MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from –40 to +85 °C and –40 to +125 °C.

DESCRIPTION

The 74LVC(H)162373A is a 16-bit D-type transparent latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. One latch enable (pin nLE) input and one output enable (pin n$\overline{OE}$) are provided for each octal. Inputs can be driven from either 3.3 or 5 V devices. In 3-state operation, outputs can handle 5 V. These features allow the use of these devices in a mixed 3.3 and 5 V environment.

The 74LVC(H)162373A consists of 2 sections of eight D-type transparent latches with 3-state true outputs. When pin nLE is HIGH, data at the corresponding data inputs (pins nDn) enter the latches. In this condition the latches are transparent, i.e., a latch output will change each time its corresponding data inputs changes.

When pin nLE is LOW the latches store the information that was present at the data inputs a set-up time preceding the HIGH-to-LOW transition of pin nLE. When pin n$\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When pin n$\overline{OE}$ is HIGH, the outputs go to the high-impedance OFF-state. Operation of the n$\overline{OE}$ input does not affect the state of the latches.

The 74LVCH162373A bushold data inputs eliminates the need for external pull-up resistors to hold unused inputs.

The 74LVC(H)162373A is designed with 30 Ω series termination resistors in both high and low output stages to reduce line noise.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nDn to nQn	C_L = 50 pF; V_{CC} = 3.3 V	3.3	ns
	propagation delay nLE to nQn	C_L = 50 pF; V_{CC} = 3.3 V	3.5	ns
t_{PZH}/t_{PZL}	3-state output enable time n$\overline{OE}$ to nQn	C_L = 50 pF; V_{CC} = 3.3 V	4.0	ns
t_{PHZ}/t_{PLZ}	3-state output disable time n$\overline{OE}$ to nQn	C_L = 50 pF; V_{CC} = 3.3 V	3.4	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation per latch	V_{CC} = 3.3 V; notes 1 and 2		
		outputs enabled	26	pF
		outputs disabled	19	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	TEMPERATURE RANGE	PACKAGE			
		PINS	PACKAGE	MATERIAL	CODE
74LVC162373ADGG	–40 to +125 °C	48	TSSOP48	plastic	SOT362-1
74LVCH162373ADGG	–40 to +125 °C	48	TSSOP48	plastic	SOT362-1
74LVC162373ADL	–40 to +125 °C	48	SSOP48	plastic	SOT370-1
74LVCH162373ADL	–40 to +125 °C	48	SSOP48	plastic	SOT370-1

FUNCTION TABLE

Per section of eight bits; note 1

OPERATING MODES	INPUT			INTERNAL LATCH	OUTPUT nQn
	$n\overline{OE}$	nLE	nDn		
Enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	Z
	H	L	h	H	Z

Note

1. H = HIGH voltage level;

   h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition;

   L = LOW voltage level;

   l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition;

   Z = high-impedance OFF-state.

PINNING

SYMBOL	PIN	DESCRIPTION
$1\overline{OE}$	1	output enable input (active LOW)
1Q0	2	data output
1Q1	3	data output
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
1Q2	5	data output
1Q3	6	data output
V_{CC}	7, 18, 31, 42	supply voltage
1Q4	8	data output
1Q5	9	data output
1Q6	11	data output
1Q7	12	data output
2Q0	13	data output
2Q1	14	data output
2Q2	16	data output
2Q3	17	data output
2Q4	19	data output
2Q5	20	data output
2Q6	22	data output
2Q7	23	data output
$2\overline{OE}$	24	output enable input (active LOW)
2LE	25	latch enable input (active HIGH)
2D7	26	data input
2D6	27	data input
2D5	29	data input
2D4	30	data input
2D3	32	data input
2D2	33	data input
2D1	35	data input
2D0	36	data input
1D7	37	data input
1D6	38	data input
1D5	40	data input
1D4	41	data input
1D3	43	data input
1D2	44	data input
1D1	46	data input
1D0	47	data input
1LE	48	latch enable input (active HIGH)

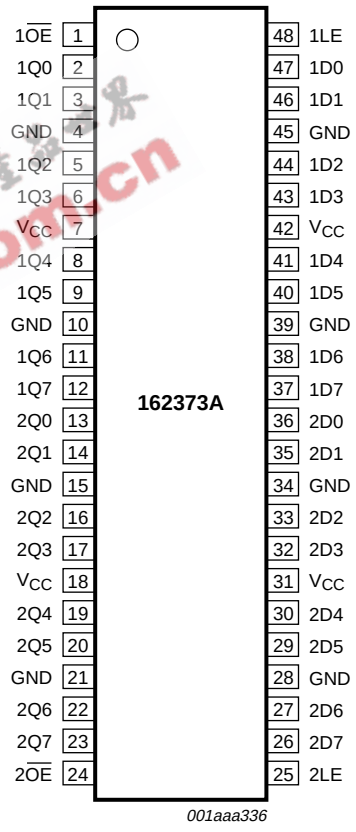


Fig.1 Pin configuration SSOP48 and TSSOP48.

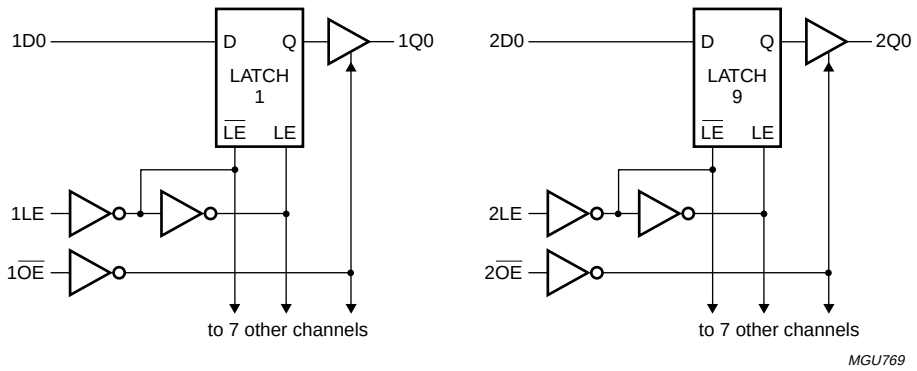


Fig.2 Logic diagram.

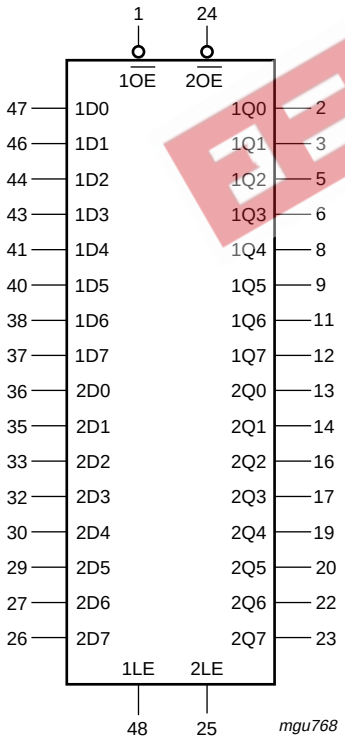


Fig.3 Logic symbol.

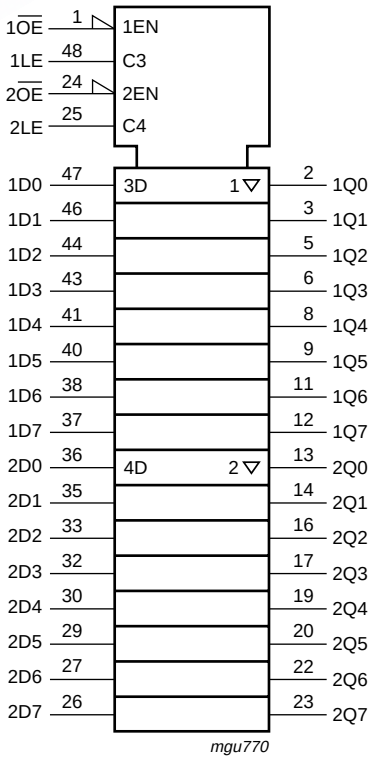


Fig.4 Logic symbol (IEEE/IEC).

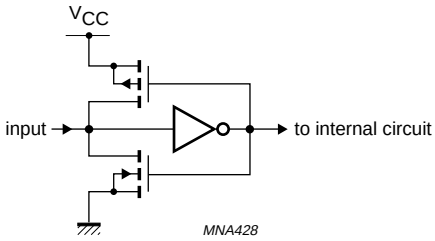


Fig.5 Bushold circuit.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	for maximum speed performance	2.7	3.6	V
		for low-voltage applications	1.2	3.6	V
V_I	input voltage		0	5.5	V
V_O	output voltage	output HIGH or LOW state	0	V_{CC}	V
		output 3-state	0	5.5	V
T_{amb}	operating ambient temperature	in free-air	–40	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.2 to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 to 3.6 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0$	–	–50	mA
V_I	input voltage	note 1	–0.5	+6.5	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$	–	±50	mA
V_O	output voltage	output HIGH or LOW state; note 1	–0.5	V_{CC} + 0.5	V
		output 3-state; note 1	–0.5	+6.5	V
I_O	output source or sink current	V_O = 0 to V_{CC}	–	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 to +125 °C; note 2	–	500	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +85 °C; note 1							
V_{IH}	HIGH-level input voltage		1.2	V_{CC}	–	–	V
			2.7 to 3.6	2.0	–	–	V
V_{IL}	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = −100 µA	2.7 to 3.6	V_{CC} − 0.2	V_{CC}[2]	–	V
		I_O = −6 mA	2.7	V_{CC} − 0.5	–	–	V
		I_O = −12 mA	3.0	V_{CC} − 0.8	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 100 µA	2.7 to 3.6	–	GND[2]	0.20	V
		I_O = 6 mA	2.7	–	–	0.40	V
		I_O = 12 mA	3.0	–	–	0.55	V
I_{LI}	input leakage current	V_I = 5.5 V or GND; note 3	3.6	–	±0.1	±5	µA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND; note 3	3.6	–	±0.1	±5	µA
I_{off}	power-off leakage current	V_I or V_O = 5.5 V	0	–	±0.1	±10	µA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	3.6	–	0.1	20	µA
ΔI_{CC}	additional quiescent supply current per input pin	V_I = V_{CC} − 0.6 V; I_O = 0	2.7 to 3.6	–	5[2]	500	µA
I_{BHL}	bushold LOW sustaining current	V_I = 0.8 V; notes 4 and 5	3.0	75	–	–	µA
I_{BHH}	bushold HIGH sustaining current	V_I = 2.0 V; notes 4 and 5	3.0	−75	–	–	µA
I_{BHLO}	bushold LOW overdrive current	notes 4 and 6	3.6	500	–	–	µA
I_{BHHO}	bushold HIGH overdrive current	notes 4 and 6	3.6	−500	–	–	µA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +125 °C							
V_{IH}	HIGH-level input voltage		1.2	V_{CC}	–	–	V
			2.7 to 3.6	2.0	–	–	V
V_{IL}	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = −100 µA	2.7 to 3.6	V_{CC} − 0.3	–	–	V
		I_O = −6 mA	2.7	V_{CC} − 0.65	–	–	V
		I_O = −12 mA	3.0	V_{CC} − 1	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 100 µA	2.7 to 3.6	–	–	0.3	V
		I_O = 6 mA	2.7	–	–	0.6	V
		I_O = 12 mA	3.0	–	–	0.8	V
I_{LI}	input leakage current	V_I = 5.5 V or GND; note 3	3.6	–	–	±20	µA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND; note 3	3.6	–	–	±20	µA
I_{off}	power off leakage current	V_I or V_O = 5.5 V	0	–	–	±20	µA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	3.6	–	–	80	µA
ΔI_{CC}	additional quiescent supply current per input pin	V_I = V_{CC} − 0.6 V; I_O = 0	2.7 to 3.6	–	–	5000	µA
I_{BHL}	bushold LOW sustaining current	V_I = 0.8 V; notes 4 and 5	3.0	60	–	–	µA
I_{BHH}	bushold HIGH sustaining current	V_I = 2.0 V; notes 4 and 5	3.0	−60	–	–	µA
I_{BHLO}	bushold LOW overdrive current	notes 4 and 6	3.6	500	–	–	µA
I_{BHHO}	bushold HIGH overdrive current	notes 4 and 6	3.6	−500	–	–	µA

Notes

1. All typical values are measured at T_{amb} = 25 °C.
2. Measured at V_{CC} = 3.3 V.
3. For bushold parts, the bushold circuit is switched off when V_I > V_{CC} allowing 5.5 V on the input pin.
4. Valid for data inputs of bushold parts (LVCH162373A) only. For data inputs only; control inputs do not have a bushold circuit.
5. The specified sustaining current at the data inputs holds the input below the specified V_I level.
6. The specified overdrive current at the data input forces the data input to the opposite logic input state.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 500\ \Omega$.

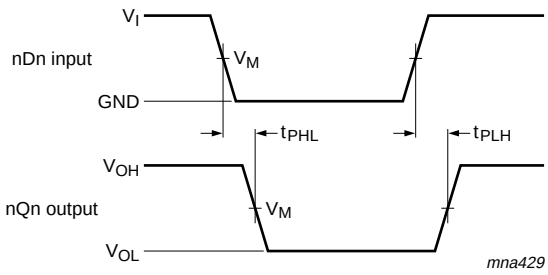
SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 to +85 °C; note1							
t_{PHL}/t_{PLH}	propagation delay nDn to nQn	see Fig 6 and 10	1.2	–	12	–	ns
			2.7	1.5	–	6.7	ns
			3.0 to 3.6	1.0	3.3[2]	5.9	ns
	propagation delay nLE to nQn	see Fig 7 and 10	1.2	–	14	–	ns
			2.7	1.5	–	7.0	ns
			3.0 to 3.6	1.5	3.5[2]	6.1	ns
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}$ to nQn	see Fig 8 and 10	1.2	–	18	–	ns
			2.7	1.5	–	7.5	ns
			3.0 to 3.6	1.0	4.0[2]	6.1	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}$ to nQn	see Fig 8 and 10	1.2	–	11	–	ns
			2.7	1.5	–	4.8	ns
			3.0 to 3.6	1.5	3.4[2]	4.6	ns
t_W	nLE pulse width HIGH	see Fig 7	1.2	–	–	–	ns
			2.7	3.0	–	–	ns
			3.0 to 3.6	3.0	2.0[2]	–	ns
t_{su}	set-up time nDn to nLE	see Fig 9	1.2	–	–	–	ns
			2.7	2.0	–	–	ns
			3.0 to 3.6	2.0	1.0[2]	–	ns
t_h	hold time nDn to nLE	see Fig 9	1.2	–	–	–	ns
			2.7	0.9	–	–	ns
			3.0 to 3.6	0.9	−1.0[2]	–	ns
$t_{sk(0)}$	skew	note 3	3.0 to 3.6	–	–	1.0	ns

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 to +125 °C							
t_{PHL}/t_{PLH}	propagation delay nDn to nQn	see Fig 6 and 10	1.2	–	–	–	ns
			2.7	1.5	–	8.5	ns
			3.0 to 3.6	1.0	–	7.5	ns
	propagation delay nLE to nQn	see Fig 7 and 10	1.2	–	–	–	ns
			2.7	1.5	–	9.0	ns
			3.0 to 3.6	1.5	–	8.0	ns
t_{PZH}/t_{PZL}	3-state output enable time n$\overline{OE}$ to nQn	see Fig 8 and 10	1.2	–	–	–	ns
			2.7	1.5	–	9.5	ns
			3.0 to 3.6	1.0	–	8.0	ns
t_{PHZ}/t_{PLZ}	3-state output disable time n$\overline{OE}$ to nQn	see Fig 8 and 10	1.2	–	–	–	ns
			2.7	1.5	–	6.0	ns
			3.0 to 3.6	1.5	–	6.0	ns
t_W	nLE pulse width HIGH	see Fig 7	1.2	–	–	–	ns
			2.7	3.0	–	–	ns
			3.0 to 3.6	3.0	–	–	ns
t_{su}	set-up time nDn to nLE	see Fig 9	1.2	–	–	–	ns
			2.7	2.0	–	–	ns
			3.0 to 3.6	2.0	–	–	ns
t_h	hold time nDn to nLE	see Fig 9	1.2	–	–	–	ns
			2.7	0.9	–	–	ns
			3.0 to 3.6	0.9	–	–	ns
$t_{sk(0)}$	skew	note 3	3.0 to 3.6	–	–	1.5	ns

Notes

1. All typical values are measured at T_{amb} = 25 °C.
2. Measured at V_{CC} = 3.3 V.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

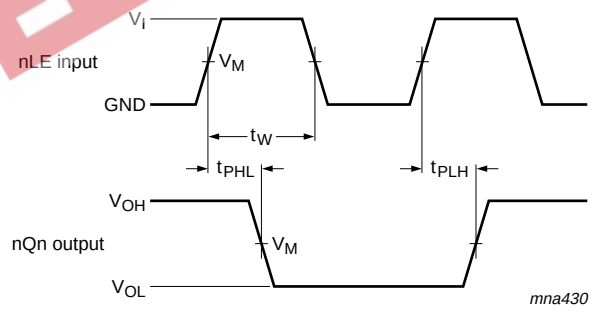
AC WAVEFORMS



V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.2 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

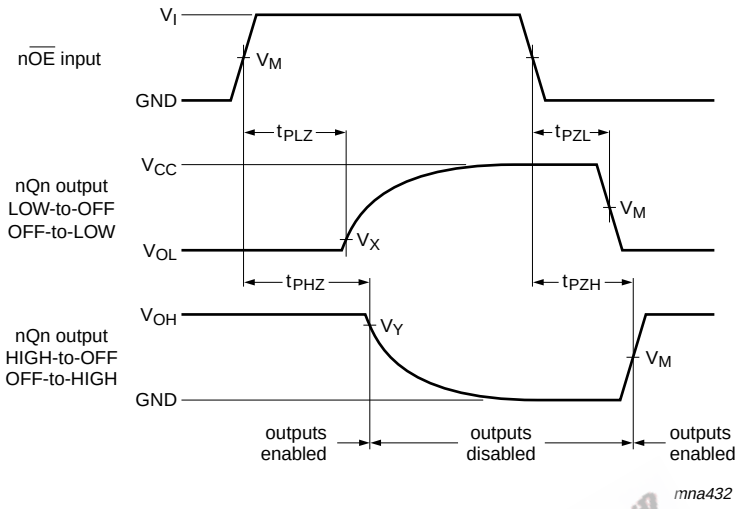
Fig.6 Input (nDn) to output (nQn) propagation delays.



V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.2 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

Fig.7 Latch enable input (nLE) pulse width, and the latch enable input to output (nQn) propagation delays.

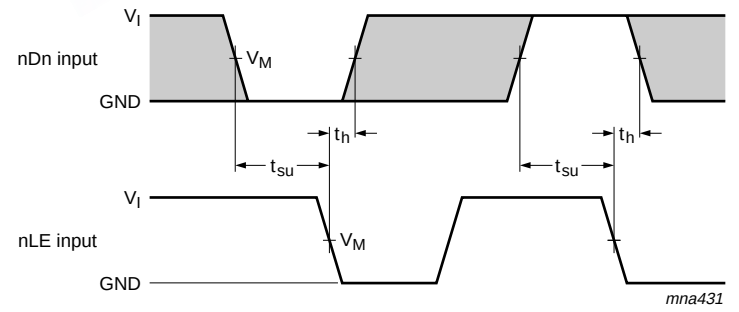


V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.2 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns

$V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V.
$V_X = V_{OL} + 0.1V_{CC}$ at $V_{CC} < 2.7$ V.
$V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V.
$V_Y = V_{OH} - 0.1V_{CC}$ at $V_{CC} < 2.7$ V.

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

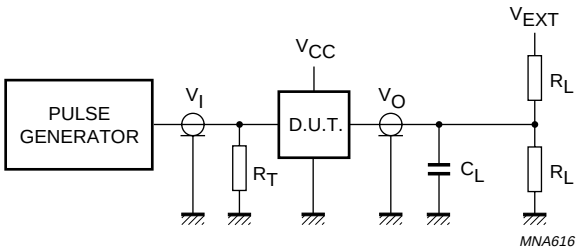
Fig.8 3-state enable and disable times.



V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.2 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns

The shaded areas indicate when the input is permitted to change for predictable performance.

Fig.9 Data set-up and hold times for the nDn input to the nLE input.



V_{CC}	V_I	C_L	R_L	V_{EXT}		
				t_{PLH}/t_{PHL}	t_{PZH}/t_{PHZ}	t_{PZL}/t_{PLZ}
1.2 V	V_{CC}	50 pF	500 Ω(1)	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	50 pF	500 Ω	open	GND	$2 \times V_{CC}$
3.0 to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	$2 \times V_{CC}$

Note

1. The circuit performs better when R_L = 1000 Ω.

Definitions for test circuit:

R_L = Load resistor.

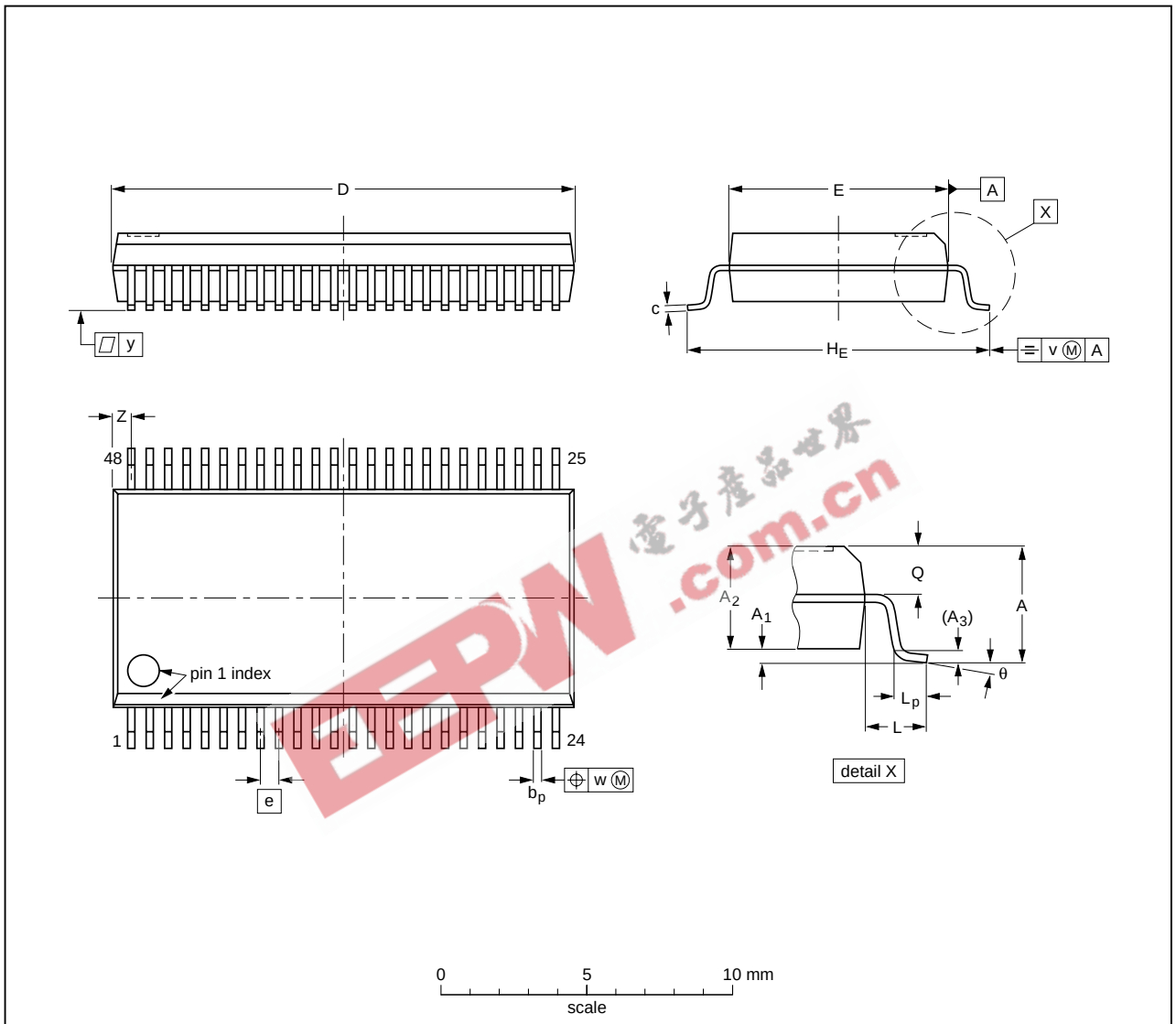
C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.10 Load circuitry for switching times.

PACKAGE OUTLINES

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**



DIMENSIONS (mm are the original dimensions)

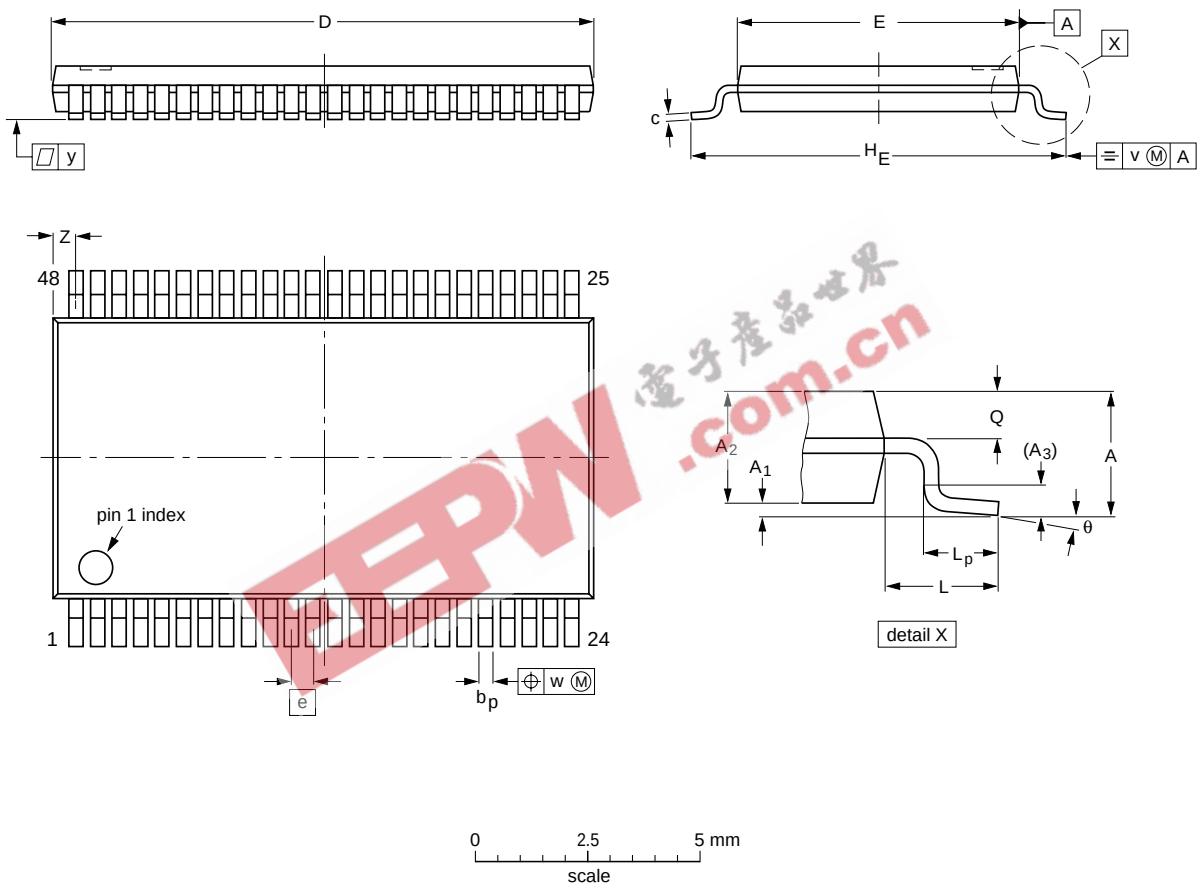
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT370-1		MO-118				~~99-12-27~~ 03-02-19

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	**0.2** **0.1**	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~99-12-27~~ 03-02-19

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LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
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