

## 74AC573 • 74ACT573

### Octal Latch with 3-STATE Outputs

#### General Description

The 74AC573 and 74ACT573 are high-speed octal latches with buffered common Latch Enable (LE) and buffered common Output Enable (OE) inputs.

The 74AC573 and 74ACT573 are functionally identical to the 74AC373 and 74ACT373 but with inputs and outputs on opposite sides.

#### Features

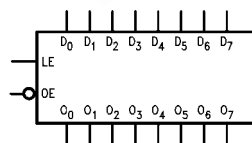
- $I_{CC}$  and  $I_{OZ}$  reduced by 50%
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 74AC373 and 74ACT373
- 3-STATE outputs for bus interfacing
- Outputs source/sink 24 mA
- 74ACT573 has TTL-compatible inputs

#### Ordering Code:

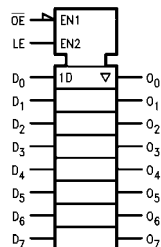
Order Number	Package Number	Package Description
74AC573SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74AC573SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC573MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC573PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT573SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74ACT573SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT573MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT573PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

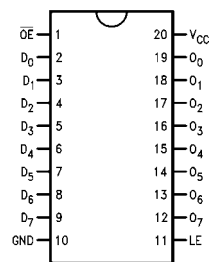
#### Logic Symbols



#### IEEE/IEC



#### Connection Diagram



#### Pin Descriptions

Pin Names	Description
$D_0$ - $D_7$	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	3-STATE Output Enable Input
$O_0$ - $O_7$	3-STATE Latch Outputs

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## Functional Description

The 74AC573 and 74ACT573 contain eight D-type latches with 3-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the  $D_n$  inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D-type input changes. When LE is LOW the latches store the information that was

present on the D-type inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE buffers are controlled by the Output Enable ( $\overline{OE}$ ) input. When  $\overline{OE}$  is LOW, the buffers are enabled. When  $\overline{OE}$  is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

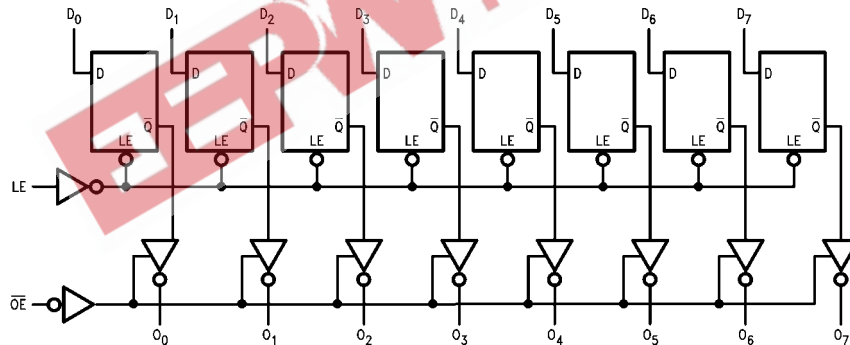
## Truth Table

Inputs			Outputs
$\overline{OE}$	LE	D	$O_n$
L	H	H	H
L	H	L	L
L	L	X	$O_0$
H	X	X	Z

H = HIGH Voltage  
L = LOW Voltage  
Z = High Impedance  
X = Immaterial

$O_0$  = Previous  $O_0$  before HIGH-to-LOW transition of Latch Enable

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 50$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Junction Temperature ( $T_J$ ) (PDIP)	140°C

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	
AC	2.0V to 6.0V
ACT	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
AC Devices	
$V_{IN}$ from 30% to 70% of $V_{CC}$	
$V_{CC}$ @ 3.0V, 4.5V, 5.5V	125 mV/ns
ACT Devices	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT<sup>™</sup> circuits outside databook specifications.

**DC Electrical Characteristics for AC**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Typ	Guaranteed Limits				
$V_{IH}$	Minimum HIGH Level Input Voltage	3.0	1.5	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
$V_{IL}$	Maximum LOW Level Input Voltage	3.0	1.5	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
$V_{OH}$	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu\text{A}$	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
			3.0		2.56	2.46	V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ (Note 2)
			4.5		3.86	3.76		
			5.5		4.86	4.76		
$V_{OL}$	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50 \mu\text{A}$	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
			3.0		0.36	0.44	V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ (Note 2)
			4.5		0.36	0.44		
			5.5		0.36	0.44		
$I_{IN}$ (Note 3)	Maximum Input Leakage Current	5.5		$\pm 0.1$	$\pm 1.0$	$\mu\text{A}$	$V_I = V_{CC}$ , GND	
$I_{OLD}$	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V$ Max	
$I_{OHD}$	Output Current (Note 4)	5.5			-75	mA	$V_{OHD} = 3.85V$ Min	
$I_{CC}$ (Note 3)	Maximum Quiescent Supply Current	5.5		4.0	40.0	$\mu\text{A}$	$V_{IN} = V_{CC}$ or GND	
$I_{OZ}$	Maximum 3-STATE Leakage Current	5.5		$\pm 0.25$	$\pm 2.5$	$\mu\text{A}$	$V_I$ (OE) = $V_{IL}$ , $V_{IH}$ $V_I = V_{CC}$ , GND $V_O = V_{CC}$ , GND	

**Note 2:** All outputs loaded; thresholds on input associated with output under test.

**Note 3:**  $I_{IN}$  and  $I_{CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{CC}$ .

**Note 4:** Maximum test duration 2.0 ms, one output loaded at a time.

## AC Electrical Characteristics for AC

Symbol	Parameter	V <sub>CC</sub> (V) (Note 5)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
t <sub>PHL</sub>	Propagation Delay	3.3	0.5	8.5	10.5	2.5	11.0	ns
t <sub>PLH</sub>	D <sub>n</sub> to O <sub>n</sub>	5.0	1.5	5.5	7.0	1.5	7.5	
t <sub>PLH</sub>	Propagation Delay	3.3	2.5	8.5	12.0	2.5	12.5	ns
t <sub>PHL</sub>	LE to O <sub>n</sub>	5.0	2.0	6.0	8.0	2.0	8.5	
t <sub>PZL</sub>	Output Enable Time	3.3	2.5	8.5	13.0	2.5	13.5	ns
t <sub>PZH</sub>		5.0	1.5	6.0	8.5	1.5	9.0	
t <sub>PHZ</sub>	Output Disable Time	3.3	1.0	9.0	14.5	1.0	15.0	ns
t <sub>PLZ</sub>		5.0	1.0	6.0	9.5	1.0	10.0	

Note 5: Voltage Range 5.0 is 5.0V ± 0.5V  
Voltage Range 3.3 is 3.3V ± 0.3V

## AC Operating Requirements for AC

Symbol	Parameter	V <sub>CC</sub> (V) (Note 6)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Typ	Guaranteed Minimum	Typ	Guaranteed Minimum	
t <sub>S</sub>	Setup Time, HIGH or LOW D <sub>n</sub> to LE	3.3	0	3.0	3.0	ns	
		5.0	0	3.0	3.0		
t <sub>H</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to LE	3.3	0	1.5	1.5	ns	
		5.0	0	1.5	1.5		
t <sub>W</sub>	LE Pulse Width, HIGH	3.3	2.0	4.0	4.0	ns	
		5.0	2.0	4.0	4.0		

Note 6: Voltage Range 5.0 is 5.0V ± 0.5V  
Voltage Range 3.3 is 3.3V ± 0.3V

DC Electrical Characteristics for ACT								
Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits				
V <sub>IH</sub>	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	
		5.5	1.5	2.0	2.0			
V <sub>IL</sub>	Maximum LOW Level Input Voltage	4.5	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	
		5.5	1.5	0.8	0.8			
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4	V	I <sub>OUT</sub> = -50 μA	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -24 mA I <sub>OH</sub> = -24 mA (Note 7)	
		5.5		4.86	4.76			
V <sub>OL</sub>	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1	V	I <sub>OUT</sub> = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 24 mA (Note 7)	
		5.5		0.36	0.44			
I <sub>IN</sub>	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND	
I <sub>OZ</sub>	Maximum 3-STATE Leakage Current	5.5		±0.25	±2.5	μA	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> V <sub>O</sub> = V <sub>CC</sub> , GND	
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	5.5	0.6		1.5	mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1V	
I <sub>OLD</sub>	Minimum Dynamic	5.5			75	mA	V <sub>OLD</sub> = 1.65V Max	
I <sub>OHD</sub>	Output Current (Note 8)	5.5			-75	mA	V <sub>OHD</sub> = 3.85V Min	
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	

**Note 7:** All outputs loaded; thresholds on input associated with output under test.

**Note 8:** Maximum test duration 2.0 ms, one output loaded at a time.

### AC Electrical Characteristics for ACT

Symbol	Parameter	V <sub>CC</sub> (V) (Note 9)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay D <sub>n</sub> to O <sub>n</sub>	5.0	2.5	6.0	10.5	2.0	12.0	ns
t <sub>PHL</sub>	Propagation Delay LE to O <sub>n</sub>	5.0	3.0	6.0	10.5	2.5	12.0	ns
t <sub>PLH</sub>	Propagation Delay LE to O <sub>n</sub>	5.0	2.5	5.5	9.5	2.0	10.5	ns
t <sub>PZH</sub>	Output Enable Time	5.0	2.0	5.5	10.0	1.5	11.0	ns
t <sub>PZL</sub>	Output Enable Time	5.0	1.5	5.5	9.5	1.5	10.5	ns
t <sub>PHZ</sub>	Output Disable Time	5.0	2.5	6.5	11.0	1.5	12.5	ns
t <sub>PLZ</sub>	Output Disable Time	5.0	1.5	5.0	8.5	1.0	9.5	ns

**Note 9:** Voltage Range 5.0 is 5.0V ± 0.5V

### AC Operating Requirements for ACT

Symbol	Parameter	V <sub>CC</sub> (V) (Note 10)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C	Units
			Typ	Guaranteed Minimum		
t <sub>S</sub>	Setup Time, HIGH or LOW D <sub>n</sub> to LE	5.0	1.5	3.0	3.5	ns
t <sub>H</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to LE	5.0	-1.5	0	0	ns
t <sub>W</sub>	LE Pulse Width, HIGH	5.0	2.0	3.5	4.0	ns

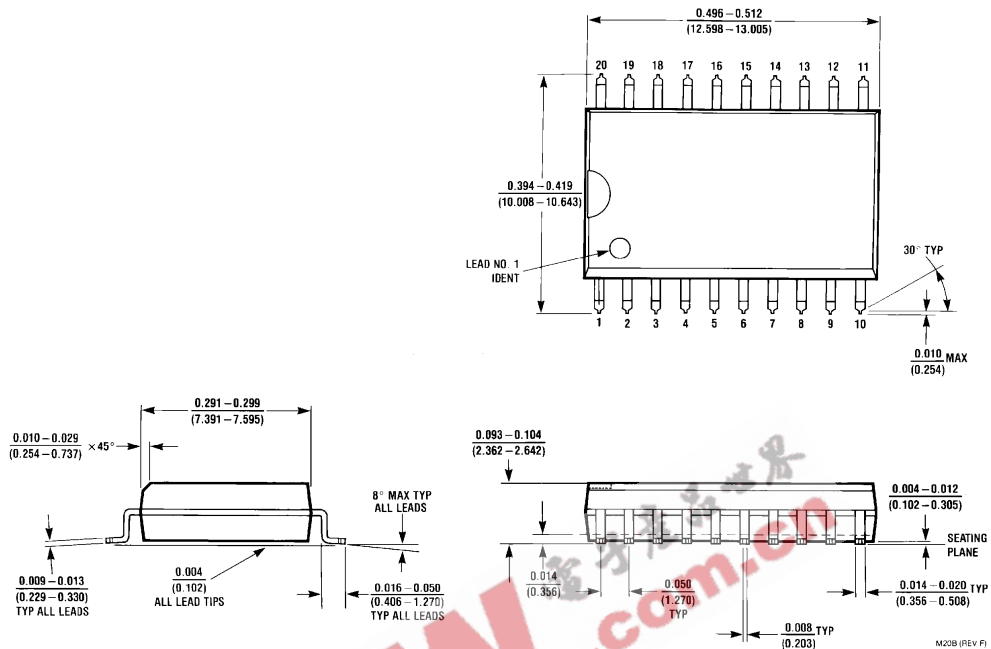
Note 10: Voltage Range 5.0 is 5.0V ± 0.5V

### Capacitance

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	5.0	pF	V <sub>CC</sub> = OPEN
C <sub>PD</sub>	Power Dissipation Capacitance for AC for ACT	25.0	pF	V <sub>CC</sub> = 5.0V
		42.0		

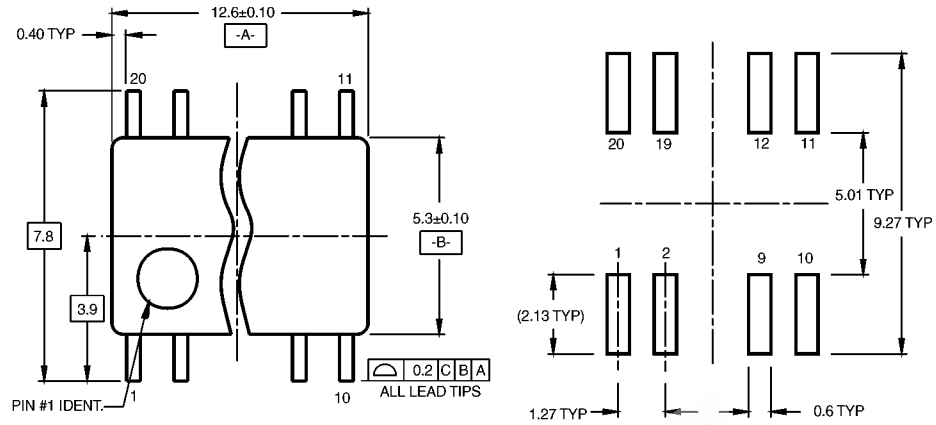
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**Physical Dimensions** inches (millimeters) unless otherwise noted

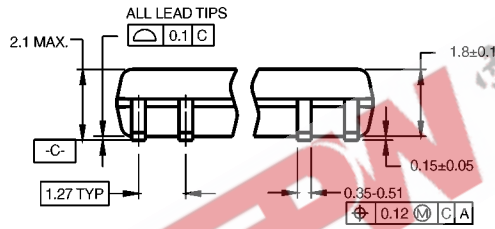


**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body  
Package Number M20B**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



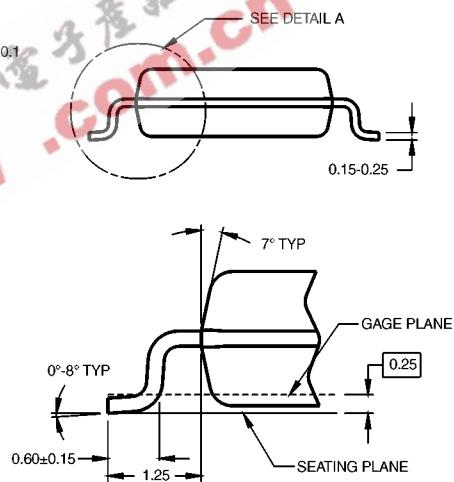
LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS

- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

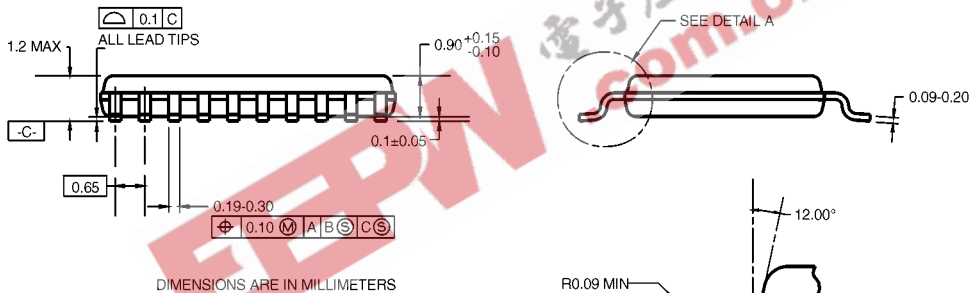
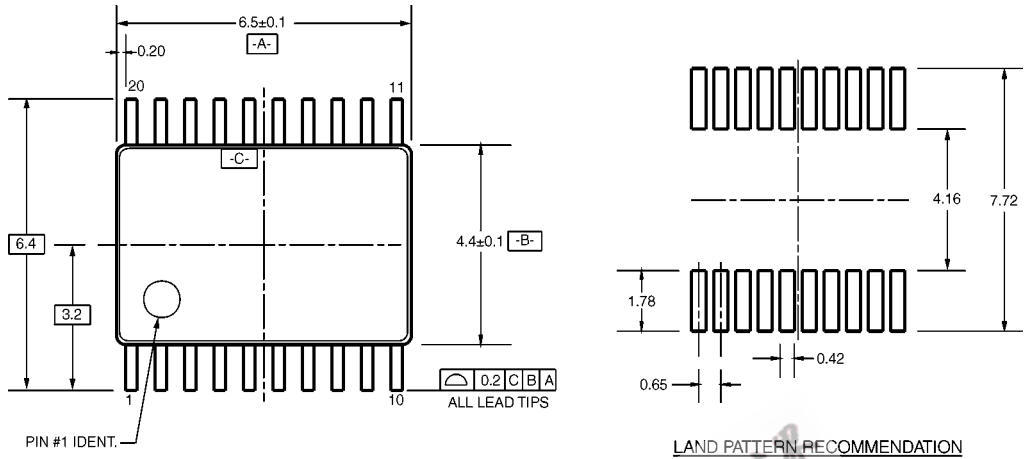


DETAIL A

**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M20D**



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

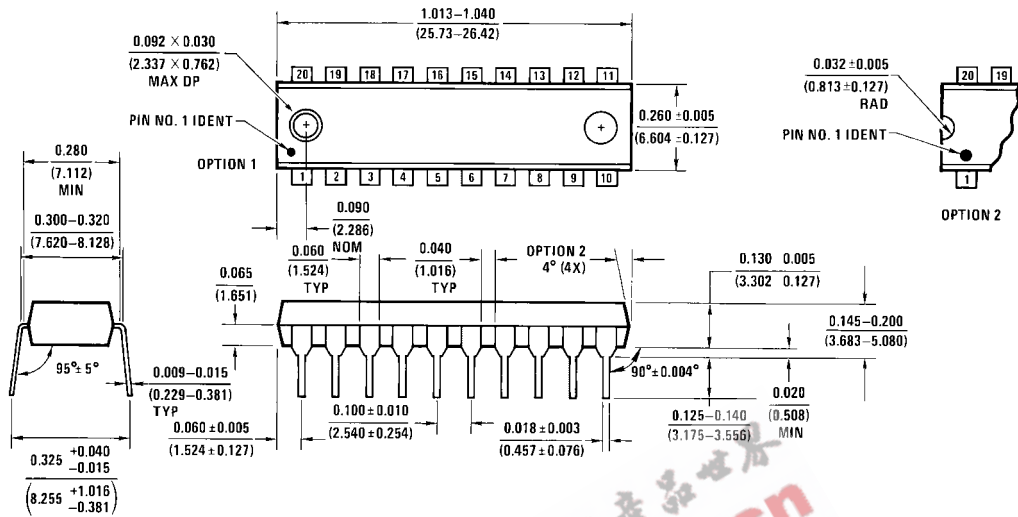


- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
  - D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20RevD1

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC20**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide  
Package Number N20A

N20A (REV G)

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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