74LVC1G125

Bus buffer/line driver; 3-state

Rev. 07 — 30 August 2007 Product data sheet

1. General description

The 74LVC1G125 provides one non-inverting buffer/line driver with 3-state output. The 3-state output is controlled by the output enable input ($\overline{OE}$). A HIGH-level at pin $\overline{OE}$ causes the output to assume a high-impedance OFF-state.

The input can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features

- Wide supply voltage range from 1.65 V to 5.5 V
- High noise immunity
- ±24 mA output drive (V_{CC} = 3.0 V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from –40 °C to +85 °C and –40 °C to +125 °C
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8-B/JESD36 (2.7 V to 3.6 V)

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC1G125GW	–40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74LVC1G125GV	–40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753
74LVC1G125GM	–40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886
74LVC1G125GF	–40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1 × 0.5 mm	SOT891

4. Marking

Table 2. Marking

Type number	Marking code
74LVC1G125GW	VM
74LVC1G125GV	V25
74LVC1G125GM	VM
74LVC1G125GF	VM

5. Functional diagram

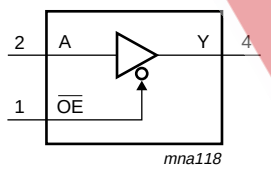


Fig 1. Logic symbol

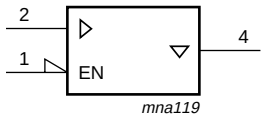


Fig 2. IEC logic symbol

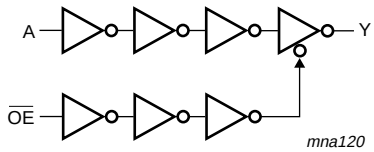


Fig 3. Logic diagram

6. Pinning information

6.1 Pinning

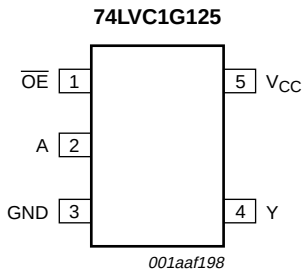


Fig 4. Pin configuration SOT353-1 and SOT753

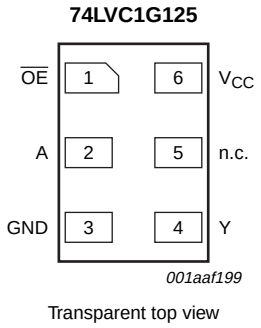


Fig 5. Pin configuration SOT886

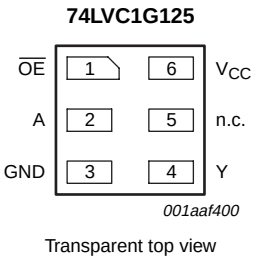


Fig 6. Pin configuration SOT891

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT353-1/SOT753	SOT886/SOT891	
$\overline{OE}$	1	1	output enable input
A	2	2	data input
GND	3	3	ground (0 V)
Y	4	4	data output
n.c.	-	5	not connected
V_{CC}	5	6	supply voltage

7. Functional description

Table 4. Function table[1]

Input		Output
$\overline{OE}$	A	Y
L	L	L
L	H	H
H	X	Z

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
Z = high-impedance OFF-state.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		–50	-	mA
V_I	input voltage		[1]	–0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	Active mode	[1][2]	–0.5	V_{CC} + 0.5	V
		Power-down mode	[1][2]	–0.5	+6.5	V
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			–100	-	mA
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[3]	-	250	mW
T_{stg}	storage temperature			–65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When V_{CC} = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.

[3] For TSSOP5 and SC-74A packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.
For XSON6 packages: above 45 °C the value of P_{tot} derates linearly with 2.4 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	Active mode	0	-	V_{CC}	V
		V_{CC} = 0 V; Power-down mode	0	-	5.5	V
T_{amb}	ambient temperature		–40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	-	-	20	ns/V
		V_{CC} = 2.7 V to 5.5 V	-	-	10	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{amb} = −40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 1.95 V	-	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	0.3 × V_{CC}	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 1.65 V to 5.5 V; I_O = 100 µA	-	-	0.1	V
		V_{CC} = 1.65 V; I_O = 4 mA	-	-	0.45	V
		V_{CC} = 2.3 V; I_O = 8 mA	-	-	0.3	V
		V_{CC} = 2.7 V; I_O = 12 mA	-	-	0.4	V
		V_{CC} = 3.0 V; I_O = 24 mA	-	-	0.55	V
		V_{CC} = 4.5 V; I_O = 32 mA	-	-	0.55	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 1.65 V to 5.5 V; I_O = −100 µA	V_{CC} − 0.1	-	-	V
		V_{CC} = 1.65 V; I_O = −4 mA	1.2	-	-	V
		V_{CC} = 2.3 V; I_O = −8 mA	1.9	-	-	V
		V_{CC} = 2.7 V; I_O = −12 mA	2.2	-	-	V
		V_{CC} = 3.0 V; I_O = −24 mA	2.7	-	-	V
		V_{CC} = 4.5 V; I_O = −32 mA	3.8	-	-	V
I_I	input leakage current	V_{CC} = 0 V to 5.5 V; V_I = 5.5 V or GND	-	±0.1	±5	µA
I_{OZ}	OFF-state output current	V_{CC} = 3.6 V; V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND	-	±0.1	±10	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 5.5 V	-	±0.1	±10	µA
I_{CC}	supply current	V_I = 5.5 V or GND; V_{CC} = 1.65 V to 5.5 V; I_O = 0 A	-	0.1	10	µA
ΔI_{CC}	additional supply current	per pin; V_{CC} = 2.3 V to 5.5 V; V_I = V_{CC} − 0.6 V; I_O = 0 A	-	5	500	µA
C_I	input capacitance		-	5	-	pF

Table 7. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{amb} = −40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 1.95 V	-	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	0.3 × V_{CC}	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 1.65 V to 5.5 V; I_O = 100 µA	-	-	0.1	V
		V_{CC} = 1.65 V; I_O = 4 mA	-	-	0.70	V
		V_{CC} = 2.3 V; I_O = 8 mA	-	-	0.45	V
		V_{CC} = 2.7 V; I_O = 12 mA	-	-	0.60	V
		V_{CC} = 3.0 V; I_O = 24 mA	-	-	0.80	V
		V_{CC} = 4.5 V; I_O = 32 mA	-	-	0.80	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 1.65 V to 5.5 V; I_O = −100 µA	V_{CC} − 0.1	-	-	V
		V_{CC} = 1.65 V; I_O = −4 mA	0.95	-	-	V
		V_{CC} = 2.3 V; I_O = −8 mA	1.7	-	-	V
		V_{CC} = 2.7 V; I_O = −12 mA	1.9	-	-	V
		V_{CC} = 3.0 V; I_O = −24 mA	2.0	-	-	V
		V_{CC} = 4.5 V; I_O = −32 mA	3.4	-	-	V
I_I	input leakage current	V_{CC} = 0 V to 5.5 V; V_I = 5.5 V or GND	-	-	±100	µA
I_{OZ}	OFF-state output current	V_{CC} = 3.6 V; V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND	-	-	±200	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 5.5 V	-	-	±200	µA
I_{CC}	supply current	V_I = 5.5 V or GND; V_{CC} = 1.65 V to 5.5 V; I_O = 0 A	-	-	200	µA
ΔI_{CC}	additional supply current	per pin; V_{CC} = 2.3 V to 5.5 V; V_I = V_{CC} − 0.6 V; I_O = 0 A	-	-	5000	µA

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 9.

Symbol	Parameter	Conditions		–40 °C to +85 °C			–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	A to Y; see Figure 7	[2]						
		V_{CC} = 1.65 V to 1.95 V		1.0	3.3	8.0	1.0	10.5	ns
		V_{CC} = 2.3 V to 2.7 V		0.5	2.2	5.5	0.5	7	ns
		V_{CC} = 2.7 V		0.5	2.5	5.5	0.5	7	ns
		V_{CC} = 3.0 V to 3.6 V		0.5	2.1	4.5	0.5	6	ns
		V_{CC} = 4.5 V to 5.5 V		0.5	1.7	4.0	0.5	5.5	ns
t_{en}	enable time	$\overline{OE}$ to Y; see Figure 8	[3]						
		V_{CC} = 1.65 V to 1.95 V		1.0	4.1	9.4	1.0	12	ns
		V_{CC} = 2.3 V to 2.7 V		0.5	2.8	6.6	0.5	8.5	ns
		V_{CC} = 2.7 V		0.5	3.3	6.6	0.5	8.5	ns
		V_{CC} = 3.0 V to 3.6 V		0.5	2.4	5.3	0.5	7	ns
		V_{CC} = 4.5 V to 5.5 V		0.5	2.1	5.0	0.5	6.5	ns
t_{dis}	disable time	$\overline{OE}$ to Y; see Figure 8	[4]						
		V_{CC} = 1.65 V to 1.95 V		1.0	4.3	9.2	1.0	12	ns
		V_{CC} = 2.3 V to 2.7 V		0.5	2.7	5.0	0.5	6.5	ns
		V_{CC} = 2.7 V		0.5	3.0	5.0	0.5	6.5	ns
		V_{CC} = 3.0 V to 3.6 V		0.5	3.1	5.0	0.5	6.5	ns
		V_{CC} = 4.5 V to 5.5 V		0.5	2.2	4.2	0.5	5.5	ns
C_{PD}	power dissipation capacitance	per buffer; V_I = GND to V_{CC}	[5]						
		output enabled		-	25	-	-	-	pF
		output disabled		-	6	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

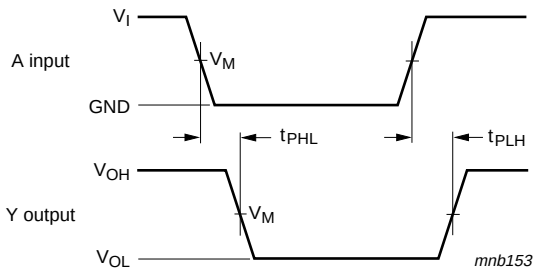
[2] t_{pd} is the same as t_{PLH} and t_{PHL}

[3] t_{en} is the same as t_{PZH} and t_{PZL}

[4] t_{dis} is the same as t_{PLZ} and t_{PHZ}

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

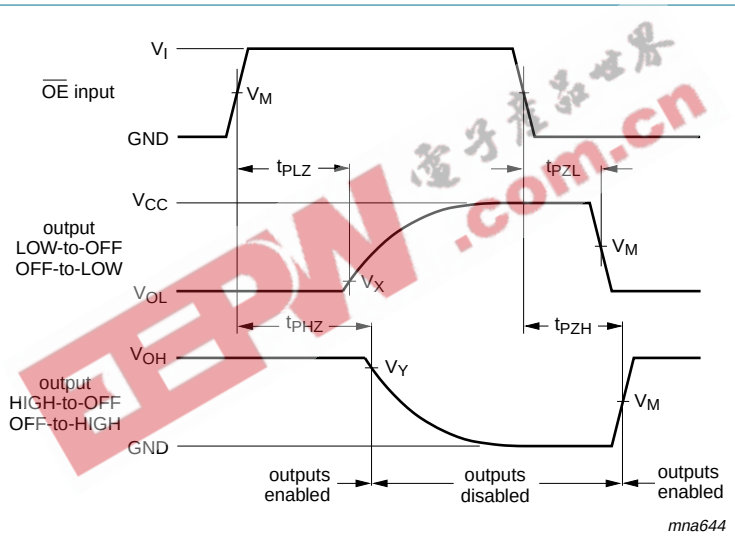
12. Waveforms



Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. Input A to output Y propagation delay times



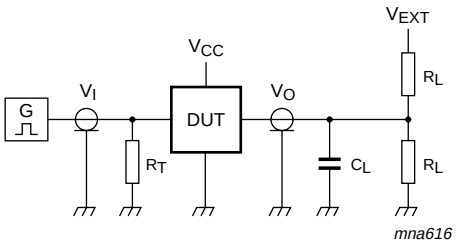
Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 8. 3-state enable and disable times

Table 9. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
1.65 V to 1.95 V	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.15 V	V_{OH} − 0.15 V
2.3 V to 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.15 V	V_{OH} − 0.15 V
2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V
3.0 V to 3.6 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V
4.5 V to 5.5 V	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.3 V	V_{OH} − 0.3 V



Test data is given in Table 10.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

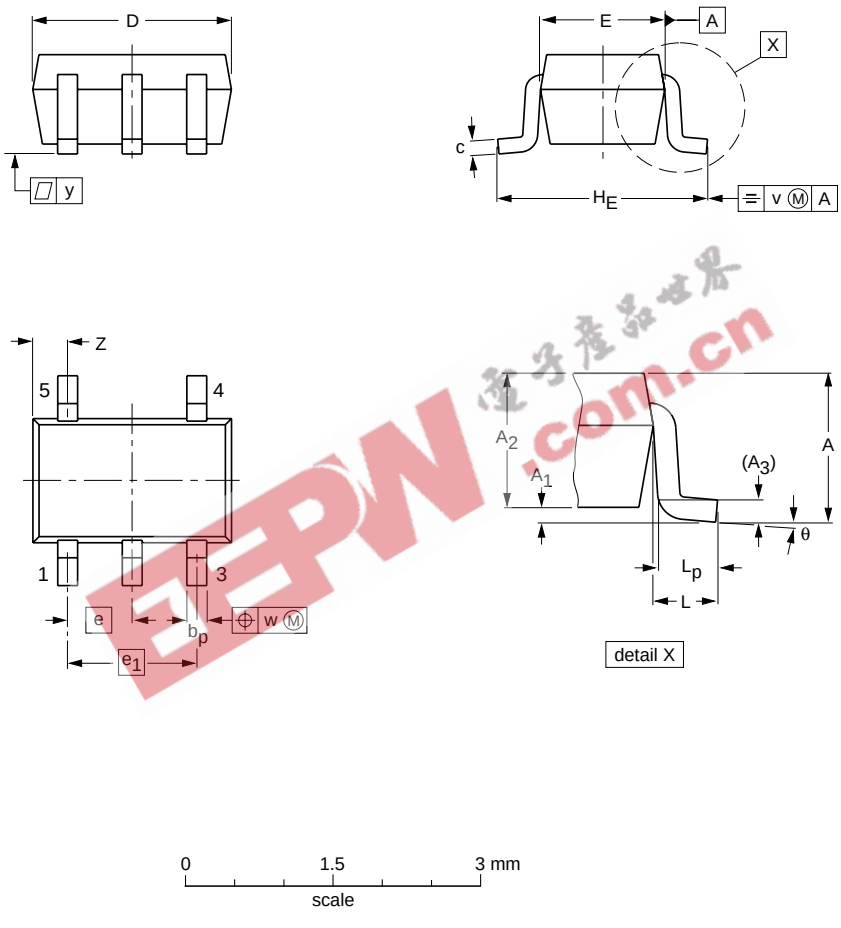
Fig 9. Load circuitry for switching times

Table 10. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 kΩ	open	GND	$2V_{CC}$
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	GND	$2V_{CC}$
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2V_{CC}$

13. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm **SOT353-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	e_1	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.1 0	1.0 0.8	0.15	0.30 0.15	0.25 0.08	2.25 1.85	1.35 1.15	0.65	1.3	2.25 2.0	0.425	0.46 0.21	0.3	0.1	0.1	0.60 0.15	7° 0°

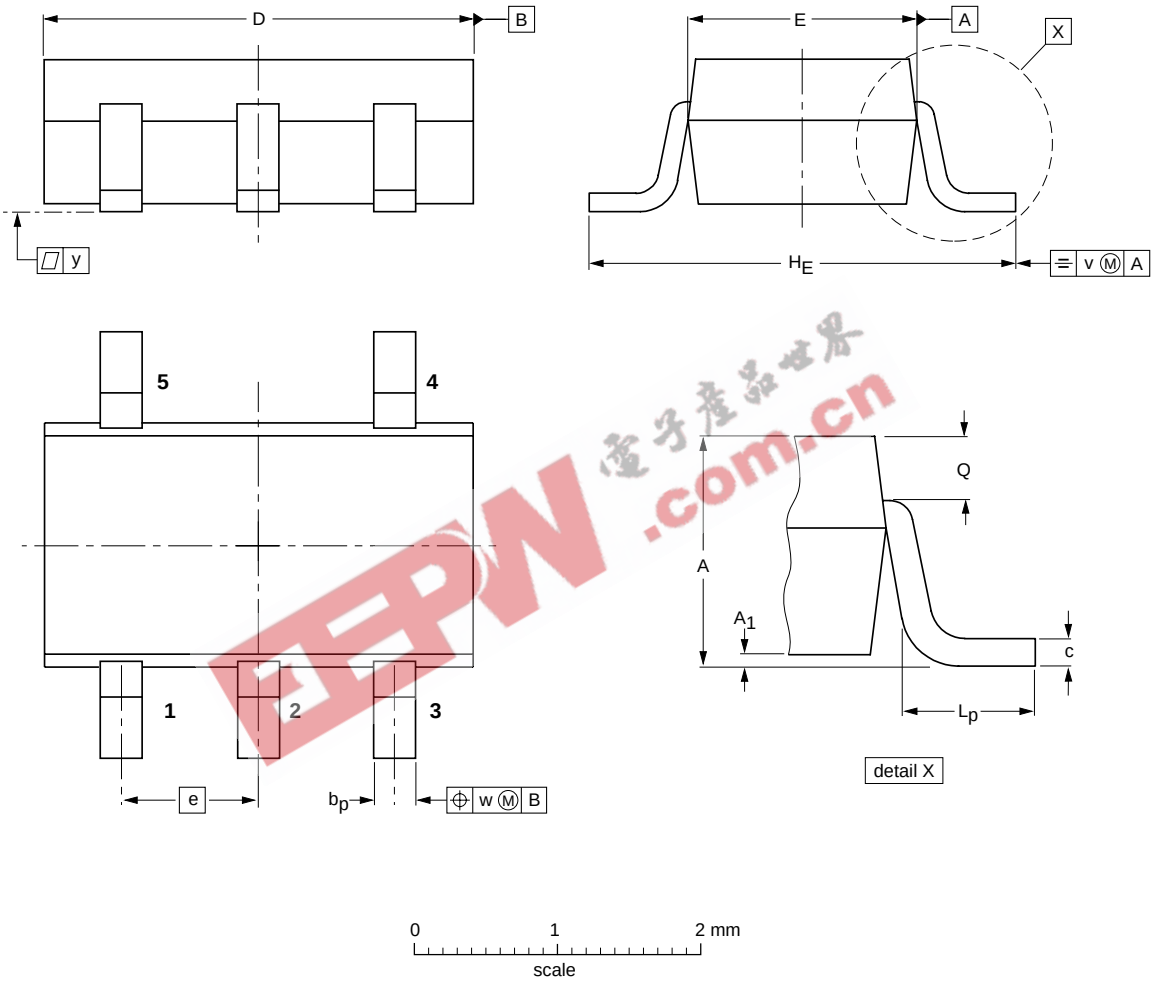
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT353-1		MO-203	SC-88A			~~00-09-01~~ 03-02-19

Fig 10. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads **SOT753**



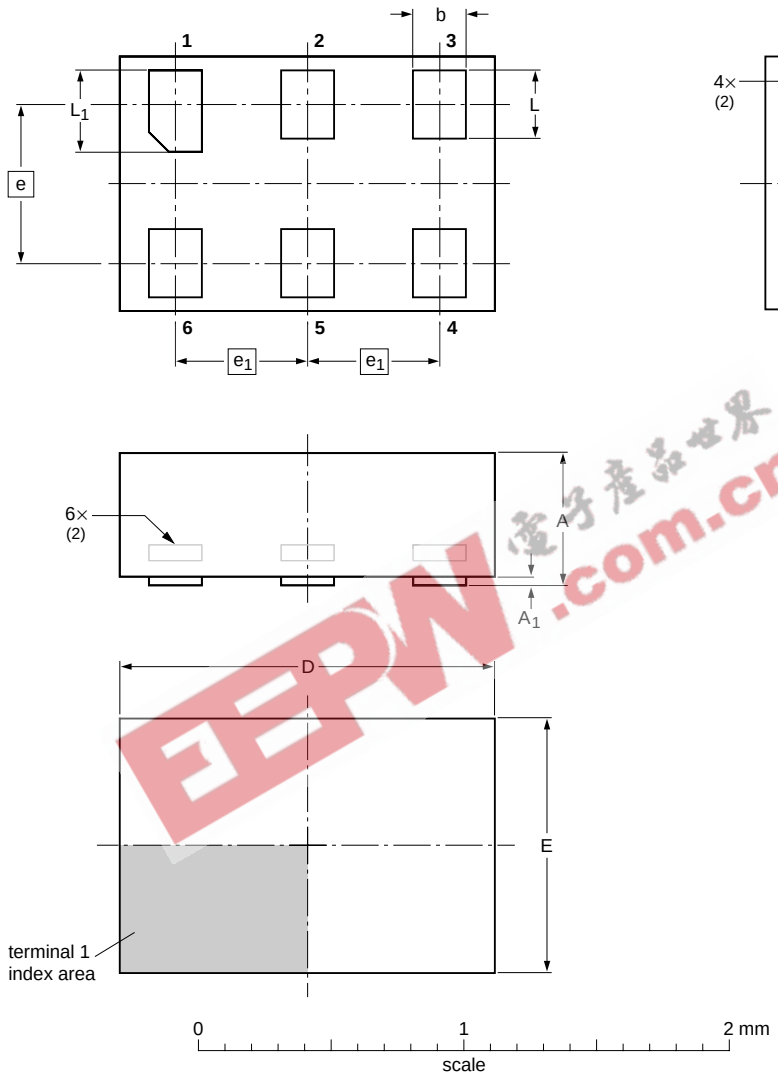
DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.100 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT753			SC-74A			~~02-04-16~~ 06-03-16

Fig 11. Package outline SOT753

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm **SOT886**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A1 max	b	D	E	e	e1	L	L1
mm	0.5	0.04	0.25 0.17	1.5 1.4	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

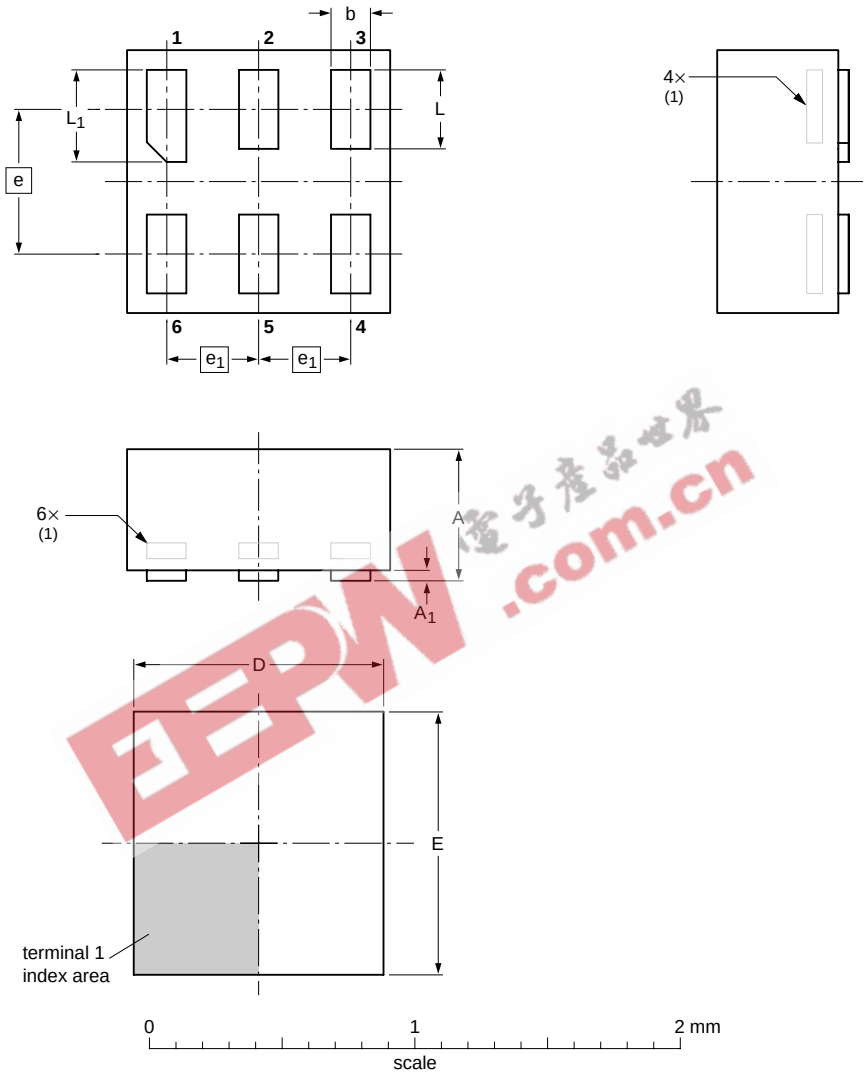
Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT886		MO-252				~~04-07-15~~ 04-07-22

Fig 12. Package outline SOT886 (XSON6)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1 x 0.5 mm **SOT891**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1 max	b	D	E	e	e_1	L	L_1
mm	0.5	0.04	0.20 0.12	1.05 0.95	1.05 0.95	0.55	0.35	0.35 0.27	0.40 0.32

Note

1. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT891						~~05-04-06~~ 07-05-15

Fig 13. Package outline SOT891 (XSON6)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G125_7	20070830	Product data sheet	-	74LVC1G125_6
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • In Section 10 “Static characteristics”, changed conditions for input leakage and supply current. • Figure 13 “Package outline SOT891 (XSON6)” updated.			
74LVC1G125_6	20060912	Product data sheet	-	74LVC1G125_5
74LVC1G125_5	20040915	Product specification	-	74LVC1G125_4
74LVC1G125_4	20021118	Product specification	-	74LVC1G125_3
74LVC1G125_3	20020528	Product specification	-	74LVC1G125_2
74LVC1G125_2	20010406	Product specification	-	74LVC1G125_1
74LVC1G125_1	20001222	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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