

74LVT16244B; 74LVTH16244B

3.3 V 16-bit buffer/driver; 3-state

Rev. 05 — 21 March 2006

Product data sheet

1. General description

The 74LVT16244B; 74LVTH16244B is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V.

This device is a 16-bit buffer and line driver featuring non-inverting 3-state bus outputs. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer.

2. Features

- 16-bit bus interface
- 3-state buffers
- Output capability: +64 mA and -32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Power-up 3-state
- Live insertion and extraction permitted
- No bus current loading when output is tied to 5 V bus
- Latch-up protection:
 - ◆ JESD78: exceeds 500 mA
- ESD protection:
 - ◆ MIL STD 883C method 3015: exceeds 2000 V
 - ◆ Machine model: exceeds 200 V

3. Quick reference data

Table 1. Quick reference data

$GND = 0 V$; $T_{amb} = 25 ^\circ C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	LOW-to-HIGH propagation delay nAn to nYn	$C_L = 50 \text{ pF}$; $V_{CC} = 3.3 \text{ V}$	-	1.8	-	ns
t_{PHL}	HIGH-to-LOW propagation delay nAn to nYn	$C_L = 50 \text{ pF}$; $V_{CC} = 3.3 \text{ V}$	-	1.7	-	ns
C_i	input capacitance	$V_I = 0 \text{ V}$ or 3.0 V	-	3	-	pF
C_o	output capacitance	outputs disabled; $V_O = 0 \text{ V}$ or 3.0 V	-	9	-	pF
I_{CC}	quiescent supply current	outputs disabled; $V_{CC} = 3.6 \text{ V}$; $I_O = 0 \text{ A}$; $V_I = GND$ or V_{CC}	-	70	-	μA

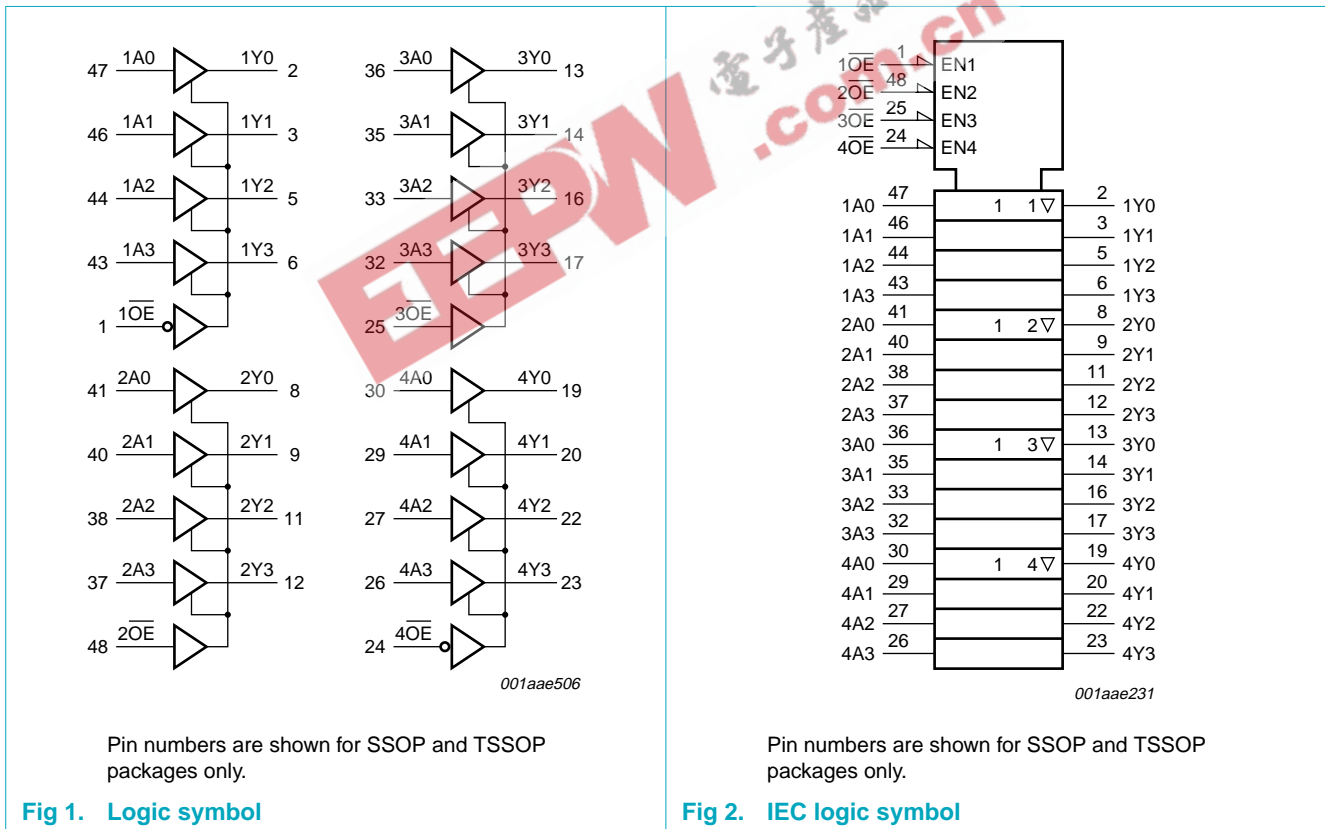
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4. Ordering information

Table 2. Ordering information

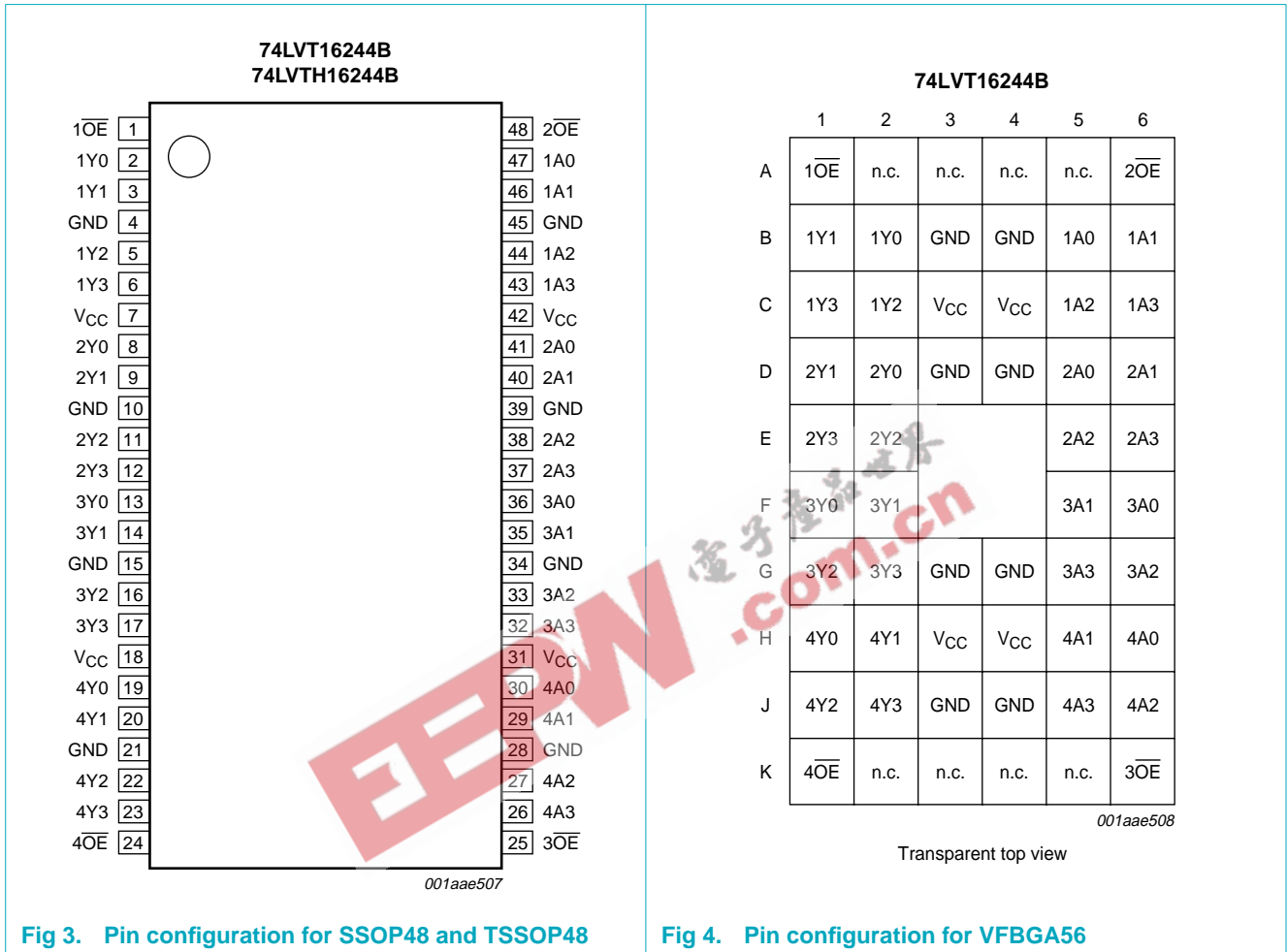
Type number	Package			Version
	Temperature range	Name	Description	
74LVT16244BDL	-40 °C to +85 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1
74LVT16244BDGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74LVT16244BEV	-40 °C to +85 °C	VFBGA56	plastic very thin fine-pitch ball grid array package; 56 balls; body 4.5 × 7 × 0.65 mm	SOT702-1
74LVTH16244BDL	-40 °C to +85 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1
74LVTH16244BDGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

5. Functional diagram



6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	(T)SSOP48	VFBGA56	
1OE	1	A1	output enable input 1OE
n.c.	-	A2, A3, A4, A5	not connected
1Y0	2	B2	data output 1Y0
1Y1	3	B1	data output 1Y1
GND	4	B3	ground (0 V)
1Y2	5	C2	data output 1Y2
1Y3	6	C1	data output 1Y3
VCC	7	C3	supply voltage
2Y0	8	D2	data output 2Y0

Table 3. Pin description ...continued

Symbol	Pin		Description
	(T)SSOP48	VFBGA56	
2Y1	9	D1	data output 2Y1
GND	10	D3	ground (0 V)
2Y2	11	E2	data output 2Y2
2Y3	12	E1	data output 2Y3
3Y0	13	F1	data output 3Y0
3Y1	14	F2	data output 3Y1
GND	15	G3	ground (0 V)
3Y2	16	G1	data output 3Y2
3Y3	17	G2	data output 3Y3
V _{CC}	18	H3	supply voltage
4Y0	19	H1	data output 4Y0
4Y1	20	H2	data output 4Y1
GND	21	J3	ground (0 V)
4Y2	22	J1	data output 4Y2
4Y3	23	J2	data output 4Y3
4 \overline{OE}	24	K1	output enable input 4 \overline{OE}
n.c.	-	K2, K3, K4, K5	not connected
3 \overline{OE}	25	K6	output enable input 3 \overline{OE}
4A3	26	J5	data input 4A3
4A2	27	J6	data input 4A2
GND	28	J4	ground (0 V)
4A1	29	H5	data input 4A1
4A0	30	H6	data input 4A0
V _{CC}	31	H4	supply voltage
3A3	32	G5	data input 3A3
3A2	33	G6	data input 3A2
GND	34	G4	ground (0 V)
3A1	35	F5	data input 3A1
3A0	36	F6	data input 3A0
2A3	37	E6	data input 2A3
2A2	38	E5	data input 2A2
GND	39	D4	ground (0 V)
2A1	40	D6	data input 2A1
2A0	41	D5	data input 2A0
V _{CC}	42	C4	supply voltage
1A3	43	C6	data input 1A3
1A2	44	C5	data input 1A2
GND	45	B4	ground (0 V)

Table 3. Pin description ...continued

Symbol	Pin		Description
	(T)SSOP48	VFBGA56	
1A1	46	B6	data input 1A1
1A0	47	B5	data input 1A0
$\overline{2OE}$	48	A6	output enable input $\overline{2OE}$

7. Functional description

7.1 Function table

Table 4. Function table^[1]

Control	Input	Output
\overline{nOE}	nAn	nYn
L	L	L
	H	H
H	X	Z

- [1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
Z = high-impedance OFF-state.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
V_I	input voltage		^[1] -0.5	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state	^[1] -0.5	+7.0	V
I_{IK}	input clamping current	$V_I < 0$ V	-	-50	mA
I_{OK}	output clamping current	$V_O < 0$ V	-	-50	mA
I_O	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-	-64	mA
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		^[2] -	150	°C

- [1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
- [2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.7	-	3.6	V
V_I	input voltage		0	-	5.5	V
V_{IH}	HIGH-state input voltage		2.0	-	-	V
V_{IL}	LOW-state input voltage		-	-	0.8	V
I_{OH}	HIGH-state output current		-	-	-32	mA
I_{OL}	LOW-state output current	none	-	-	32	mA
		current duty cycle $\leq 50\%$; $f_i \geq 1$ kHz	-	-	64	mA
T_{amb}	ambient temperature	in free-air	-40	-	+85	$^{\circ}\text{C}$
$\Delta t/\Delta V$	input transition rise and fall rate	outputs enabled	-	-	10	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ [1]							
V_{IK}	input clamping voltage	$V_{CC} = 2.7\text{ V}$; $I_{IK} = -18\text{ mA}$	-	-0.85	-1.2	V	
V_{OH}	HIGH-state output voltage	$I_{OH} = -100\text{ }\mu\text{A}$; $V_{CC} = 2.7\text{ V}$ to 3.6 V	$V_{CC} - 0.2$	V_{CC}	-	V	
		$I_{OH} = -8\text{ mA}$; $V_{CC} = 2.7\text{ V}$	2.4	2.5	-	V	
		$I_{OH} = -32\text{ mA}$; $V_{CC} = 3.0\text{ V}$	2.0	2.3	-	V	
V_{OL}	LOW-state output voltage	$V_{CC} = 2.7\text{ V}$					
		$I_{OL} = 100\text{ }\mu\text{A}$	-	0.07	0.2	V	
		$I_{OL} = 24\text{ mA}$	-	0.3	0.5	V	
		$V_{CC} = 3.0\text{ V}$					
		$I_{OL} = 16\text{ mA}$	-	0.25	0.4	V	
		$I_{OL} = 32\text{ mA}$	-	0.3	0.5	V	
I_{LI}	input leakage current	$I_{OL} = 64\text{ mA}$	-	0.4	0.55	V	
		all input pins	$V_{CC} = 0\text{ V}$ or 3.6 V ; $V_I = 5.5\text{ V}$	-	0.4	10	μA
		control pins	$V_{CC} = 3.6\text{ V}$; $V_I = V_{CC}$ or GND	-	0.1	± 1.0	μA
		data pins	$V_{CC} = 3.6\text{ V}$	[2]			
			$V_I = V_{CC}$	-	0.1	1	μA
	$V_I = 0\text{ V}$	-	-0.4	-5	μA		
I_{OFF}	power-off leakage current	$V_{CC} = 0\text{ V}$; V_I or $V_O = 0\text{ V}$ to 4.5 V	-	0.1	± 100	μA	

Table 7. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
I _{HOLD}	bus hold current data input	V _{CC} = 3 V	[3]				
		V _I = 0.8 V	75	135	-	μA	
		V _I = 2.0 V	-75	-135	-	μA	
		V _{CC} = 0 V to 3.6 V					
		V _I = 3.6 V	±500	-	-	μA	
I _{EX}	external current into output	output in HIGH-state when V _O > V _{CC} ; V _O = 5.5 V; V _{CC} = 3.0 V	-	50	125	μA	
I _{O(pu/pd)}	power-up/power-down output current	V _{CC} ≤ 1.2 V; V _O = 0.5 V to V _{CC} ; V _I = GND or V _{CC} ; nOE = don't care	[4]	1	±100	μA	
I _{OZ}	OFF-state output current	V _{CC} = 3.6 V; V _I = V _{IH} or V _{IL}					
		output HIGH: V _O = 3.0 V	-	0.5	5	μA	
		output LOW: V _O = 0.5 V	-	+0.5	-5	μA	
I _{CC}	quiescent supply current	V _{CC} = 3.6 V; V _I = GND or V _{CC} ; I _O = 0 A					
		output HIGH		0.07	0.12	mA	
		output LOW		-	4.0	6.0	mA
		outputs disabled	[5]	0.07	0.12	mA	
ΔI _{CC}	additional quiescent supply current	per input pin; V _{CC} = 3.0 V to 3.6 V; one input at V _{CC} - 0.6 V and other inputs at V _{CC} or GND	[6]	0.1	0.2	mA	
C _i	input capacitance	V _I = 0 V or 3.0 V	-	3	-	pF	
C _o	output capacitance	outputs disabled; V _O = 0 V or 3.0 V	-	9	-	pF	

[1] Typical values are measured at V_{CC} = 3.3 V and at T_{amb} = 25 °C.[2] Unused pins at V_{CC} or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 μs is permitted. This parameter is valid for T_{amb} = 25 °C only.[5] I_{CC} is measured with outputs pulled to V_{CC} or GND.[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

11. Dynamic characteristics

Table 8. Dynamic characteristicsVoltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T _{amb} = -40 °C to +85 °C [1]						
t _{PLH}	LOW-to-HIGH propagation delay nAn to nYn	see Figure 5				
		V _{CC} = 2.7 V	-	-	4.0	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	1.8	3.2	ns
t _{PHL}	HIGH-to-LOW propagation delay nAn to nYn	see Figure 5				
		V _{CC} = 2.7 V	-	-	4.0	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	1.7	3.2	ns

Table 8. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t _{PZH}	output enable time to HIGH-level	see Figure 6				
		V _{CC} = 2.7 V	-	-	5.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.3	4.0	ns
t _{PZL}	output enable time to LOW-level	see Figure 6				
		V _{CC} = 2.7 V	-	-	5.3	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.1	4.0	ns
t _{PHZ}	output disable time from HIGH-level	see Figure 6				
		V _{CC} = 2.7 V	-	-	5.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	3.2	4.5	ns
t _{PLZ}	output disable time from LOW-level	see Figure 6				
		V _{CC} = 2.7 V	-	-	4.4	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.9	4.0	ns

[1] Typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

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12. Waveforms

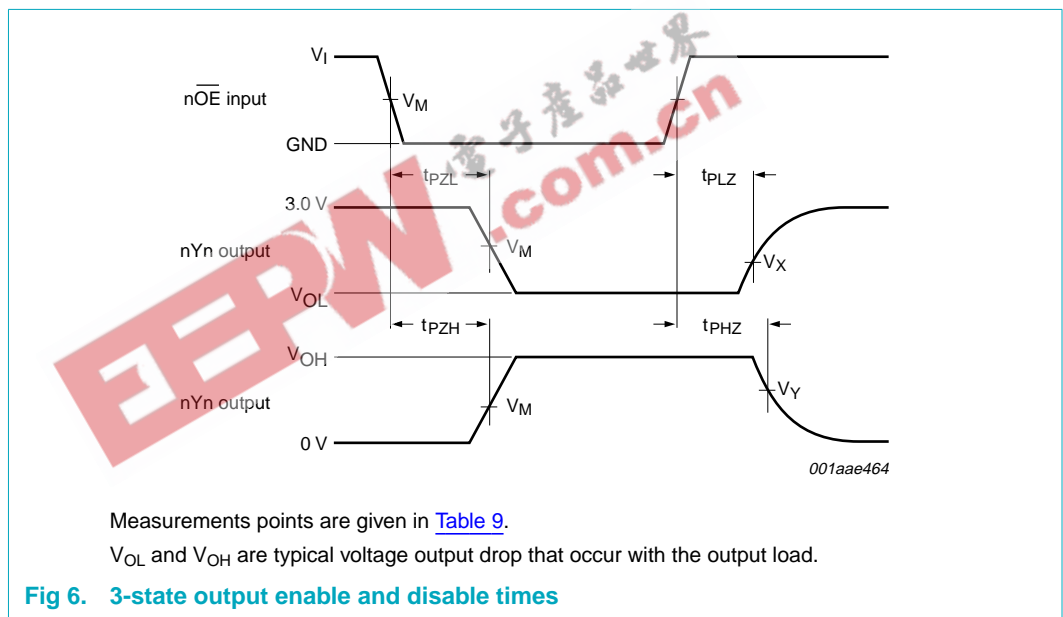
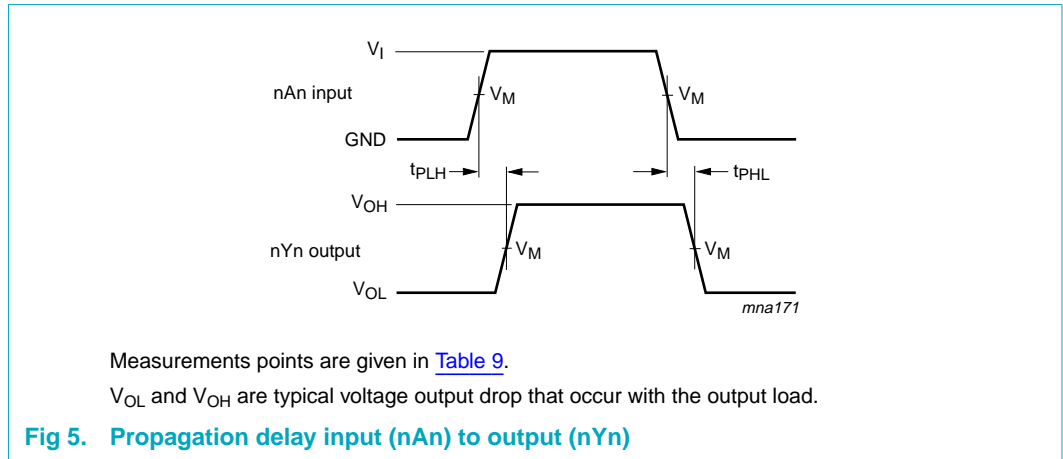


Table 9. Measurement points

Input	Output		
V_M	V_M	V_X	V_Y
1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$

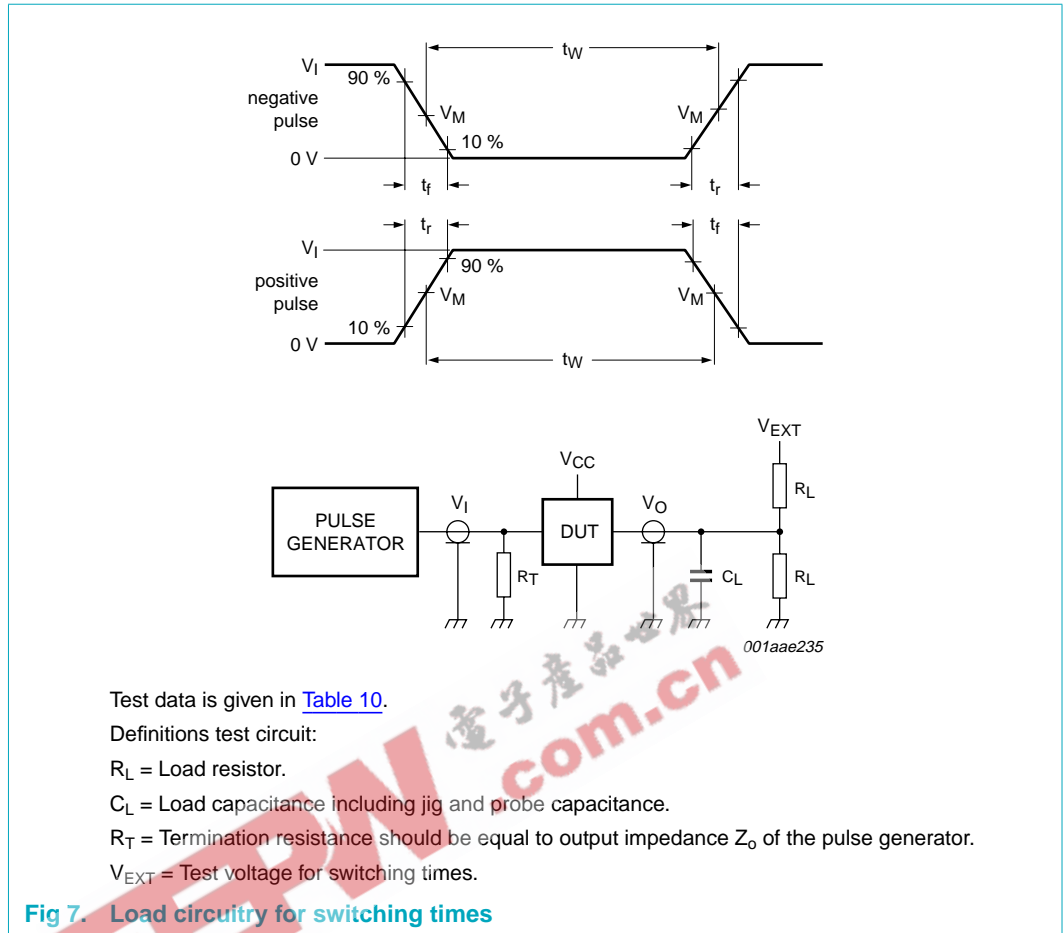


Table 10. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_w	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	GND	6 V	open

13. Package outline

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1

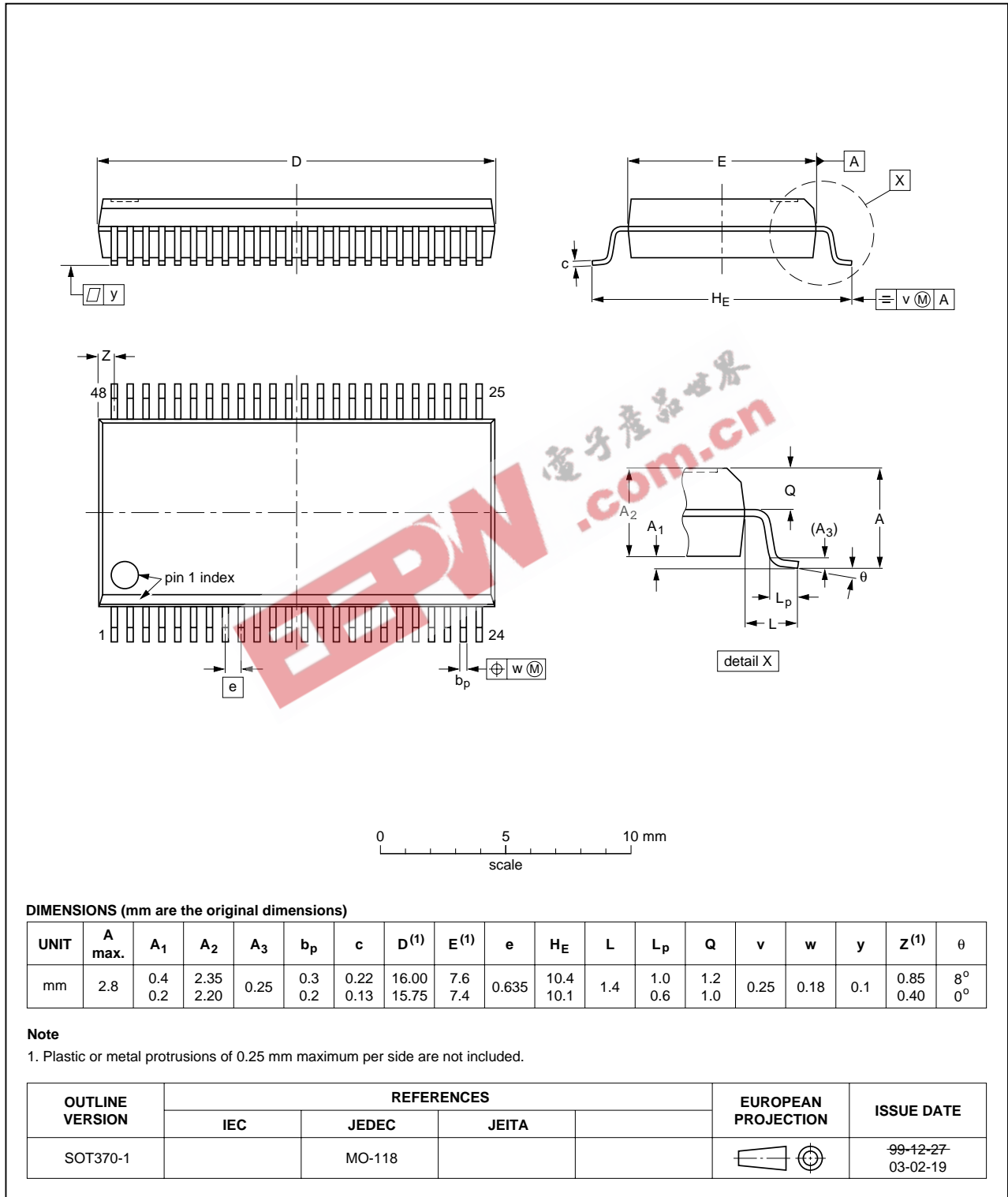


Fig 8. Package outline SOT370-1 (SSOP48)

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

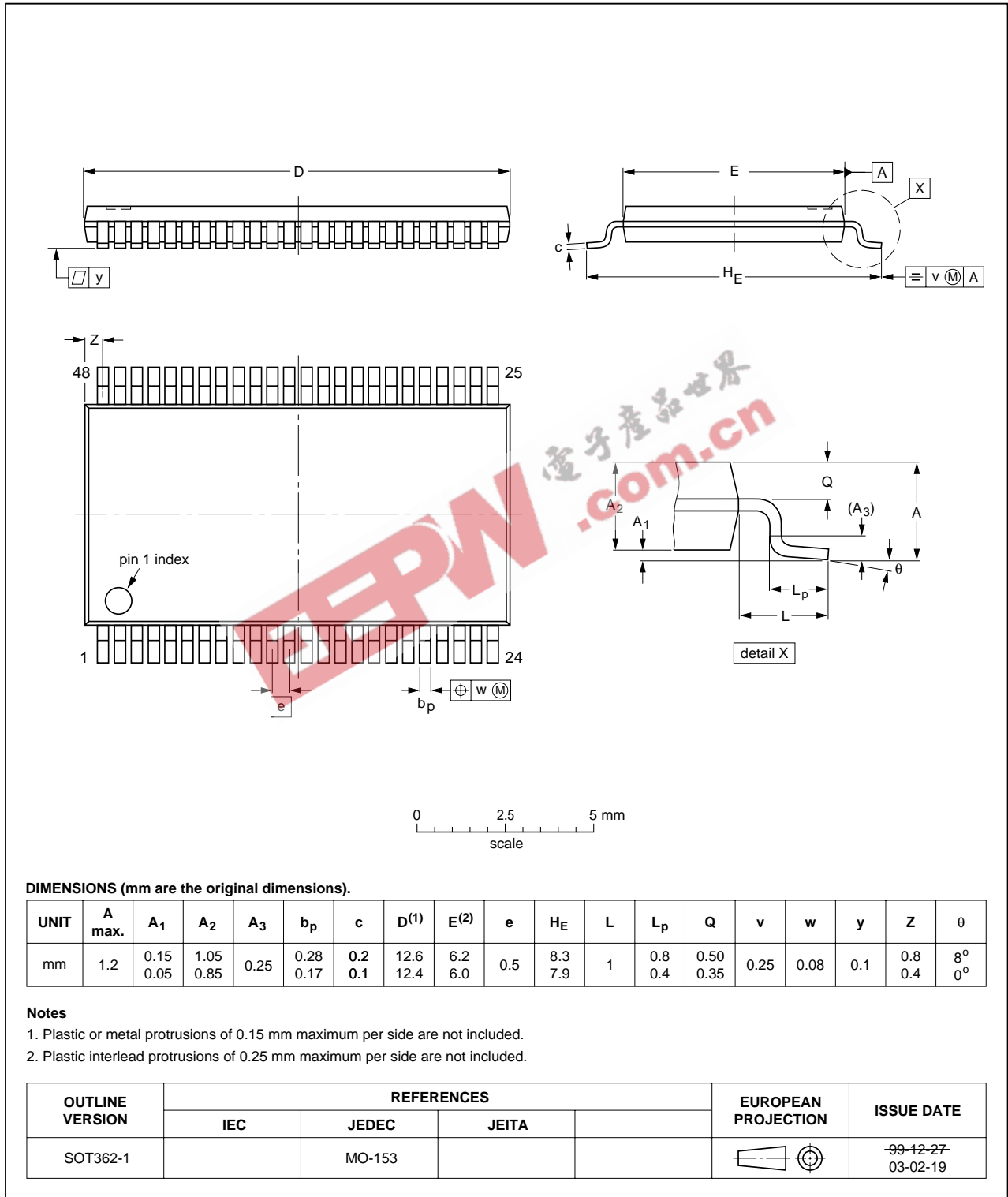


Fig 9. Package outline SOT362-1 (TSSOP48)

VFPGA56: plastic very thin fine-pitch ball grid array package; 56 balls; body 4.5 x 7 x 0.65 mm

SOT702-1

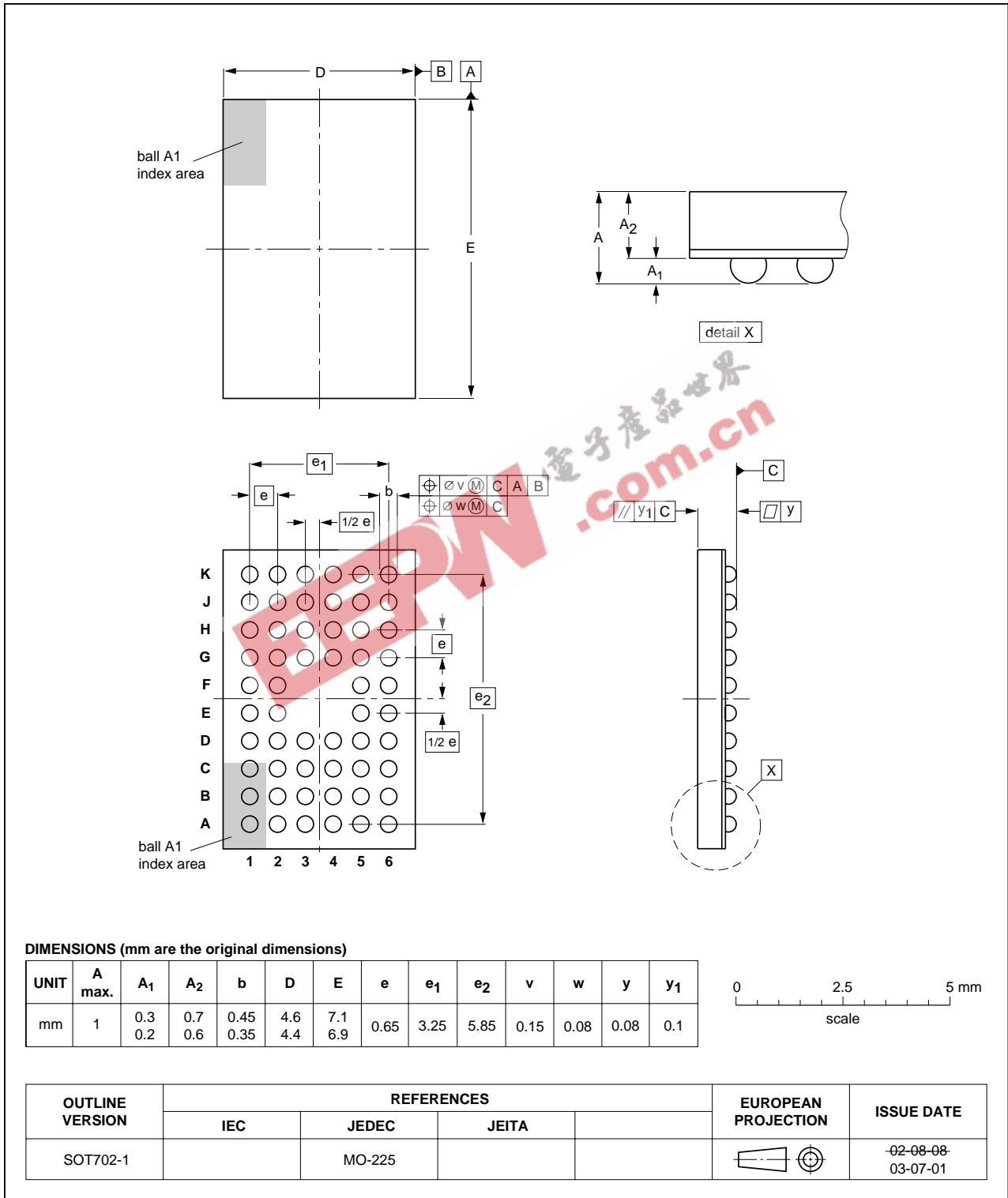


Fig 10. Package outline SOT702-1 (VFPGA56)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	Electrostatic Discharge
TTL	Transistor-Transistor Logic

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT_LVTH16244B_5	20060321	Product data sheet	-	74LVT16244B_4
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. Section 4: added type numbers 74LVTH16244BDL and 74LVTH16244BDGG. 			
74LVT16244B_4	20021031	Product specification	-	74LVT16244B_3
74LVT16244B_3	19981007	Product specification	-	74LVT16244B_2
74LVT16244B_2	19980219	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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