74LVC32245A

32-bit bus transceiver with direction pin; 5 V tolerant; 3-state

Rev. 01 — 20 August 2007 Product data sheet

1. General description

The 74LVC32245A is a 32-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The device features four output enable ($n\overline{OE}$) inputs for easy cascading and four send/receive (nDIR) inputs for direction control. Pin $n\overline{OE}$ controls the outputs so that the buses are effectively isolated.

Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs. These features allow the use of these devices in mixed 3.3 V and 5 V applications.

To ensure the high-impedance state during power-up or power-down, pin $n\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

2. Features

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- MULTIBYTE flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- High-impedance when V_{CC} = 0 V
- Complies with JEDEC standard JESD8-B / JESD36
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
- Specified from –40 °C to +85 °C
- Packaged in plastic fine-pitch ball grid array package

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC32245AEC	–40 °C to +85 °C	LFBGA96	plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 × 5.5 × 1.05 mm	SOT536-1

4. Functional diagram

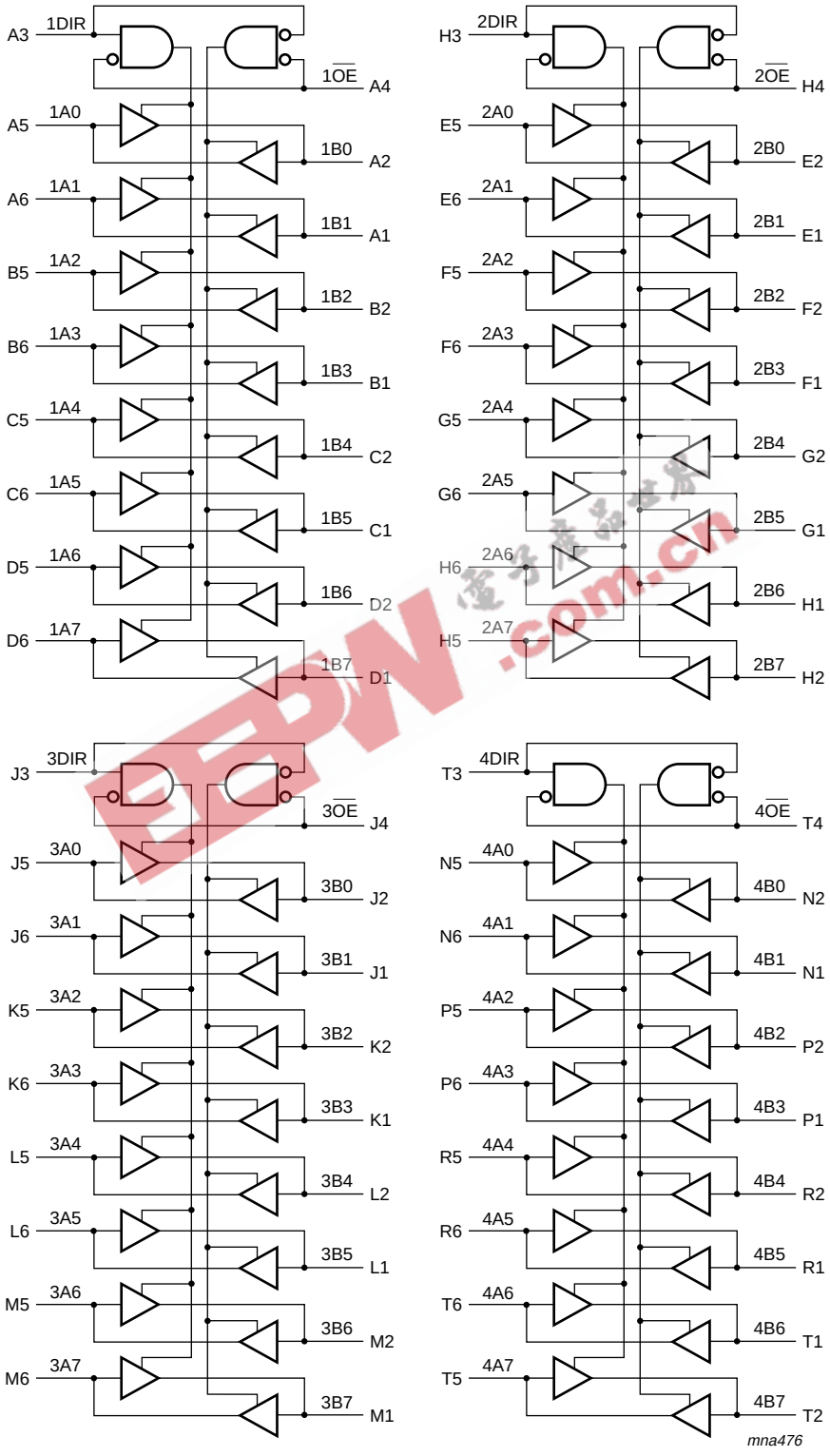


Fig 1. Logic symbol

5. Pinning information

5.1 Pinning

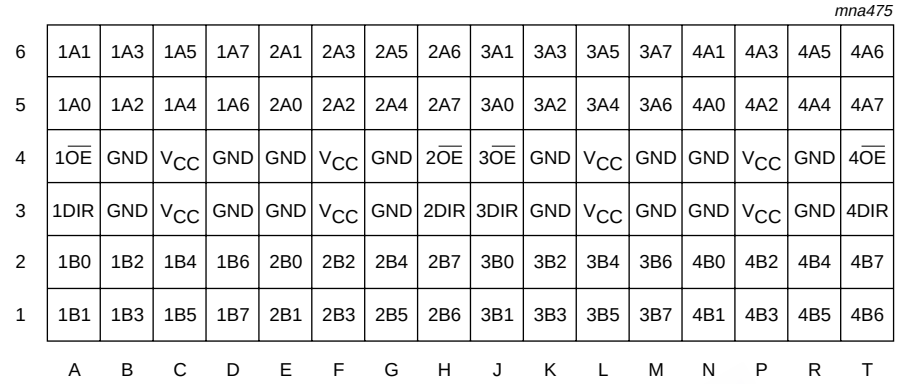


Fig 2. Pin configuration

5.2 Pin description

Table 2. Pin description

Pin name	Ball	Description
nDIR (n = 1 to 4)	A3, H3, J3, T3	direction control
n$\overline{OE}$ (n = 1 to 4)	A4, H4, J4, T4	output enable input (active LOW)
1A[0:7]	A5, A6, B5, B6, C5, C6, D5, D6	input or output
1B[0:7]	A2, A1, B2, B1, C2, C1, D2, D1	input or output
2A[0:7]	E5, E6, F5, F6, G5, G6, H6, H5	input or output
2B[0:7]	E2, E1, F2, F1, G2, G1, H1, H2	input or output
3A[0:7]	J5, J6, K5, K6, L5, L6, M5, M6	input or output
3B[0:7]	J2, J1, K2, K1, L2, L1, M2, M1	input or output
4A[0:7]	N5, N6, P5, P6, R5, R6, T6, T5	input or output
4B[0:7]	N2, N1, P2, P1, R2, R1, T1, T2	input or output
GND	B3, B4, D3, D4, E3, E4, G3, G4, K3, K4, M3, M4, N3, N4, R3, R4	ground (0 V)
V_{CC}	C3, C4, F3, F4, L3, L4, P3, P4	supply voltage

6. Functional description

Table 3. Function selection[1]

Input		Output	
n$\overline{OE}$	**nDIR**	**nAn**	**nBn**
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		–50	-	mA
V_I	input voltage		[1]	–0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	output HIGH or LOW state	[2]	–0.5	V_{CC} + 0.5	V
		output 3-state	[2]	–0.5	+6.5	V
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current		[3]	-	200	mA
I_{GND}	ground current		[3]	–200	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +85 °C	[4]	-	1000	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] All supply and ground pins connected externally to one voltage source.

[4] Above 70 °C the value of P_{tot} derates linearly with 1.8 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	for maximum speed performance	2.7	-	3.6	V
		for low-voltage applications	1.2	-	-	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	output HIGH or LOW state	0	-	V_{CC}	V
		output 3-state	0	-	5.5	V
T_{amb}	ambient temperature	in free air	–40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.2 V to 2.7 V	-	-	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	-	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Typ[1]	Max	Unit
T_{amb} = −40 °C to +85 °C							
V_{IH}	HIGH-level input voltage		1.2	V_{CC}	-	-	V
			2.7 to 3.6	2.0	-	-	V
V_{IL}	LOW-level input voltage		1.2	-	-	GND	V
			2.7 to 3.6	-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = −100 µA	2.7 to 3.6	V_{CC} − 0.2	V_{CC}	-	V
		I_O = −12 mA	2.7	V_{CC} − 0.5	-	-	V
		I_O = −18 mA	3.0	V_{CC} − 0.6	-	-	V
		I_O = −24 mA	3.0	V_{CC} − 0.8	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 100 µA	2.7 to 3.6	-	GND	0.20	V
		I_O = 12 mA	2.7	-	-	0.40	V
		I_O = 24 mA	3.0	-	-	0.55	V
I_I	input leakage current	V_I = 5.5 V or GND	3.6	-	±0.1	±5	µA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND	3.6 [2]	-	±0.1	±5	µA
I_{OFF}	power-off leakage current	V_I or V_O = 5.5 V	0.0	-	±0.1	±10	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A	3.6	-	0.1	40	µA
ΔI_{CC}	additional supply current	per input pin; V_I = V_{CC} − 0.6 V; I_O = 0 A	2.7 to 3.6	-	5	500	µA
C_I	input capacitance	V_I = GND to V_{CC}	0 to 3.6	-	5.0	-	pF
$C_{I/O}$	input/output capacitance	V_I = GND to V_{CC}	0 to 3.6	-	10	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

[2] For I/O ports the parameter I_{OZ} includes the input leakage current.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 5.

Symbol	Parameter	Conditions	V_{CC} (V)		Min	Typ[1]	Max	Unit
T_{amb} = −40 °C to +85 °C								
t_{pd}	propagation delay	nAn to nBn; nBn to nAn; see Figure 3	1.2	[2]	-	13.0	-	ns
			2.7		1.0	2.7	4.7	ns
			3.0 to 3.6		1.0	2.2	4.5	ns
t_{en}	enable time	$n\overline{OE}$ to nAn, nBn: see Figure 4	1.2	[2]	-	15.0	-	ns
			2.7		1.5	3.6	6.7	ns
			3.0 to 3.6		1.0	2.8	5.5	ns
t_{dis}	disable time	$n\overline{OE}$ to nAn, nBn; see Figure 4	1.2	[2]	-	11.0	-	ns
			2.7		1.5	3.4	6.6	ns
			3.0 to 3.6		1.5	3.2	5.6	ns
$t_{sk(o)}$	output skew time		3.0 to 3.6	[3]	-	-	1.0	ns
C_{PD}	power dissipation capacitance	per buffer; V_I = GND to V_{CC}	3.3	[4]	-	30	-	pF

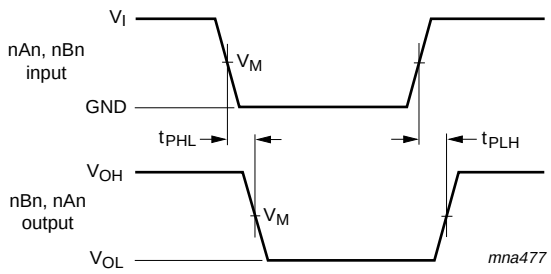
[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 2.7 V, and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

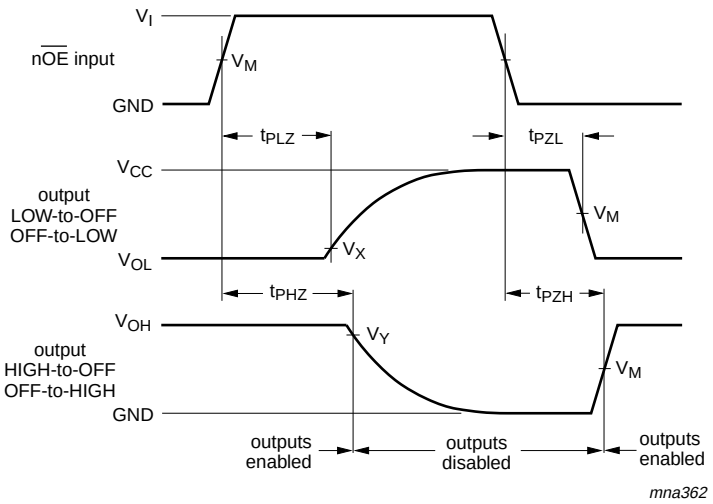
[4] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; f_o = output frequency in MHz
C_L = output load capacitance in pF
V_{CC} = supply voltage in Volts
N = number of inputs switching
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11. Waveforms



V_M = 1.5 V at $V_{CC} \geq$ 2.7 V.
V_M = 0.5 × V_{CC} at V_{CC} < 2.7 V.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 3. The input (nAn, nBn) to output (nBn, nAn) propagation delays



V_M = 1.5 V at $V_{CC} \geq$ 2.7 V.

V_M = 0.5 $\times V_{CC}$ at V_{CC} < 2.7 V.

$V_X = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 2.7 V;

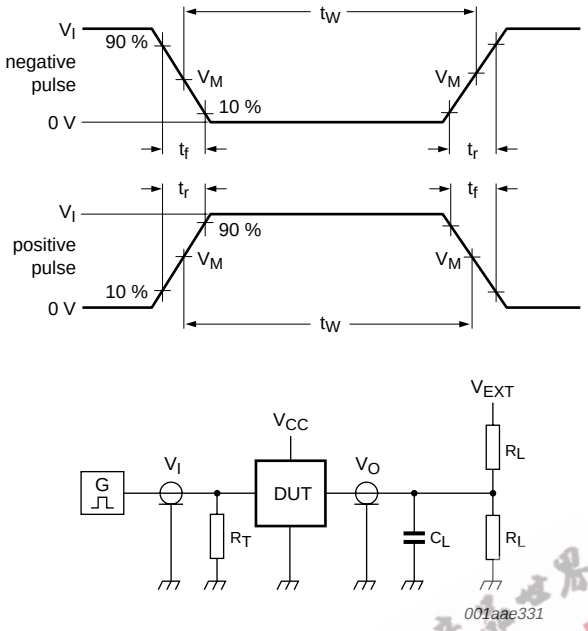
$V_X = V_{OL}$ + 0.15 V at V_{CC} < 2.7 V.

$V_Y = V_{OH}$ − 0.3 V at $V_{CC} \geq$ 2.7 V;

$V_Y = V_{OH}$ − 0.15 V at V_{CC} < 2.7 V.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 4. 3-state enable and disable times.



Test data is given in Table 8.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

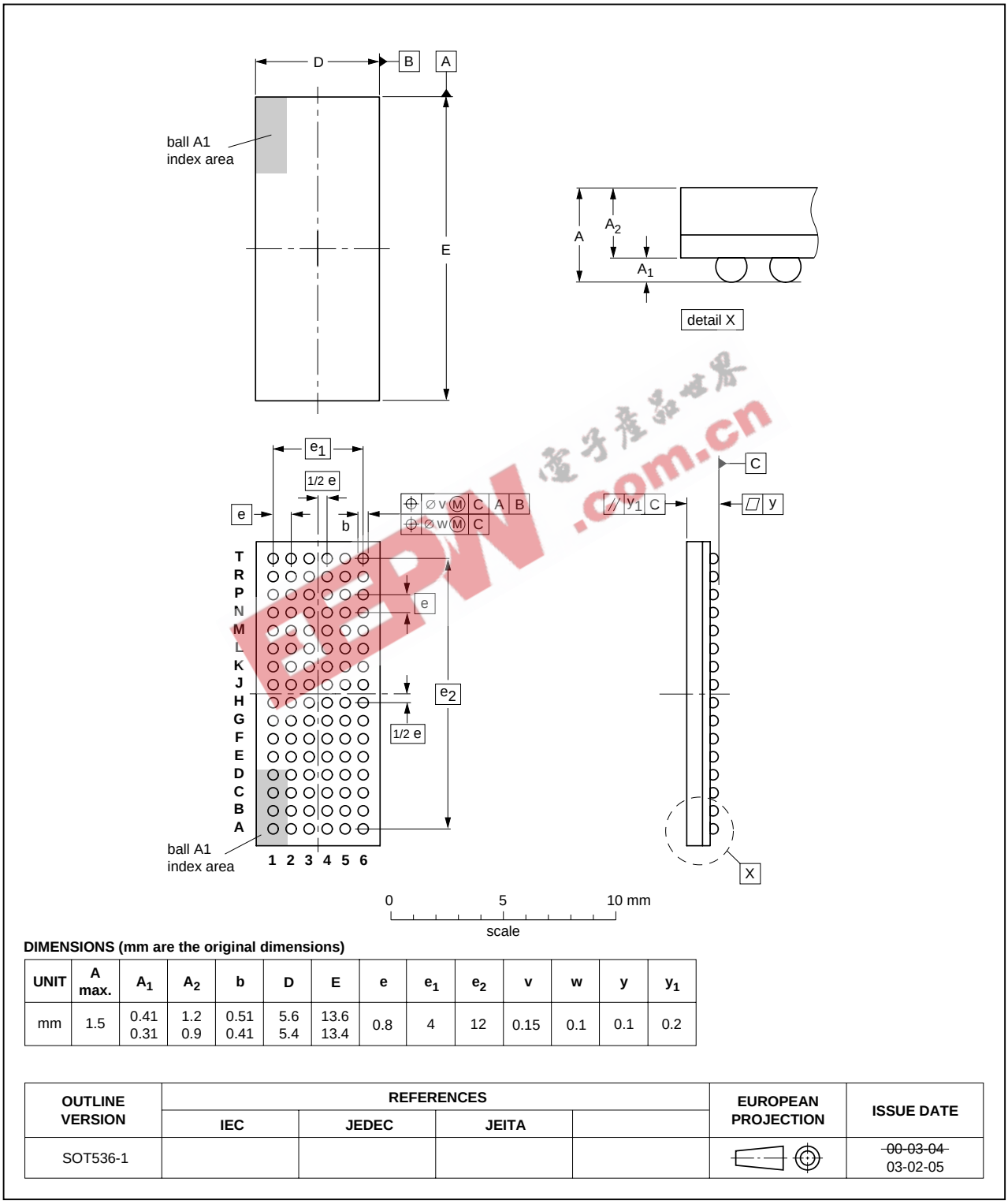
Fig 5. Load circuitry for switching times

Table 8. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND

12. Package outline

LFBGA96: plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 x 5.5 x 1.05 mm SOT536-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.5	0.41 0.31	1.2 0.9	0.51 0.41	5.6 5.4	13.6 13.4	0.8	4	12	0.15	0.1	0.1	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT536-1						~~00-03-04~~ 03-02-05

Fig 6. Package outline SOT536-1 (LFBGA96)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC32245A_1	20070820	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[2] The term 'short data sheet' is explained in section "Definitions".

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17. Contents

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