FAIRCHILD

SEMICONDUCTOR ™

74AC253 • 74ACT253
Dual 4-Input Multiplexer with 3-STATE Outputs

General Description

The AC/ACT253 is a dual 4-input multiplexer with 3-STATE outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus oriented systems.

Features

- I_{CC} and I_{OZ} reduced by 50%
- Multifunction capability
- Non inverting 3-STATE outputs
- Outputs source/sink 24 mA
- ACT253 has TTL-compatible inputs

Ordering Code:

Order Number	Package Number	Package Description
74AC253SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74AC253SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC253PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
74ACT253SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74ACT253SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT253MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT253PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Device also available Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Diagrams

IEEE/IEC
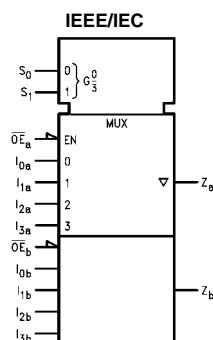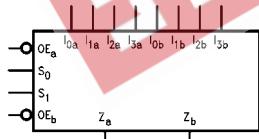
Connection Diagram
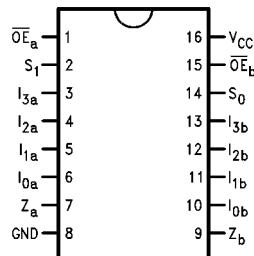
Pin Descriptions

Pin Names	Description
I_{0a}–I_{3a}	Side A Data Inputs
I_{0b}–I_{3b}	Side B Data Inputs
S_0, S_1	Common Select Inputs
$\overline{OE}_a$	Side A Output Enable Input
$\overline{OE}_b$	Side B Output Enable Input
Z_a, Z_b	3-STATE Outputs

FACT™ is a trademark of Fairchild Semiconductor Corporation.

Functional Description

The AC/ACT253 contains two identical 4-input multiplexers with 3-STATE outputs. They select two bits from four sources selected by common Select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which, when HIGH, force the outputs to a high impedance (High Z) state. This device is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown:

$$Z_a = \overline{OE}_a \bullet \quad (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + $$
$$I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$
$$Z_b = \overline{OE}_b \bullet \quad (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + $$
$$I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

If the outputs of 3-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-STATE devices whose outputs are tied together are designed so that there is no overlap.

Truth Table

Select Inputs		Data Inputs				Output Enable	Outputs
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Z
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address Inputs S_0 and S_1 are common to both sections.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram
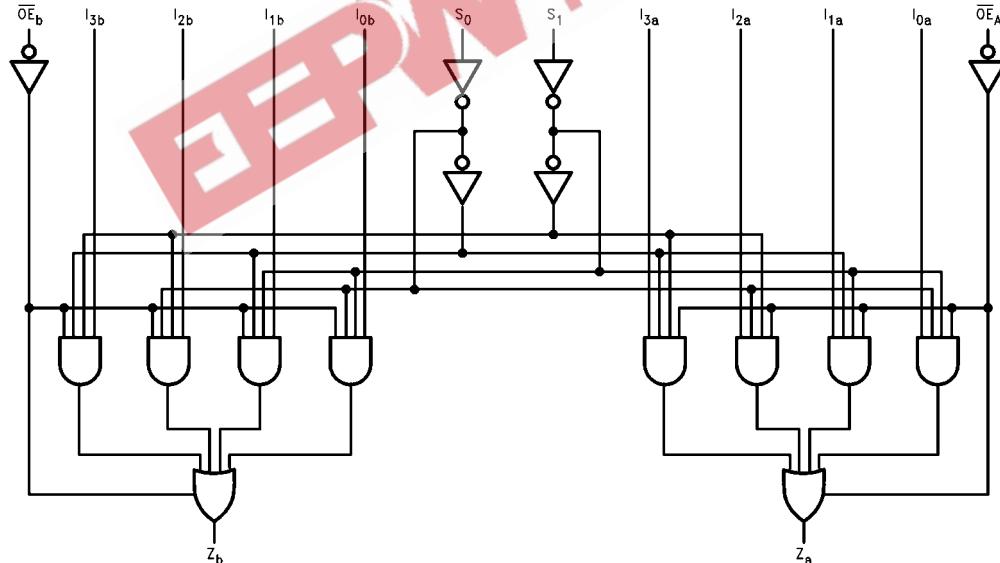
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = −0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = −0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to $V_{CC} + 0.5V$
DC Output Source	
or Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	± 50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
AC	2.0V to 6.0V
ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Typ	$T_A = −40°C$ to +85°C Guaranteed Limits		Units	Conditions
V_{IH}	Minimum HIGH Level Input Voltage	3.0	1.5	2.1	2.1		$V_{OUT} = 0.1V$ or $V_{CC} − 0.1V$
		4.5	2.25	3.15	3.15	V	
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum LOW Level Input Voltage	3.0	1.5	0.9	0.9		$V_{OUT} = 0.1V$ or $V_{CC} − 0.1V$
		4.5	2.25	1.35	1.35	V	
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9		$I_{OUT} = −50 \mu A$
		4.5	4.49	4.4	4.4	V	
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46		$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = −12$ mA
		4.5		3.86	3.76	V	$I_{OH} = −24$ mA
		5.5		4.86	4.76		$I_{OH} = −24$ mA (Note 2)
V_{OL}	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1		$I_{OUT} = 50 \mu A$
		4.5	0.001	0.1	0.1	V	
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.44		$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 12$ mA
		4.5		0.36	0.44	V	$I_{OL} = 24$ mA
		5.5		0.36	0.44		$I_{OL} = 24$ mA (Note 2)
I_{IN} (Note 4)	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum 3-STATE Current	5.5		±0.25	±2.5	μA	V_I (OE) $= V_{IL}$, V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
I_{OLD}	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}	Output Current (Note 3)	5.5			−75	mA	$V_{OHD} = 3.85V$ Min
I_{CC} (Note 4)	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

74AC253 • 74ACT253

DC Electrical Characteristics for ACT

Symbol	Parameter	V$_{CC}$ (V)	T$_A$ = +25°C		T$_A$ = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits	Guaranteed Limits		
V$_{IH}$	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0	V	V$_{OUT}$ = 0.1V or V$_{CC}$ − 0.1V
		5.5	1.5	2.0	2.0		
V$_{IL}$	Maximum LOW Level Input Voltage	4.5	1.5	0.8	0.8	V	V$_{OUT}$ = 0.1V or V$_{CC}$ − 0.1V
		5.5	1.5	0.8	0.8		
V$_{OH}$	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4	V	I$_{OUT}$ = −50 µA
		5.5	5.49	5.4	5.4		
		4.5		3.86	3.76	V	V$_{IN}$ = V$_{IL}$ or V$_{IH}$ I$_{OH}$ = −24 mA
		5.5		4.86	4.76		I$_{OH}$ = −24 mA (Note 5)
V$_{OL}$	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1	V	I$_{OUT}$ = 50 µA
		5.5	0.001	0.1	0.1		
		4.5		0.36	0.44	V	V$_{IN}$ = V$_{IL}$ or V$_{IH}$ I$_{OL}$ = 24 mA
		5.5		0.36	0.44		I$_{OL}$ = 24 mA (Note 5)
I$_{IN}$	Maximum Input Leakage Current	5.5		±0.1	±1.0	µA	V$_I$ = V$_{CC}$, GND
I$_{OZ}$	Maximum 3-STATE Current	5.5		±0.25	±2.5	µA	V$_I$ = V$_{IL}$, V$_{IH}$ V$_O$ = V$_{CC}$, GND
I$_{CCT}$	Maximum I$_{CC}$/Input	5.5	0.6		1.5	mA	V$_I$ = V$_{CC}$ − 2.1V
I$_{OLD}$	Minimum Dynamic	5.5			75	mA	V$_{OLD}$ = 1.65V Max
I$_{OHD}$	Output Current (Note 6)	5.5			−75	mA	V$_{OHD}$ = 3.85V Min
I$_{CC}$	Maximum Quiescent Supply Current	5.5		4.0	40.0	µA	V$_{IN}$ = V$_{CC}$ or GND

Note 5: All outputs loaded; thresholds on input associated with output under test.

Note 6: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics for AC

Symbol	Parameter	V$_{CC}$ (V) (Note 7)	T$_A$ = +25°C C$_L$ = 50 pF			T$_A$ = −40°C to +85°C C$_L$ = 50 pF		Units
			Min	Typ	Max	Min	Max	
t$_{PLH}$	Propagation Delay S$_n$ to Z$_n$	3.3	2.0	8.5	15.5	2.0	17.5	ns
		5.0	2.0	6.5	11.0	1.5	12.5	
t$_{PHL}$	Propagation Delay S$_n$ to Z$_n$	3.3	2.5	9.5	16.0	2.0	18.0	ns
		5.0	2.0	7.0	11.5	1.5	13.0	
t$_{PLH}$	Propagation Delay I$_n$ to Z$_n$	3.3	1.5	7.0	14.5	1.5	17.0	ns
		5.0	1.5	5.5	10.0	1.5	11.5	
t$_{PHL}$	Propagation Delay I$_n$ to Z$_n$	3.3	2.0	7.5	13.0	1.5	15.0	ns
		5.0	1.5	5.5	9.5	1.5	11.0	
t$_{PZH}$	Output Enable Time	3.3	1.5	4.5	8.0	1.0	8.5	ns
		5.0	1.5	3.5	6.0	1.0	6.5	
t$_{PZL}$	Output Enable Time	3.3	1.5	5.0	8.0	1.0	9.0	ns
		5.0	1.5	3.5	6.0	1.0	7.0	
t$_{PHZ}$	Output Disable Time	3.3	2.0	5.5	9.5	1.5	10.0	ns
		5.0	2.0	5.0	8.0	1.5	8.5	
t$_{PLZ}$	Output Disable Time	3.3	1.5	5.0	8.0	1.0	9.0	ns
		5.0	1.5	4.0	7.0	1.0	7.5	

Note 7: Voltage Range 3.3 is 3.3V ± 0.3V

Voltage Range 5.0 is 5.0V ± 0.5V

AC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V) (Note 8)	$T_A = +25°C$ $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay S_n to Z_n	5.0	2.0	7.0	11.5	2.0	13.0	ns
t_{PHL}	Propagation Delay S_n to Z_n	5.0	3.0	7.5	13.0	2.5	14.5	ns
t_{PLH}	Propagation Delay I_n to Z_n	5.0	2.5	5.5	10.0	2.0	11.0	ns
t_{PHL}	Propagation Delay I_n to Z_n	5.0	3.5	6.5	11.0	3.0	12.5	ns
t_{PZH}	Output Enable Time	5.0	2.0	4.5	7.5	1.5	8.5	ns
t_{PZL}	Output Enable Time	5.0	2.0	5.0	8.0	1.5	9.0	ns
t_{PHZ}	Output Disable Time	5.0	3.0	6.0	9.5	2.5	10.0	ns
t_{PLZ}	Output Disable Time	5.0	2.5	4.5	7.5	2.0	8.5	ns

Note 8: Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	50.0	pF	V_{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted

0.386 − 0.394
(9.804 − 10.00)

16 15 14 13 12 11 10 9

0.228 − 0.244
(5.791 − 6.198)

30°
TYP

LEAD NO.1
IDENT

1 2 3 4 5 6 7 8

0.010 MAX
(0.254)

0.150 − 0.157
(3.810 − 3.988)

0.010 − 0.020
(0.254 − 0.508) × 45°

8° MAX TYP
ALL LEADS

0.008 − 0.010
(0.203 − 0.254)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.053 − 0.069
(1.346 − 1.753)

0.004 − 0.010
(0.102 − 0.254)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.014 − 0.020 TYP
(0.356 − 0.508)

0.008 TYP
(0.203)

M16A (REV H)
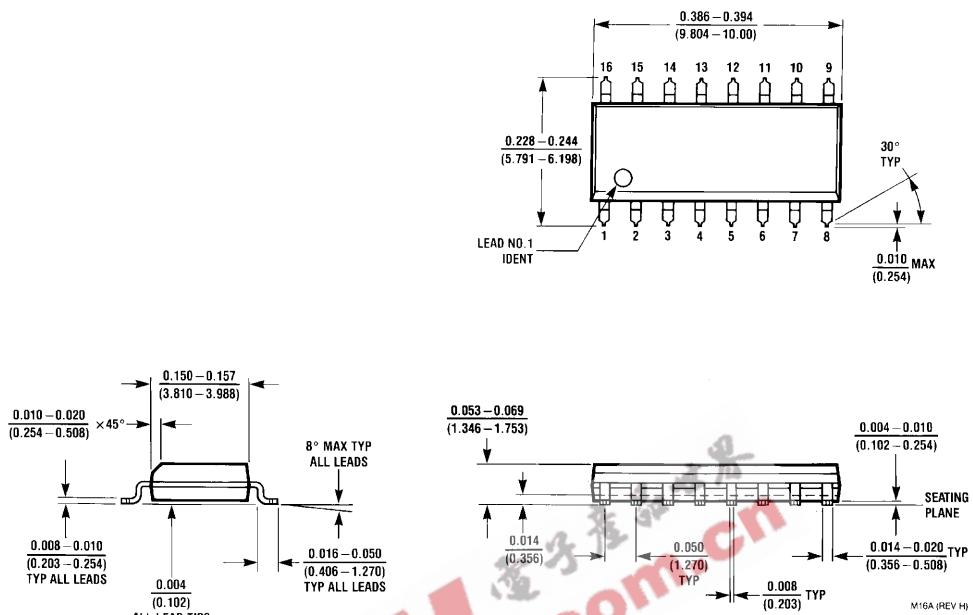
16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

10.2±0.1

-A-

0.47 TYP

16   9

7.8

5.3±0.1

-B-

3.9

⌓ 0.2 C B A
ALL LEAD TIPS

PIN #1 IDENT.

1   8

LAND PATTERN RECOMMENDATION

16   15   10   9

5.01 TYP

9.27 TYP

1   2   7   8

(2.13 TYP)

1.27 TYP   0.6 TYP

ALL LEAD TIPS

2.1 MAX.

⌓ 0.1 C

-C-

1.27 TYP

0.35-0.51

⊕ 0.12 Ⓜ C A

DIMENSIONS ARE IN MILLIMETERS

1.8±0.1

0.15±0.05

SEE DETAIL A

0.15-0.25

7° TYP

GAGE PLANE

0°-8° TYP

0.25

0.60±0.15

1.25

SEATING PLANE

DETAIL A
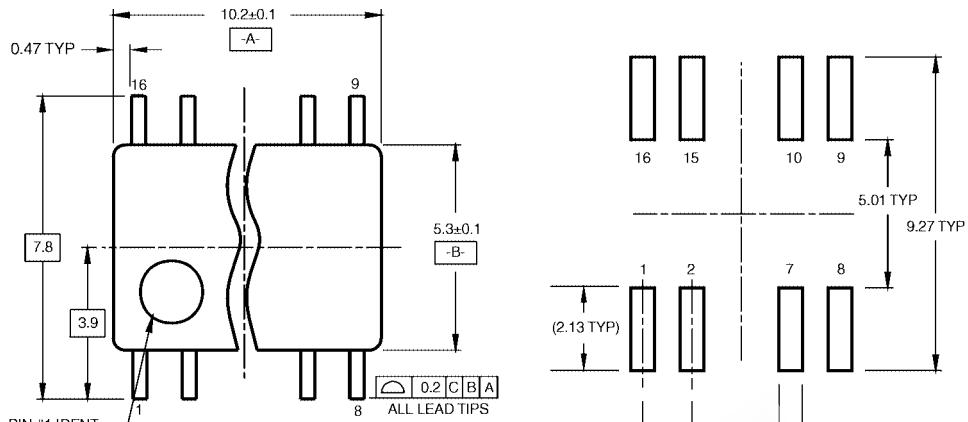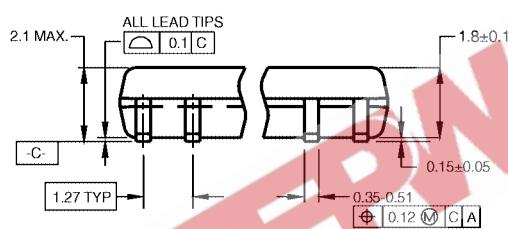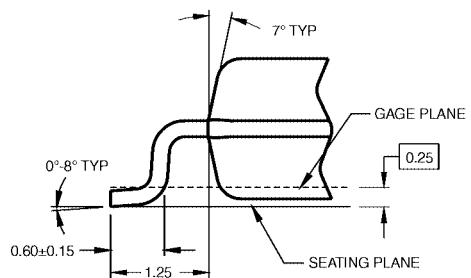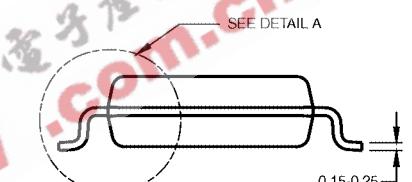
NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION,
   ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD
   FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1

**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

DIMENSIONS METRIC ONLY

7.72 TYP.
4.16 TYP.

(1.78 TYP)

0.42 TYP

0.65 TYP

LAND PATTERN RECOMMENDATION

5.0 ± 0.1

-A-

16   9

6.4

3.2

4.4 ± 0.1

-B-

0° - 8°

PIN #1 IDENT.

1   8

⌀ 0.2 C B A

ALL LEAD TIPS

⌀ 0.1 C

ALL LEAD TIPS

-C-

0.65 TYP

(0.90)

1.1 MAX TYP

0.10 ± 0.05 TYP

0.19 - 0.30 TYP

⊕ 0.13 Ⓜ A B Ⓢ C Ⓢ

GAGE PLANE

0.25

SEATING PLANE

0.6 ± 0.1

DETAIL A

TYPICAL, SCALE: 40X

SEE DETAIL A

0.09-0.20 TYP

MTC16 (REV C)
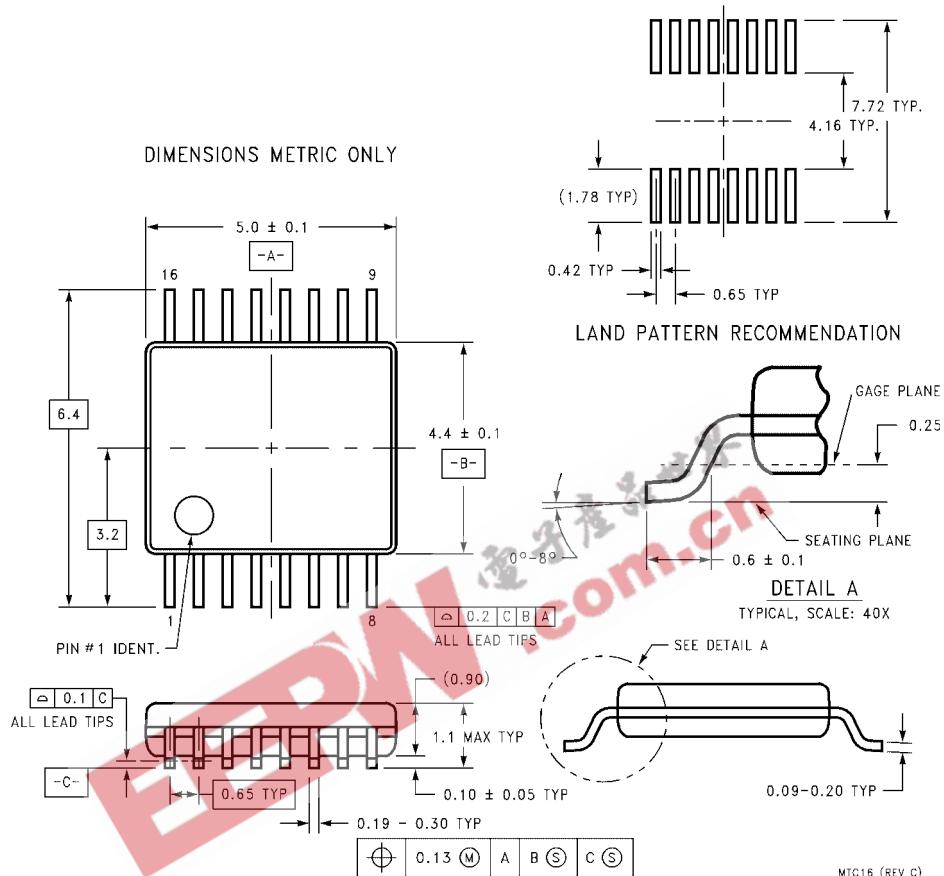
16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)
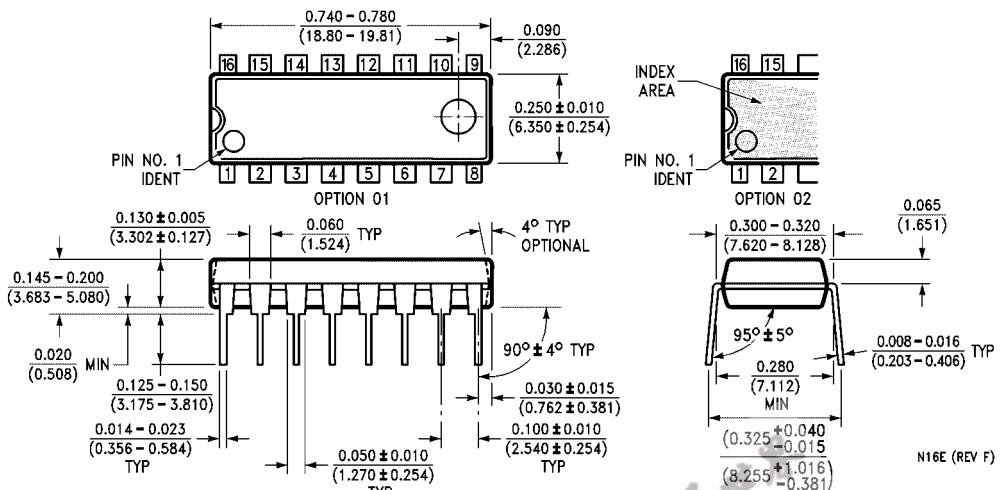
16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E

N16E (REV F)

LIFE SUPPORT POLICY