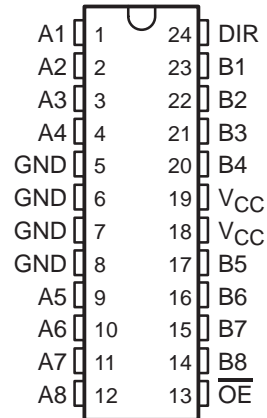# 74AC11640
OCTAL BUS TRANSCEIVER
WITH 3–STATE OUTPUTS
SCAS052A – JULY 1987 – REVISED APRIL 1993

- **Bidirectional Bus Transceivers in High-Density 24-Pin Packages**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **_EPIC_ ™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)

A1	1	24	DIR
A2	2	23	B1
A3	3	22	B2
A4	4	21	B3
GND	5	20	B4
GND	6	19	V_{CC}
GND	7	18	V_{CC}
GND	8	17	B5
A5	9	16	B6
A6	10	15	B7
A7	11	14	B8
A8	12	13	$\overline{OE}$

description

These octal bus transceivers are designed for asynchronous communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

The 74AC11640 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to B bus
H	X	Isolation

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TEXAS INSTRUMENTS

74AC11640
OCTAL BUS TRANSCEIVER
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logic symbol†

```
 OE   13 ─────▷  G3
 DIR  24 ─────▷  3 EN1 [BA]
                 3 EN2 [AB]

 A1   1 ──◁──  ▽ 1    1        23  B1
               1    2 ▽
 A2   2 ◄──►                   22  B2
 A3   3 ◄──►                   21  B3
 A4   4 ◄──►                   20  B4
 A5   9 ◄──►                   17  B5
 A6  10 ◄──►                   16  B6
 A7  11 ◄──►                   15  B7
 A8  12 ◄──►                   14  B8
```
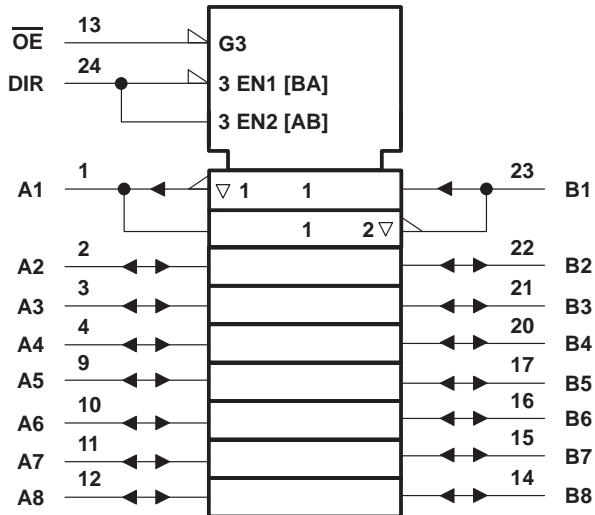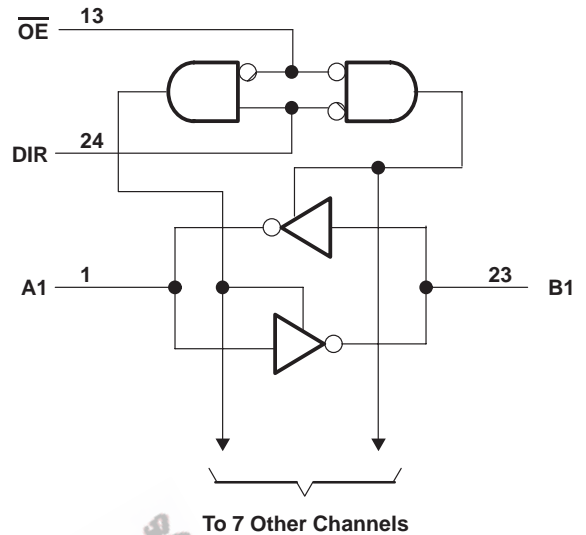
logic diagram (positive logic)

To 7 Other Channels

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and
   IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) .... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) .... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) .... ±50 mA
Continuous current through V_{CC} or GND pins .... ±200 mA
Storage temperature range .... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

TEXAS
INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate	$\overline{OE}$ or DIR	0		5	ns/V
		Data	0		10	
T_A	Operating free-air temperature		−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = −50 µA	3 V	2.9			2.9		V
			4.5 V	4.4			4.4		
			5.5 V	5.4			5.4		
		I_{OH} = −4 mA	3 V	2.58			2.48		
		I_{OH} = −24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = −75 mA[†]	5.5 V				3.85		
V_{OL}		I_{OL} = 50 µA	3 V			0.1		0.1	V
			4.5 V			0.1		0.1	
			5.5 V			0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA[†]	5.5 V					1.65	
I_I	$\overline{OE}$ or DIR	V_I = V_{CC} or GND	5.5 V		±0.1			±1	µA
I_{OZ}[‡]	A or B ports	V_O = V_{CC} or GND	5.5 V		±0.5			±5	µA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V		8			80	µA
C_i	$\overline{OE}$ or DIR	V_I = V_{CC} or GND	5 V		4				pF
C_{io}		V_O = V_{CC} or GND	5 V		12				pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

TEXAS
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switching characteristics over recommended operating free-air temperature range,
$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ **(unless otherwise noted) (see Figure 1)**

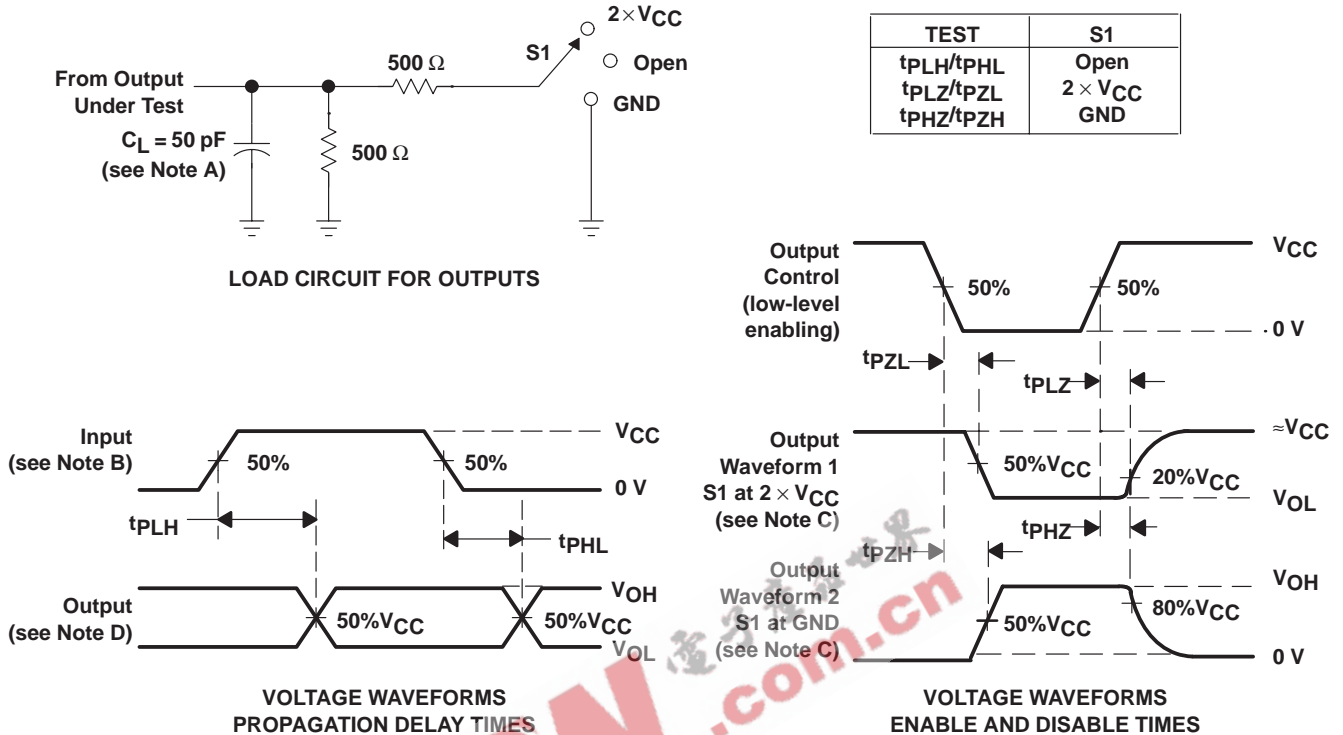| PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25°C$			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	1.5	7	10.5	1.5	12	ns
t_{PHL}			1.5	6.3	9.1	1.5	10.2	
t_{PZH}	OE	A or B	1.5	8.9	12.5	1.5	14.3	ns
t_{PZL}			1.5	8.4	12.9	1.5	14.6	
t_{PHZ}	OE	A or B	1.5	7.9	10	1.5	10.8	ns
t_{PLZ}			1.5	8.6	11	1.5	12	

switching characteristics over recommended operating free-air temperature range,
$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ **(unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25°C$			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	1.5	5.1	7.7	1.5	8.8	ns
t_{PHL}			1.5	4.6	6.9	1.5	7.8	
t_{PZH}	OE	A or B	1.5	6.5	9.4	1.5	10.6	ns
t_{PZL}			1.5	6.1	9.4	1.5	10.6	
t_{PHZ}	OE	A or B	1.5	6.7	8.6	1.5	9.3	ns
t_{PLZ}			1.5	7.2	9.1	1.5	9.9	

operating characteristics, $V_{CC} = 5 \text{ V}, T_A = 25°C$

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd} Power dissipation capacitance per transceiver	Outputs enabled	$C_L = 50 \text{ pF},$	$f = 1 \text{ MHz}$	45	pF
	Outputs disabled			12	

PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT FOR OUTPUTS

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
For testing pulse duration: t_r = t_f = 1 to 3 ns. Pulse polarity can be either high-to-low-to-high or low-to-high-to-low.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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