![Texas Instruments logo] **TEXAS INSTRUMENTS**
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**SN54LVTH162245, SN74LVTH162245
3.3-V ABT 16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS**

SCBS260Q−JUNE 1993−REVISED NOVEMBER 2006

FEATURES

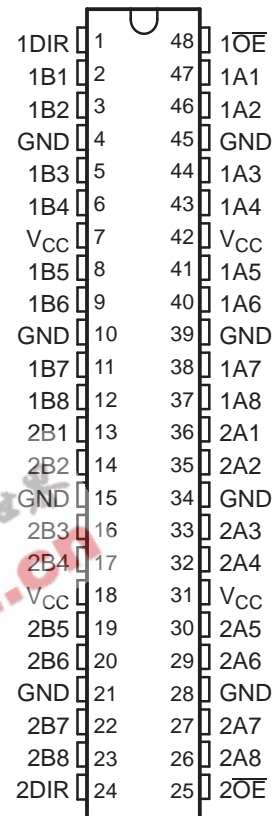- **Members of the Texas Instruments Widebus™ Family**

- **A-Port Outputs Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required**

- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**

- **Support Unregulated Battery Operation Down to 2.7 V**

- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**

- **I_{off} and Power-Up 3-State Support Hot Insertion**

- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**

- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**

- **Flow-Through Architecture Optimizes PCB Layout**

- **Latch-Up Performance Exceeds 500 mA Per JESD 17**

- **ESD Protection Exceeds JESD 22**
    - **2000-V Human-Body Model (A114-A)**
    - **200-V Machine Model (A115-A)**
    - **1000-V Charged-Device Model (C101)**

**SN54LVTH162245 . . . WD PACKAGE
SN74LVTH162245 . . . DGG OR DL PACKAGE
(TOP VIEW)**

1DIR	1	48	1$\overline{OE}$
1B1	2	47	1A1
1B2	3	46	1A2
GND	4	45	GND
1B3	5	44	1A3
1B4	6	43	1A4
V_{CC}	7	42	V_{CC}
1B5	8	41	1A5
1B6	9	40	1A6
GND	10	39	GND
1B7	11	38	1A7
1B8	12	37	1A8
2B1	13	36	2A1
2B2	14	35	2A2
GND	15	34	GND
2B3	16	33	2A3
2B4	17	32	2A4
V_{CC}	18	31	V_{CC}
2B5	19	30	2A5
2B6	20	29	2A6
GND	21	28	GND
2B7	22	27	2A7
2B8	23	26	2A8
2DIR	24	25	2$\overline{OE}$

DESCRIPTION/ORDERING INFORMATION

The 'LVTH162245 devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

The logic levels of the direction-control (DIR) input and the output-enable ($\overline{OE}$) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports is always active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ}.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

The A-port outputs, which are designed to source or sink up to 12 mA, include equivalent 22-Ω series resistors to reduce overshoot and undershoot.

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DESCRIPTION/ORDERING INFORMATION (CONTINUED)

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

ORDERING INFORMATION

T_A	PACKAGE[1]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	FBGA – GRD	Reel of 1000	74LVTH162245GRDR	LL2245
	FBGA – ZRD (Pb-free)		74LVTH162245ZRDR	
	SSOP – DL	Tube of 25	SN74LVTH162245DL	LVTH162245
			SN74LVTH162245DLG4	
		Reel of 1000	SN74LVTH162245DLR	
			74LVTH162245DLRG4	
	TSSOP – DGG	Reel of 2000	SN74LVTH162245DGGR	LVTH162245
			74LVTH162245DGGRG4	
			74LVTH162245GRE4	
	VFBGA – GQL	Reel of 1000	SN74LVTH162245KR	LL2245
	VFBGA – ZQL (Pb-free)		74LVTH162245ZQLR	
−55°C to 125°C	CFP – WD	Tube	SNJ54LVTH162245WD	SNJ54LVTH162245WD

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

GQL OR ZQL PACKAGE
(TOP VIEW)
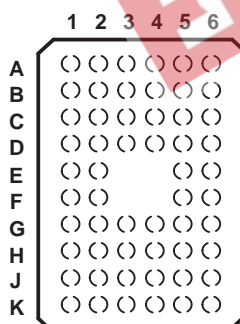
TERMINAL ASSIGNMENTS[1]
(56-Ball GQL/ZQL Package)

	1	2	3	4	5	6
A	1DIR	NC	NC	NC	NC	1$\overline{OE}$
B	1B2	1B1	GND	GND	1A1	1A2
C	1B4	1B3	V_{CC}	V_{CC}	1A3	1A4
D	1B6	1B5	GND	GND	1A5	1A6
E	1B8	1B7			1A7	1A8
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
H	2B5	2B6	V_{CC}	V_{CC}	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2DIR	NC	NC	NC	NC	2$\overline{OE}$

(1) NC – No internal connection

2

GRD OR ZRD PACKAGE
(TOP VIEW)
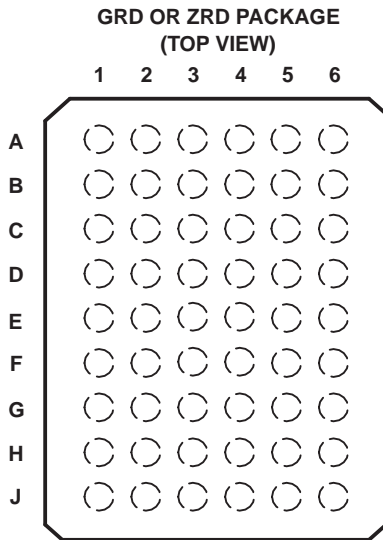
TERMINAL ASSIGNMENTS[1]
(54-Ball GRD/ZRD Package)

	1	2	3	4	5	6
A	1B1	NC	1DIR	1$\overline{\text{OE}}$	NC	1A1
B	1B3	1B2	NC	NC	1A2	1A3
C	1B5	1B4	V_{CC}	V_{CC}	1A4	1A5
D	1B7	1B6	GND	GND	1A6	1A7
E	2B1	1B8	GND	GND	1A8	2A1
F	2B3	2B2	GND	GND	2A2	2A3
G	2B5	2B4	V_{CC}	V_{CC}	2A4	2A5
H	2B7	2B6	NC	NC	2A6	2A7
J	2B8	NC	2DIR	2$\overline{\text{OE}}$	NC	2A8

(1) NC − No internal connection

FUNCTION TABLE[1]
(EACH 8-BIT SECTION)

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{\text{OE}}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os always are active.

LOGIC DIAGRAM (POSITIVE LOGIC)
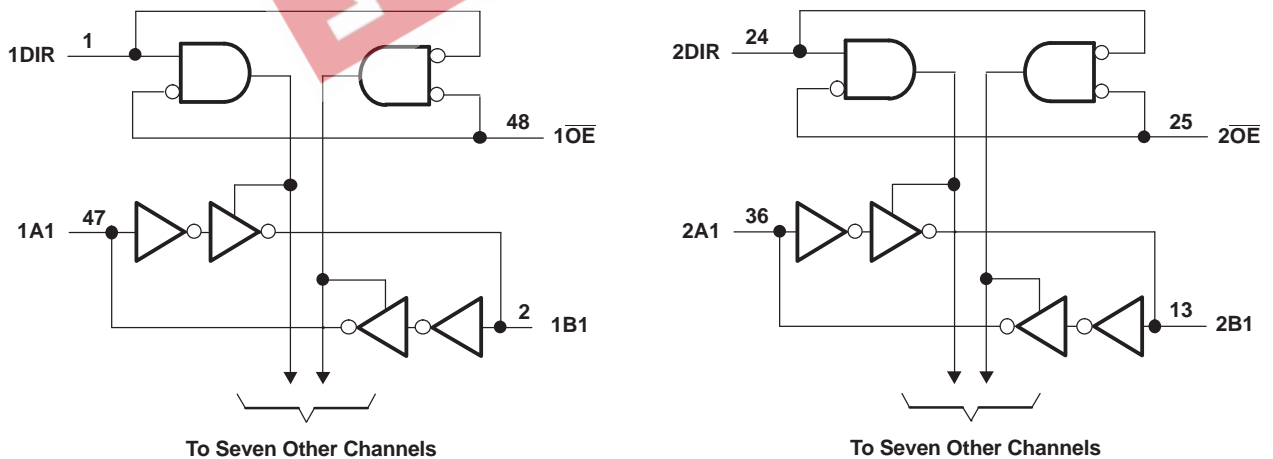
SN54LVTH162245, SN74LVTH162245
3.3-V ABT 16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS260Q−JUNE 1993−REVISED NOVEMBER 2006

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Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	4.6	V
V_I	Input voltage range[2]		−0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		−0.5	7	V
V_O	Voltage range applied to any output in the high state[2]		−0.5	V_{CC} + 0.5	V
I_O	Current into any output in the low state	SN54LVTH162245 (B port)		96	mA
		SN74LVTH162245 (B port)		128	
		A port		30	
I_O	Current into any output in the high state[3]	SN54LVTH162245 (B port)		48	mA
		SN74LVTH162245 (B port)		64	
		A port		30	
I_{IK}	Input clamp current	V_I < 0		−50	mA
I_{OK}	Output clamp current	V_O < 0		−50	mA
θ_{JA}	Package thermal impedance[4]	DGG package		70	°C/W
		DL package		63	
		GQL/ZQL package		42	
		GRD/ZRD package		36	
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This current flows only when the output is in the high state and V_O > V_{CC}.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions[1]

			SN54LVTH162245		SN74LVTH162245		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current	A port		−12		−12	mA
		B port		−24		−32	
I_{OL}	Low-level output current	A port		12		12	mA
		B port		48		64	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		µs/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH162245 MIN	TYP[1]	MAX	SN74LVTH162245 MIN	TYP[1]	MAX	UNIT
V_{IK}		V_{CC} = 2.7 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	A port	V_{CC} = 2.7 V to 3.6 V,	I_{OH} = −100 μA	V_{CC} − 0.2			V_{CC} − 0.2			V
		V_{CC} = 3 V,	I_{OH} = −12 mA	2			2			
	B port	V_{CC} = 2.7 V to 3.6 V,	I_{OH} = −100 μA	V_{CC} − 0.2			V_{CC} − 0.2			
		V_{CC} = 2.7 V,	I_{OH} = −8 mA	2.4			2.4			
		V_{CC} = 3 V	I_{OH} = −24 mA	2						
			I_{OH} = −32 mA				2			
V_{OL}	A port	V_{CC} = 2.7 V to 3.6 V,	I_{OL} = 100 μA			0.2			0.2	V
		V_{CC} = 3 V,	I_{OL} = 12 mA			0.8			0.8	
	B port	V_{CC} = 2.7 V	I_{OL} = 100 μA			0.2			0.2	
			I_{OL} = 24 mA			0.5			0.5	
		V_{CC} = 3 V	I_{OL} = 16 mA			0.4			0.4	
			I_{OL} = 32 mA			0.5			0.5	
			I_{OL} = 48 mA			0.55				
			I_{OL} = 64 mA						0.55	
I_I	Control inputs	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1			±1	μA
		V_{CC} = 0 or 3.6 V,	V_I = 5.5 V			10			10	
	A or B port[2]	V_{CC} = 3.6 V	V_I = 5.5 V			20			20	
			V_I = V_{CC}			5			5	
			V_I = 0			−10			−10	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V						±100	μA
$I_{I(hold)}$	A or B port	V_{CC} = 3 V	V_I = 0.8 V	75			75			μA
			V_I = 2 V	−75			−75			
		V_{CC} = 3.6 V,[3]	V_I = 0 to 3.6 V						500 −750	
I_{OZPU}		V_{CC} = 0 to 1.5 V, V_O = 0.5 V to 3 V, $\overline{OE}$ = don't care				±100[4]			±100	μA
I_{OZPD}		V_{CC} = 1.5 V to 0, V_O = 0.5 V to 3 V, $\overline{OE}$ = don't care				±100[4]			±100	μA
I_{CC}		V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			0.19			0.19	mA
			Outputs low			5			5	
			Outputs disabled			0.19			0.19	
ΔI_{CC}[5]		V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND				0.3			0.2	mA
C_I		V_I = 3 V or 0			4			4		pF
C_{io}		V_O = 3 V or 0			10			10		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) Unused pins at V_{CC} or GND
(3) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
(4) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(5) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

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Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH162245				SN74LVTH162245						UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V			
			MIN	MAX	MIN	MAX	MIN	TYP[1]	MAX	MIN	MAX	
t_{PLH}	A	B	1	3.5		4	1	2.3	3.3		3.7	ns
t_{PHL}			1	3.5		3.9	1	2.2	3.3		3.5	
t_{PLH}	B	A	1	4.3		5.3	1	2.8	4		4.6	ns
t_{PHL}			1	4.2		4.5	1	2.5	3.4		3.6	
t_{PZH}	$\overline{OE}$	B	1	4.8		5.9	1	2.8	4.6		5.4	ns
t_{PZL}			1	4.8		5.5	1	3	4.6		5.2	
t_{PZH}	$\overline{OE}$	A	1	5.5		7.2	1	3.3	5.3		6.3	ns
t_{PZH}			1	5.4		6.4	1	3.3	5.1		5.8	
t_{PHZ}	$\overline{OE}$	B	1.5	5.5		5.8	1.5	3.8	5.2		5.5	ns
t_{PLZ}			1.5	5.5		5.8	1.5	3.5	5.1		5.4	
t_{PHZ}	$\overline{OE}$	A	1.5	5.8		6.5	1.5	4	5.6		5.9	ns
t_{PLZ}			1.2	6.3		6.3	1.5	3.8	5.5		5.5	
$t_{sk(LH)}$									0.5			ns
$t_{sk(HL)}$									0.5			

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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PARAMETER MEASUREMENT INFORMATION
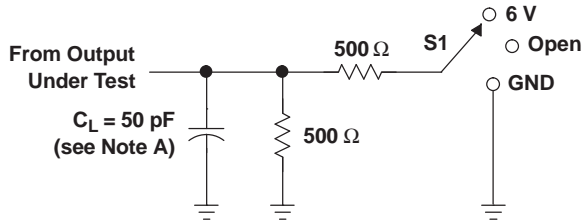
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND
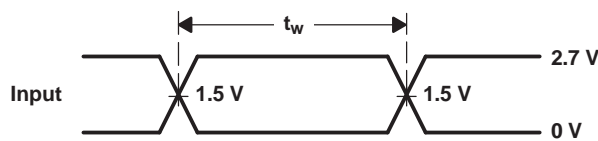
Figure 1. Load Circuit and Voltage Waveforms
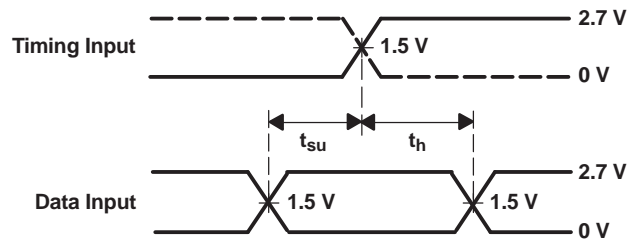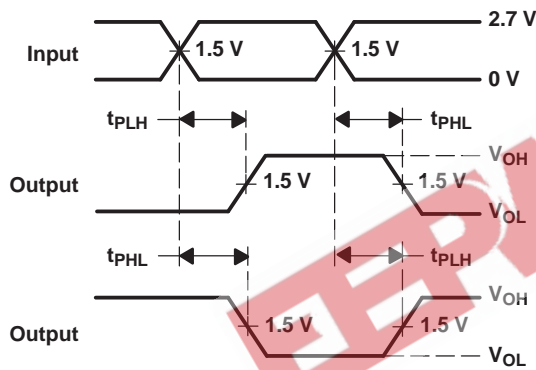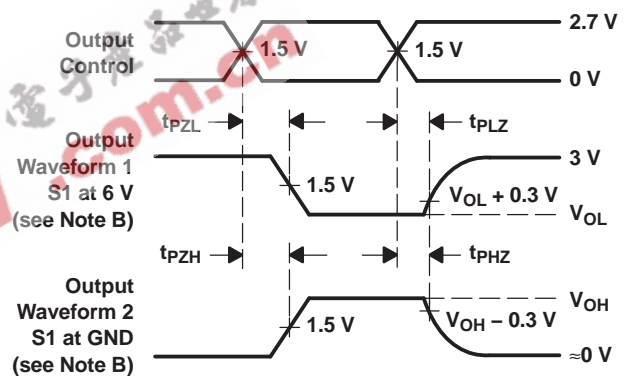
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
5962-9678001QXA	ACTIVE	CFP	WD	48	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9678001VXA	ACTIVE	CFP	WD	48	1	TBD	A42 SNPB	N / A for Pkg Type
74LVTH162245DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVTH162245DLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVTH162245GRDR	ACTIVE	BGA MICROSTAR JUNIOR	GRD	54	1000	TBD	SNPB	Level-1-240C-UNLIM
74LVTH162245GRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVTH162245ZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
74LVTH162245ZRDR	ACTIVE	BGA MICROSTAR JUNIOR	ZRD	54	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
SN74LVTH162245DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH162245DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH162245DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH162245DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH162245KR	ACTIVE	BGA MICROSTAR JUNIOR	GQL	56	1000	TBD	SNPB	Level-1-240C-UNLIM
SNJ54LVTH162245WD	ACTIVE	CFP	WD	48	1	TBD	A42 SNPB	N / A for Pkg Type

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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WD (R-GDFP-F**)

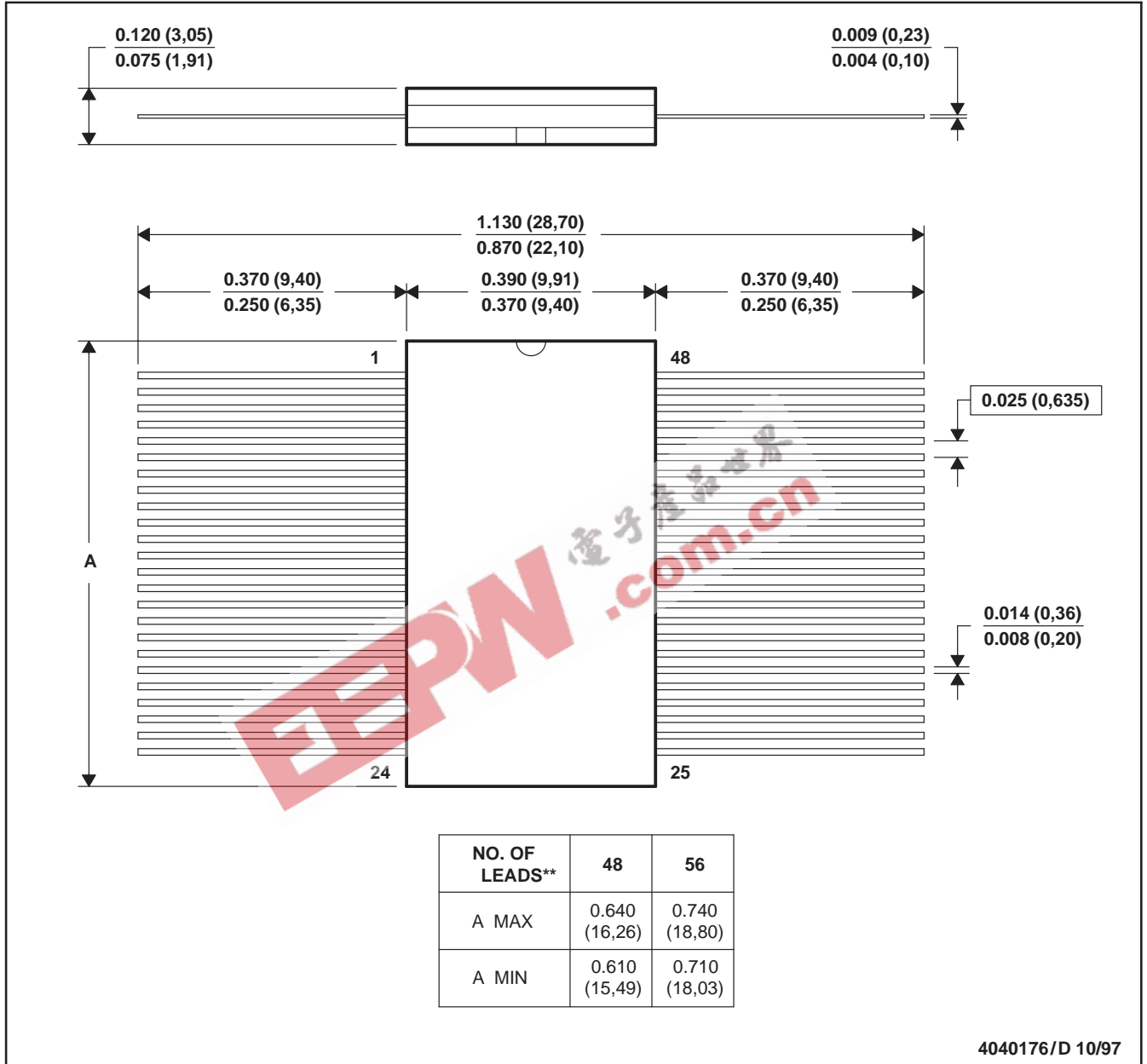## CERAMIC DUAL FLATPACK

48 LEADS SHOWN

0.120 (3,05) / 0.075 (1,91)

0.009 (0,23) / 0.004 (0,10)

1.130 (28,70) / 0.870 (22,10)

0.370 (9,40) / 0.250 (6,35)

0.390 (9,91) / 0.370 (9,40)

0.370 (9,40) / 0.250 (6,35)

0.025 (0,635)

0.014 (0,36) / 0.008 (0,20)

1   48

A

24   25

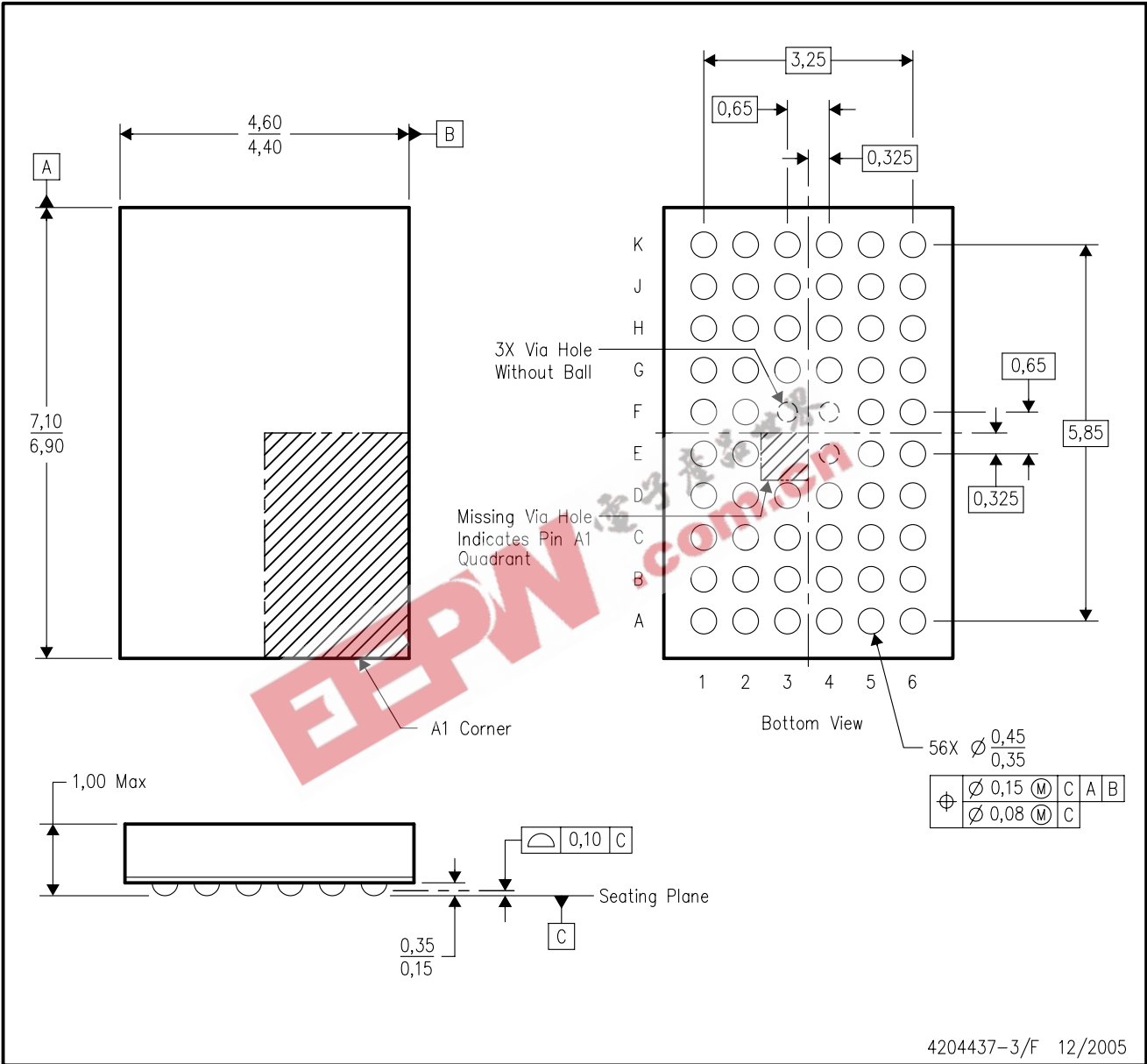| NO. OF LEADS**	48	56
A MAX	0.640 (16,26)	0.740 (18,80)
A MIN	0.610 (15,49)	0.710 (18,03)

4040176 / D 10/97

NOTES:
  A. All linear dimensions are in inches (millimeters).
  B. This drawing is subject to change without notice.
  C. This package can be hermetically sealed with a ceramic lid using glass frit.
  D. Index point is provided on cap for terminal identification only
  E. Falls within MIL STD 1835:   GDFP1-F48 and JEDEC MO-146AA
                                      GDFP1-F56 and JEDEC MO-146AB

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

ZQL (R-PBGA-N56)   PLASTIC BALL GRID ARRAY

4204437-3/F   12/2005
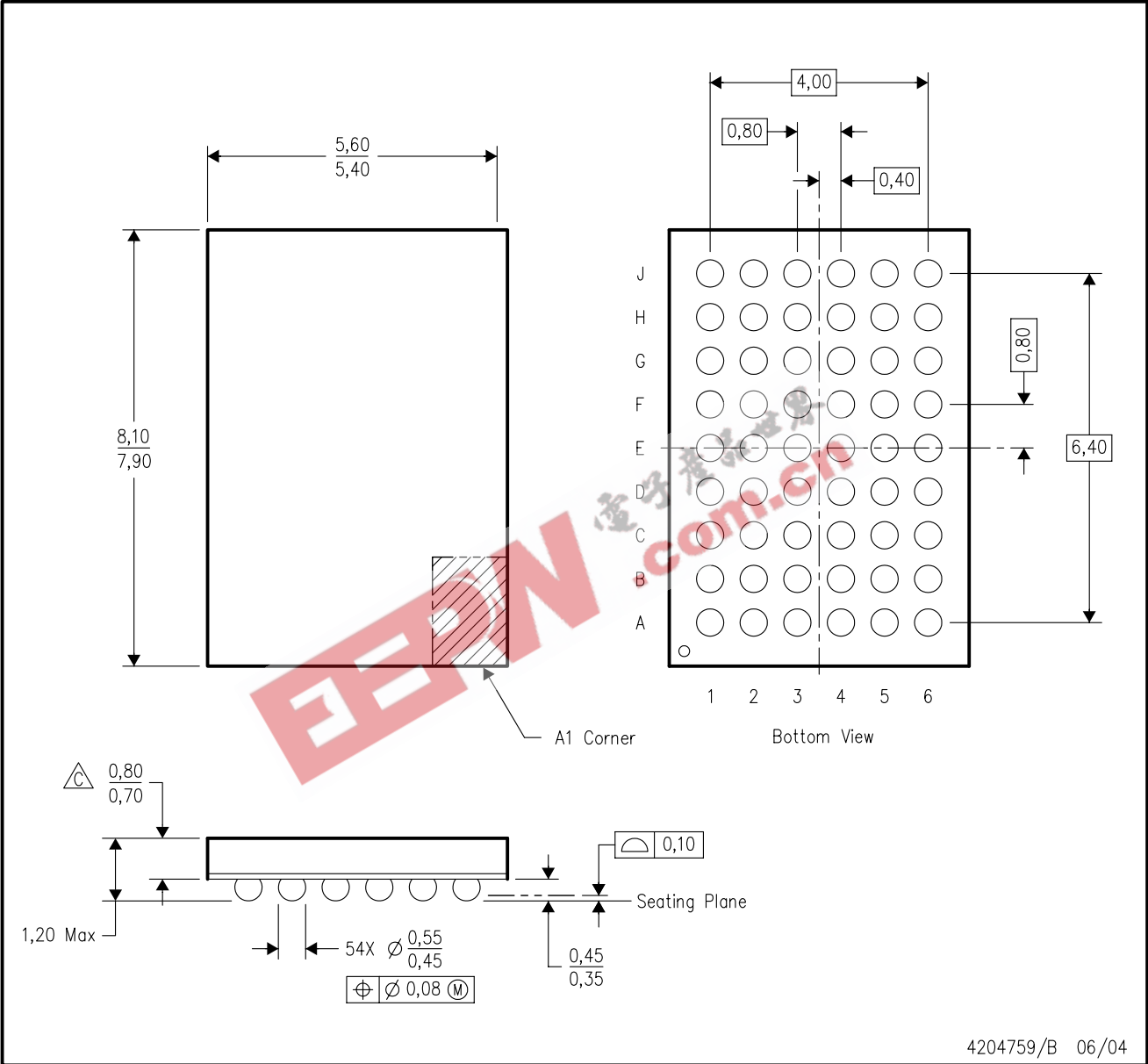
NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
         B.   This drawing is subject to change without notice.
         C.   Falls within JEDEC MO-225 variation BA.
         D.   This package is lead-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

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GRD (R−PBGA−N54)   PLASTIC BALL GRID ARRAY

4,00

0,80

0,40

5,60
5,40

8,10
7,90

0,80

6,40

J H G F E D C B A

1 2 3 4 5 6

Bottom View

A1 Corner

0,80
0,70

0,10

Seating Plane

1,20 Max
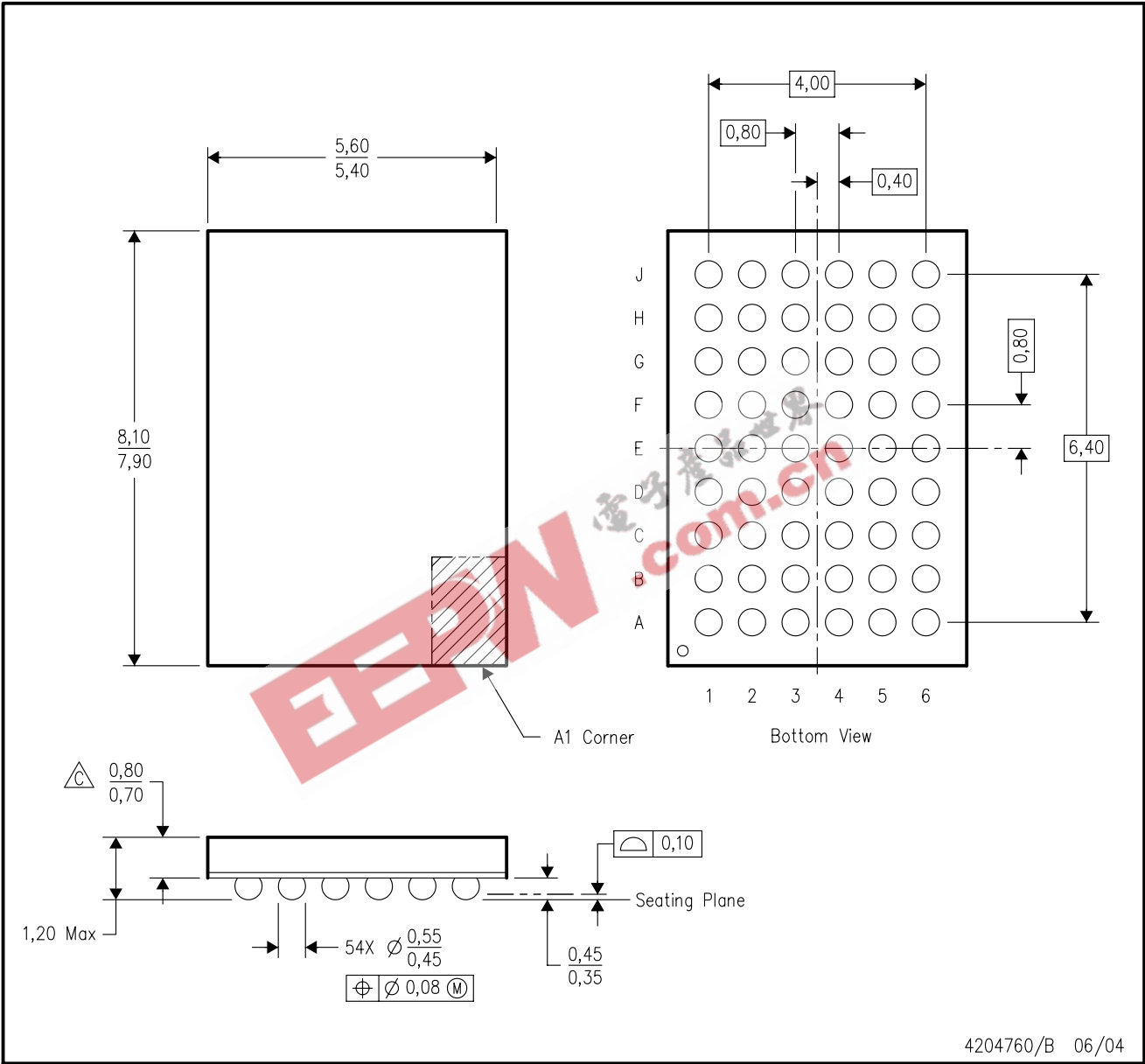
54X ∅ 0,55
0,45

0,45
0,35

⊕ ∅ 0,08 Ⓜ

4204759/B 06/04
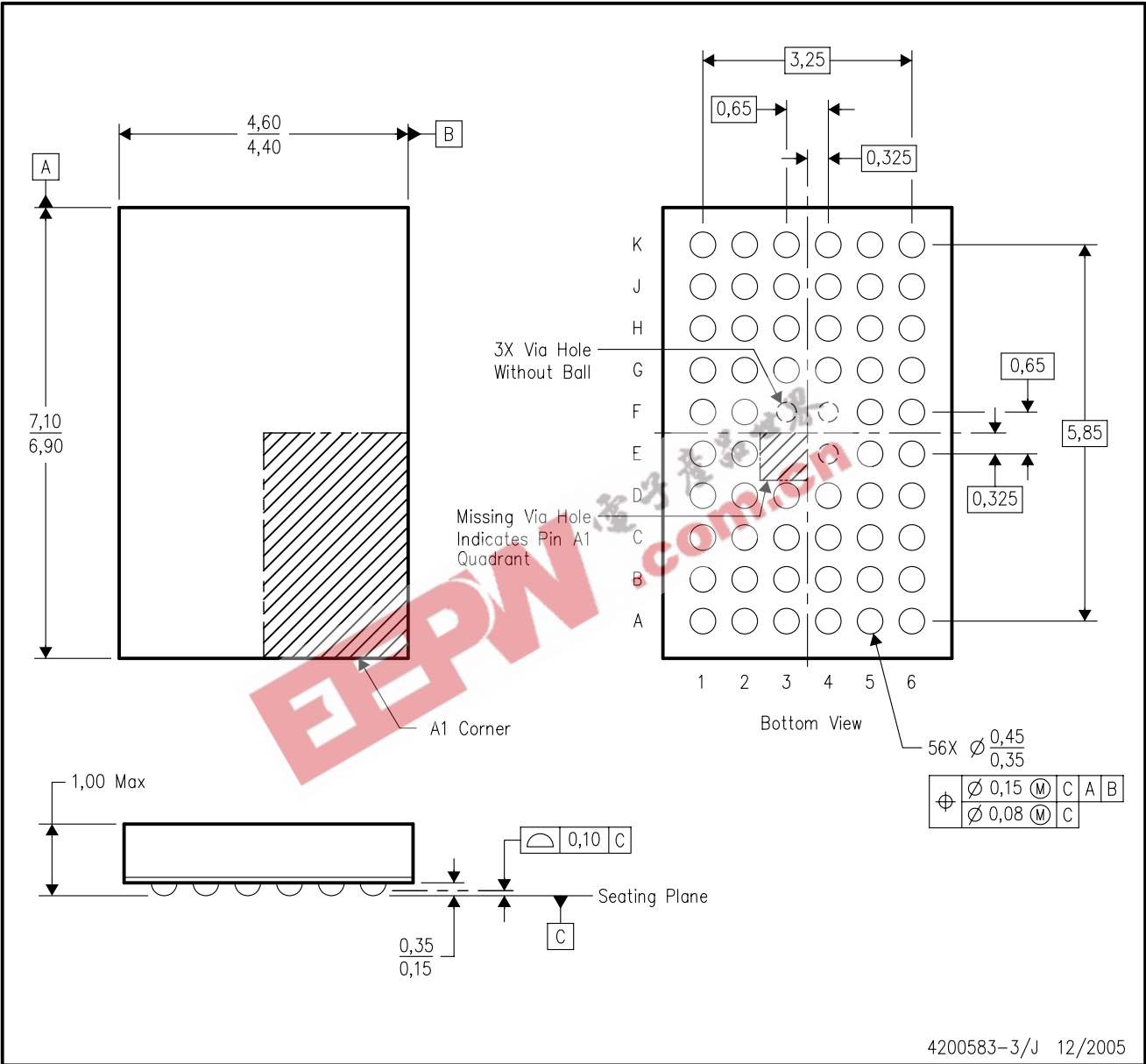
NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Falls within JEDEC MO−205 variation DD.
        D. This package is tin−lead (SnPb). Refer to the 54 ZRD package (drawing 4204760) for lead−free.

ZRD (R–PBGA–N54)   PLASTIC BALL GRID ARRAY

4,00

0,80

0,40

5,60
5,40

8,10
7,90

0,80

6,40

J
H
G
F
E
D
C
B
A

1   2   3   4   5   6

Bottom View

A1 Corner

$\triangle$ C
0,80
0,70

0,10

Seating Plane

1,20 Max

54X $\varnothing$ 0,55
0,45

0,45
0,35

$\oplus$ $\varnothing$ 0,08 Ⓜ

4204760/B   06/04

NOTES: A.   All linear dimensions are in millimeters.
   B.   This drawing is subject to change without notice.
   $\triangle$C   Falls within JEDEC MO–205 variation DD.
   D.   This package is lead–free. Refer to the 54 GRD package (drawing 4204759) for tin–lead (SnPb).

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GQL (R−PBGA−N56)   PLASTIC BALL GRID ARRAY

3,25

0,65

0,325

K
J
H

3X Via Hole
Without Ball

G
F

0,65

E

5,85

D

0,325

C

Missing Via Hole
Indicates Pin A1
Quadrant

B
A

1   2   3   4   5   6

Bottom View

A1 Corner

56X Ø 0,45 / 0,35

⌖ Ø 0,15 Ⓜ C A B
  Ø 0,08 Ⓜ C

4,60 / 4,40   B

A

7,10 / 6,90

1,00 Max

⌒ 0,10 C

Seating Plane

0,35 / 0,15

C

4200583−3/J 12/2005

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        C. Falls within JEDEC MO−225 variation BA.
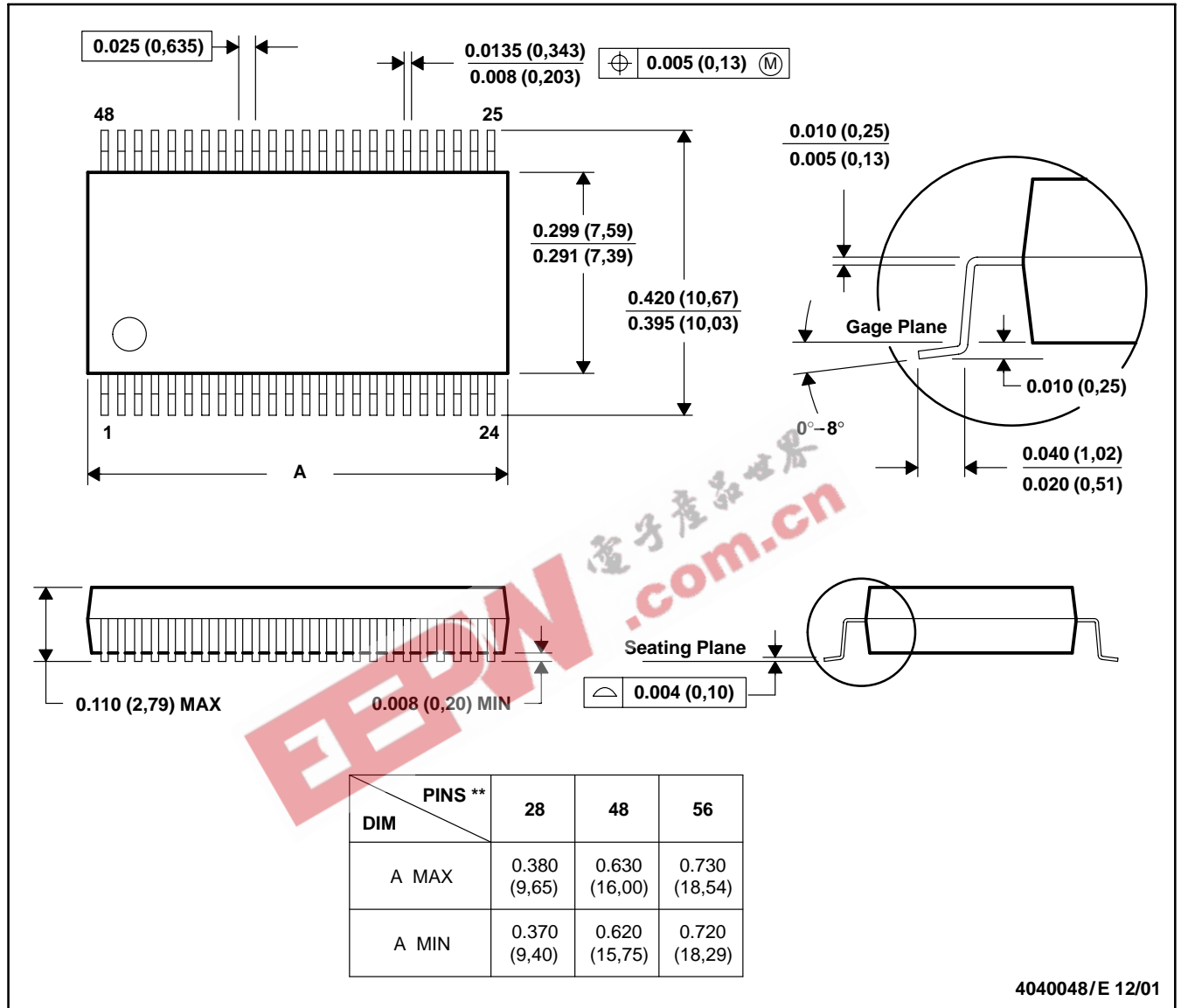   D. This package is tin−lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead−free.

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DL (R-PDSO-G**)   PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

PINS ** DIM	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048 / E 12/01

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
        D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**
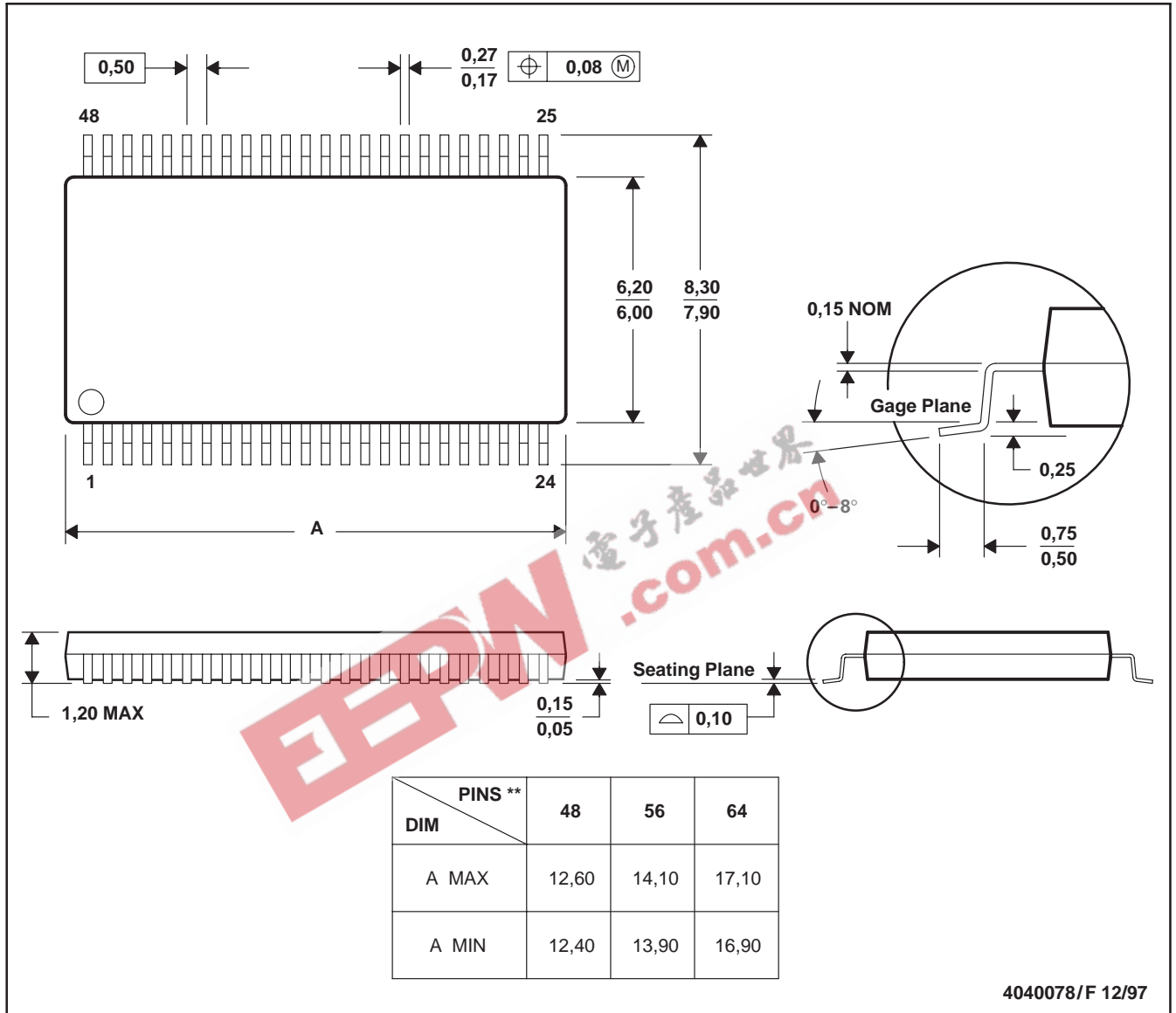
48 PINS SHOWN

PINS ** DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold protrusion not to exceed 0,15.
        D. Falls within JEDEC MO-153

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