

Octal transceiver/register, non-inverting (3-State)

74ABT652A

FEATURES

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- 3-State outputs
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT652A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT652A transceiver/register consists of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable (OEAB, $\overline{\text{OEBA}}$) and Select (SAB, SBA) pins are provided for bus management.

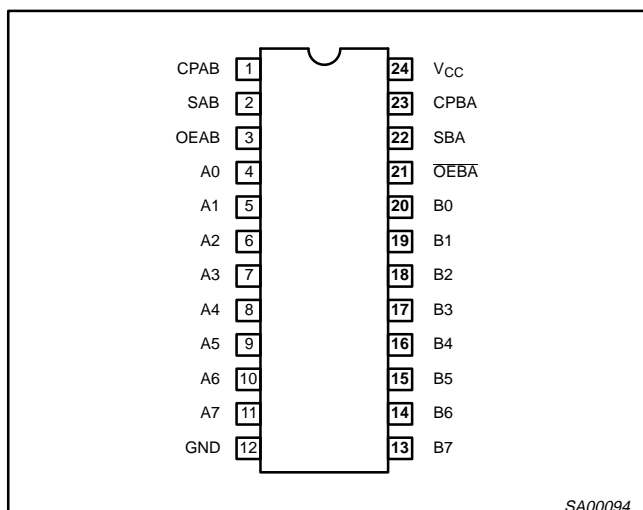
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{\text{amb}} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPBA to An or CPAB to Bn	$C_L = 50\text{pF}; V_{\text{CC}} = 5\text{V}$	3.7 4.3	ns
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}	4	pF
$C_{\text{I/O}}$	I/O capacitance	Outputs disabled; $V_O = 0\text{V}$ or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; $V_{\text{CC}} = 5.5\text{V}$	110	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24-pin plastic DIP	-40°C to $+85^{\circ}\text{C}$	74ABT652AN	SOT222-1
24-pin plastic SOL	-40°C to $+85^{\circ}\text{C}$	74ABT652AD	SOT137-1
24-pin plastic SSOP Type II	-40°C to $+85^{\circ}\text{C}$	74ABT652ADB	SOT340-1
24-pin plastic TSSOP Type I	-40°C to $+85^{\circ}\text{C}$	74ABT652APW	SOT355-1

PIN CONFIGURATION



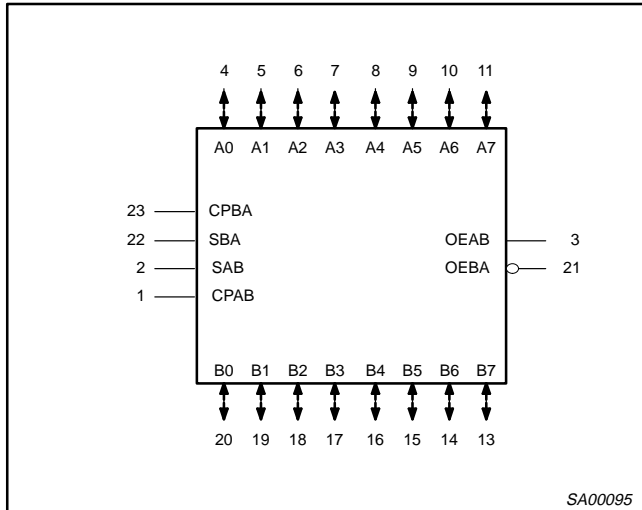
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 23	CPAB / CPBA	A to B clock input / B to A clock input
2, 22	SAB / SBA	A to B select input / B to A select input
3, 21	OEAB / OEBA	A to B Output Enable input / B to A Output Enable input (active-Low)
4, 5, 6, 7, 8, 9, 10, 11	A0 – A7	Data inputs/outputs (A side)
20, 19, 18, 17, 16, 15, 14, 13	B0 – B7	Data inputs/outputs (B side)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

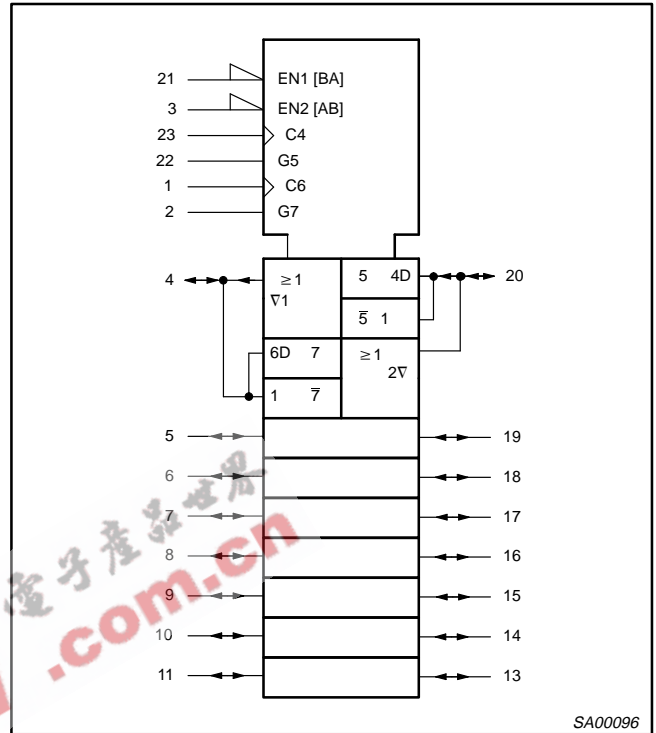
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LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
OEAB	OEBA	CPAB	CPBA	SAB	SBA	An	Bn	
L	H	H or L	H or L	X	X	Input	Input	Isolation Store A and B data
L	H	↑	↑	X	X	Input	Input	Store A, Hold B Store A in both registers
X	H	↑	H or L	X	X	Input	Unspecified output*	Store A, Hold B Store A in both registers
H	H	↑	↑	**	X	Input	Unspecified output*	Store A, Hold B Store A in both registers
L	X	H or L	↑	X	X	Unspecified output*	Input	Hold A, Store B Store B in both registers
L	L	↑	↑	X	X	Unspecified output*	Input	Hold A, Store B Store B in both registers
L	L	X	X	X	L	Output	Input	Real time B data to A bus Stored B data to A bus
L	L	X	H or L	X	H	Output	Input	Real time B data to A bus Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real time A data to B bus Store A data to B bus
H	H	H or L	X	H	X	Input	Output	Real time A data to B bus Store A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus Stored B data to A bus

H = High voltage level

L = Low voltage level

X = Don't care

↑ = Low-to-High clock transition

* The data output function may be enabled or disabled by various signals at the OEBA and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

** If both Select controls (SAB and SBA) are Low, then clocks can occur simultaneously. If either Select control is High, the clocks must be staggered in order to load both registers.

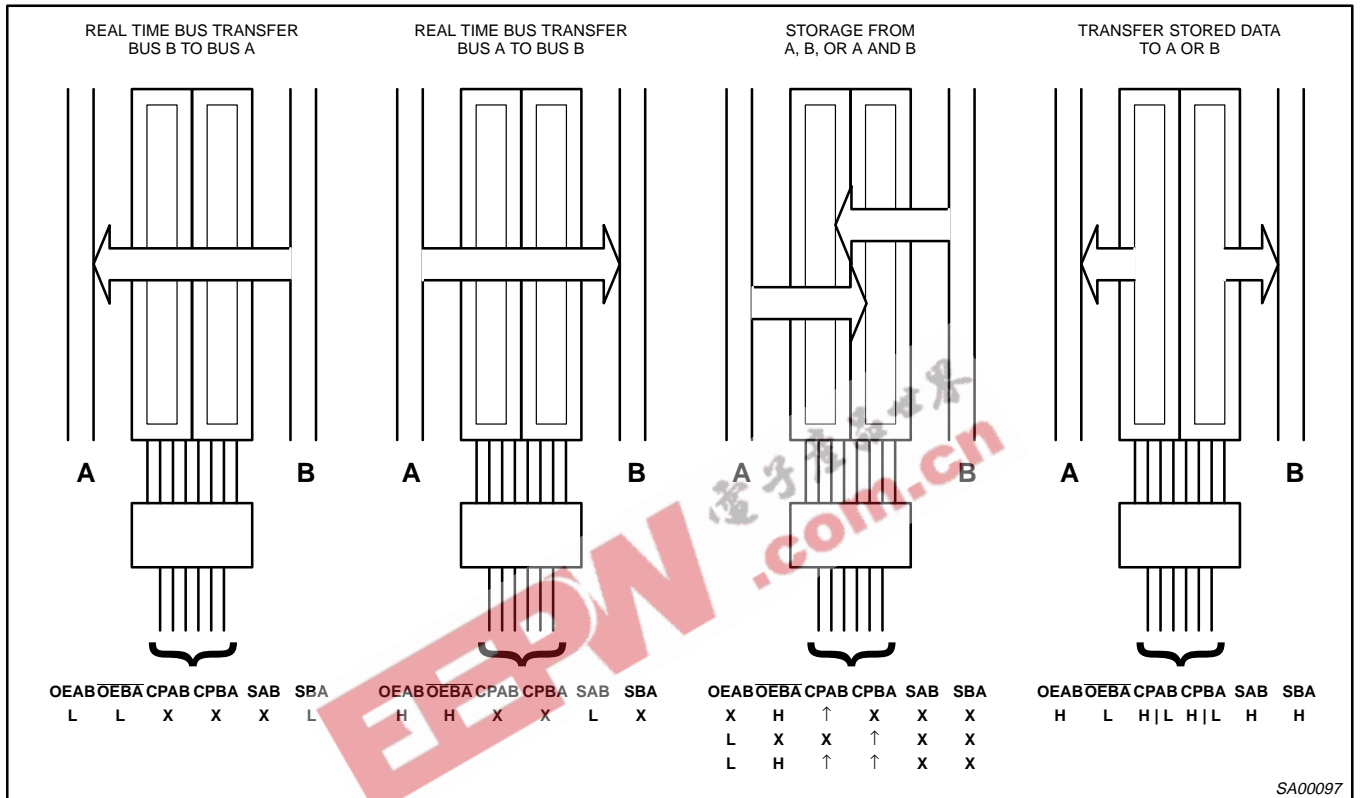
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The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74ABT652A.

The select pins determine whether data is stored or transferred through the device in real time.

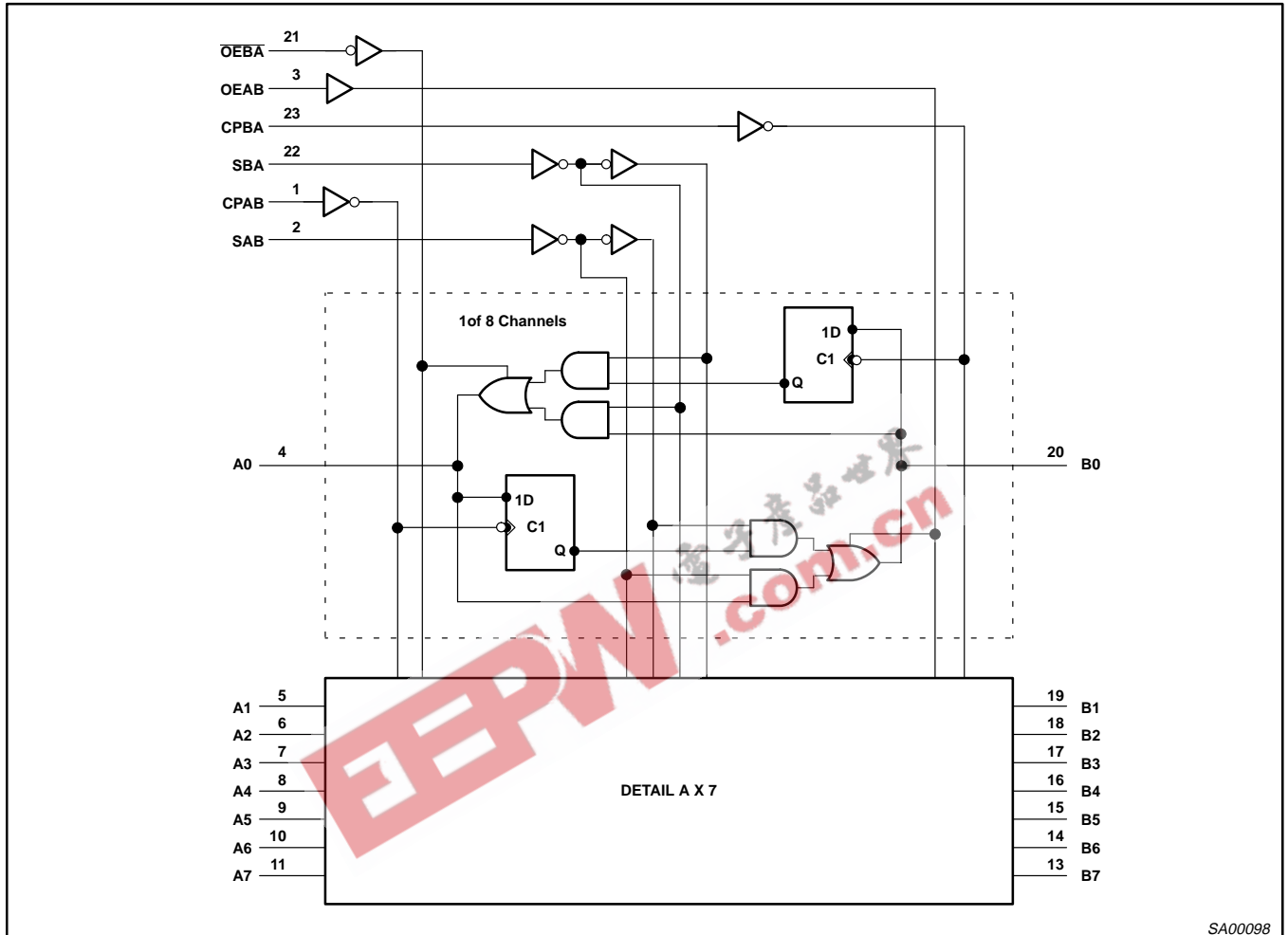
The output enable pins determine the direction of the data flow.



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LOGIC DIAGRAM



SA00098

ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0	-18	mA
V _I	DC input voltage ³		-1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	-50	mA
V _{OUT}	DC output voltage ³	output in Off or High state	-0.5 to +5.5	V
I _{OUT}	DC output current	output in Low state	128	mA
T _{stg}	Storage temperature range		-65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		-32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_{amb} = +25^\circ\text{C}$			$T_{amb} = -40^\circ\text{C}$ to $+85^\circ\text{C}$		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	$V_{CC} = 4.5\text{V}; I_{IK} = -18\text{mA}$		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage	$V_{CC} = 4.5\text{V}; I_{OH} = -3\text{mA}; V_I = V_{IL}$ or V_{IH}	2.5	3.0		2.5		V
		$V_{CC} = 5.0\text{V}; I_{OH} = -3\text{mA}; V_I = V_{IL}$ or V_{IH}	3.0	3.5		3.0		V
		$V_{CC} = 4.5\text{V}; I_{OH} = -32\text{mA}; V_I = V_{IL}$ or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	$V_{CC} = 4.5\text{V}; I_{OL} = 64\text{mA}; V_I = V_{IL}$ or V_{IH}		0.3	0.55		0.55	V
V_{RST}^3	Power-up output low voltage	$V_{CC} = 5.5\text{V}; I_O = 1\text{mA}; V_I = \text{GND}$ or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	Control pins		± 0.01	± 1.0		± 1.0	μA
		Data pins		± 5	± 100		± 100	μA
I_{OFF}	Power-off leakage current	$V_{CC} = 0.0\text{V}; V_O$ or $V_I \leq 4.5\text{V}$		± 5.0	± 100		± 100	μA
I_{PU}/I_{PD}	Power-up/down 3-State output current ⁴	$V_{CC} = 2.1\text{V}; V_O = 0.5\text{V}; V_I = \text{GND}$ or V_{CC} ; $V_{OE} = \text{Don't care}; \overline{V_{OE}} = \text{Don't care}$		± 5.0	± 50		± 50	μA
$I_{IH} + I_{OZH}$	3-State output High current	$V_{CC} = 5.5\text{V}; V_O = 2.7\text{V}; V_I = V_{IL}$ or V_{IH}		5.0	50		50	μA
$I_{IL} + I_{OZL}$	3-State output Low current	$V_{CC} = 5.5\text{V}; V_O = 0.5\text{V}; V_I = V_{IL}$ or V_{IH}		-5.0	-50		-50	μA
I_{CEX}	Output High leakage current	$V_{CC} = 5.5\text{V}; V_O = 5.5\text{V}; V_I = \text{GND}$ or V_{CC}		5.0	50		50	μA
I_O	Output current ^{1, 5}	$V_{CC} = 5.5\text{V}; V_O = 2.5\text{V}$	-40	-65	-180	-40	-180	mA
I_{CCH}	Quiescent supply current	$V_{CC} = 5.5\text{V}; \text{Outputs High}, V_I = \text{GND}$ or V_{CC}		110	250		250	μA
I_{CCL}		$V_{CC} = 5.5\text{V}; \text{Outputs Low}, V_I = \text{GND}$ or V_{CC}		20	30		30	mA
I_{CCZ}		$V_{CC} = 5.5\text{V}; \text{Outputs 3-State}; V_I = \text{GND}$ or V_{CC}		110	250		250	μA
ΔI_{CC}	Additional supply current per input pin ²	$V_{CC} = 5.5\text{V}; \text{one input at } 3.4\text{V}, \text{other inputs at } V_{CC}$ or $\text{GND}; V_{CC} = 5.5\text{V}$		0.3	1.5		1.5	mA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From $V_{CC} = 2.1\text{V}$ to $V_{CC} = 5\text{V} \pm 10\%$, a transition time of up to 100 μsec is permitted.
- This data sheet limit may vary among suppliers.

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AC CHARACTERISTICS

GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$			$T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	125	300		125		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB to Bn or CPBA to An	1	2.2 1.7	3.7 4.3	5.1 5.1	2.2 1.7	5.6 5.6	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	1.5 1.5	3.0 3.6	4.3 4.6	1.5 1.5	4.8 5.4	ns
t_{PLH} t_{PHL}	Propagation delay SAB to Bn or SBA to An	3	1.5 1.5	3.5 4.2	5.1 5.2 ¹	1.5 1.5	6.5 5.9	ns
t_{PZH} t_{PZL}	Output enable time OEBA to An	5 6	2 3	3.2 4.5	4.6 6.8	2 3	5.8 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time OEBA to An	5 6	1.5 1.5	3.9 2.9	4.7 ¹ 3.8	1.5 1.5	5.3 ¹ 4.1	ns
t_{PZH} t_{PZL}	Output enable time OEAB to Bn	5 6	2 3	3.5 4.7	6.1 6.5	2 3	6.5 7.4	ns
t_{PHZ} t_{PLZ}	Output disable time OEAB to Bn	5 6	1.5 1.5	3.8 3.0	4.6 ¹ 4.4	1.5 1.5	5.5 5.1	ns

1. This data sheet limit may vary among suppliers.

AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

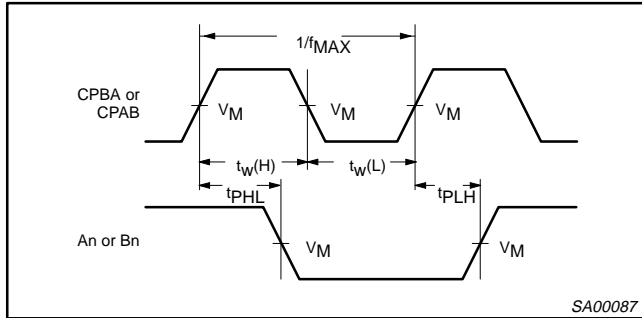
SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$		$T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$		
			Min	Typ	Min	Max	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time An to CPAB, Bn to CPBA	4	3.0 3.0	0.7 0.7	3.0 3.0		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time An to CPAB, Bn to CPBA	4	0.0 0.0	-0.5 -0.5	0.0 0.0		ns
$t_w(\text{H})$ $t_w(\text{L})$	Pulse width, High or Low CPAB or CPBA	1	4.0 4.0	1.0 1.0	4.0 4.0		ns

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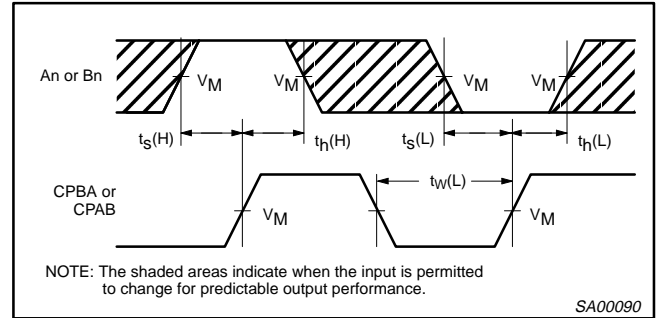
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AC WAVEFORMS

$V_M = 1.5V, V_{IN} = GND \text{ to } 3.0V$

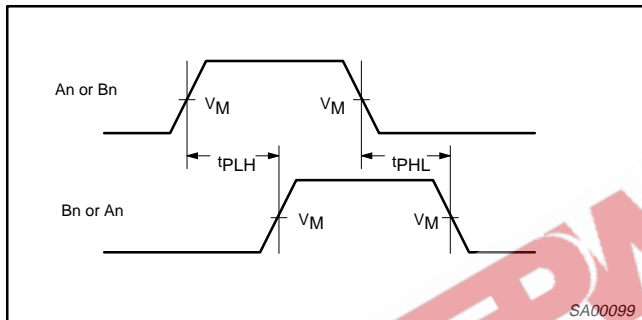


Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

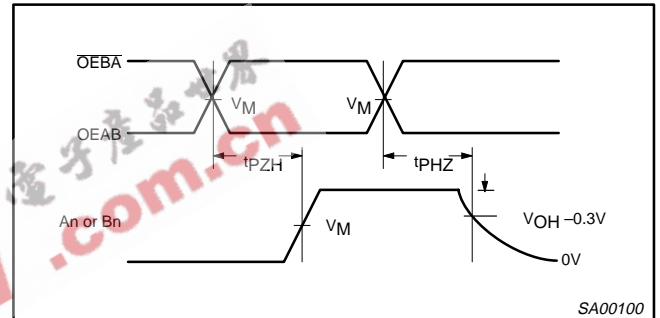


NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

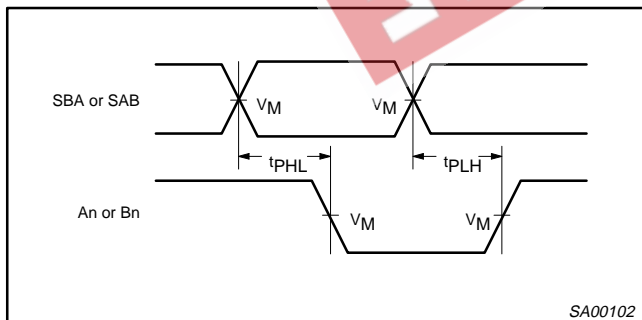
Waveform 4. Data Setup and Hold Times



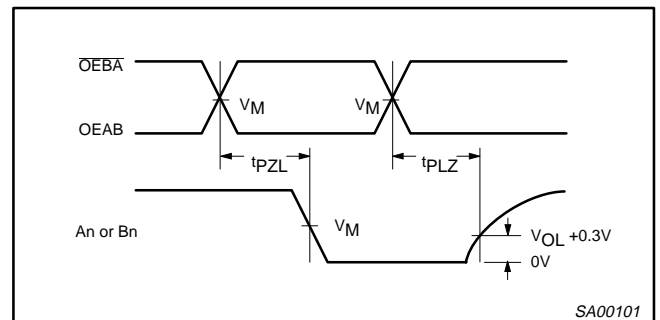
Waveform 2. Propagation Delay, An to Bn or Bn to An



Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 3. Propagation Delay, SBA to An or SAB to Bn



Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

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TEST CIRCUIT AND WAVEFORM

Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

$V_M = 1.5V$

INPUT PULSE REQUIREMENTS					
FAMILY	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012