FAIRCHILD

SEMICONDUCTOR®

March 1997
Revised April 2005

74VHCT244A
Octal Buffer/Line Driver with 3-STATE Outputs

General Description

The VHCT244A is an advanced high speed CMOS octal bus transceiver fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The VHCT244A is a non-inverting 3-STATE buffer having two active-LOW output enables. This device is designed to be used as 3-STATE memory address drivers, clock drivers, and bus oriented transmitter/receivers.

Protection circuits ensure that 0V to 7V can be applied to the input and output (Note 1) pins without regard to the supply voltage. These circuits prevent device destruction due to mismatched supply and input/output voltages. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up.

**Note 1:** Outputs in OFF-State

Features

■ High Speed: t_{PD} = 5.9 ns (typ) at V_{CC} = 5V

■ Power down protection is provided on inputs and outputs

■ Low power dissipation: I_{CC} = 4 μA (max) @ T_A = 25°C

■ Pin and function compatible with 74HCT244

Ordering Code:

Order Number	Package Number	Package Description
74VHCT244AM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74VHCT244ASJ	M20D	Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHCT244AMTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHCT244AN	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Logic Symbol
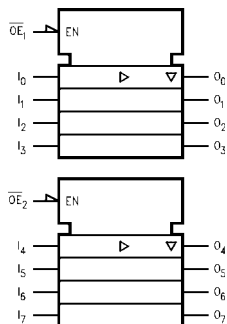
Connection Diagram

www.fairchildsemi.com
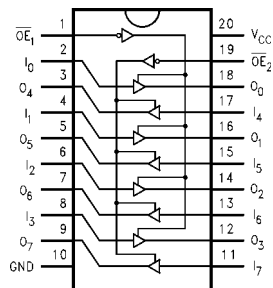
Pin Descriptions

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	3-STATE Output Enable Inputs
I_0–I_7	Inputs
O_0–O_7	3-STATE Outputs

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_n	(Pins 12, 14, 16, 18)
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I_n	(Pins 3, 5, 7, 9)
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
I = Immaterial
Z = High Impedance

Absolute Maximum Ratings(Note 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	
(Note 3)	−0.5V to V_{CC} + 0.5V
(Note 4)	−0.5V to +7.0V
Input Diode Current (I_{IK})	−20 mA
Output Diode Current (I_{OK}) (Note 5)	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 6)

Supply Voltage (V_{CC})	4.5V to +5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	
(Note 3)	0V to V_{CC}
(Note 4)	0V to +5.5V
Operating Temperature (T_{OPR})	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 5.0V ± 0.5V	0 ns/V ~ 20 ns/V

Note 2: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

Note 3: HIGH or LOW state. I_{OUT} absolute maximum rating must be observed.

Note 4: When outputs are in OFF-STATE or when V_{CC} = OV.

Note 5: V_{OUT} < GND, V_{OUT} > V_{CC} (Outputs Active).

Note 6: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = 25°C			T_A = −40°C to +85°C		Units	Conditions
			Min	Typ	Max	Min	Max		
V_{IH}	HIGH Level	4.5	2.0			2.0		V	
	Input Voltage	5.5	2.0			2.0			
V_{IL}	LOW Level	4.5			0.8		0.8	V	
	Input Voltage	5.5			0.8		0.8		
V_{OH}	HIGH Level	4.5	4.40	4.50		4.40		V	V_{IN} = V_{IH} I_{OH} = −50 μA
	Output Voltage		3.94			3.80		V	or V_{IL} I_{OH} = −8 mA
V_{OL}	LOW Level	4.5		0.0	0.1		0.1	V	V_{IN} = V_{IH} I_{OL} = 50 μA
	Output Voltage				0.36		0.44	V	or V_{IL} I_{OL} = 8 mA
I_{OZ}	3-STATE Output Off-State Current	5.5			±0.25		±2.5	μA	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND
I_{IN}	Input Leakage Current	0–5.5			±0.1		±1.0	μA	V_{IN} = 5.5V or GND
I_{CC}	Quiescent Supply Current	5.5			4.0		40.0	μA	V_{IN} = V_{CC} or GND
I_{CCT}	Maximum I_{CC}/Input	5.5			1.35		1.50	mA	V_{IN} = 3.4V Other Input = V_{CC} or GND
I_{OFF}	Output Leakage Current (Power Down State)	0.0			0.5		5.0	μA	V_{OUT} = 5.5V

Noise Characteristics

Symbol	Parameter	V_CC (V)	T_A = 25°C Typ	T_A = 25°C Limits	Units	Conditions
V_OLP (Note 7)	Quiet Output Maximum Dynamic V_OL	5.0	0.9	1.1	V	C_L = 50 pF
V_OLV (Note 7)	Quiet Output Minimum Dynamic V_OL	5.0	−0.9	−1.1	V	C_L = 50 pF
V_IHD (Note 7)	Minimum HIGH Level Dynamic Input Voltage	5.0		2.0	V	C_L = 50 pF
V_ILD (Note 7)	Maximum LOW Level Dynamic Input Voltage	5.0		0.8	V	C_L = 50 pF

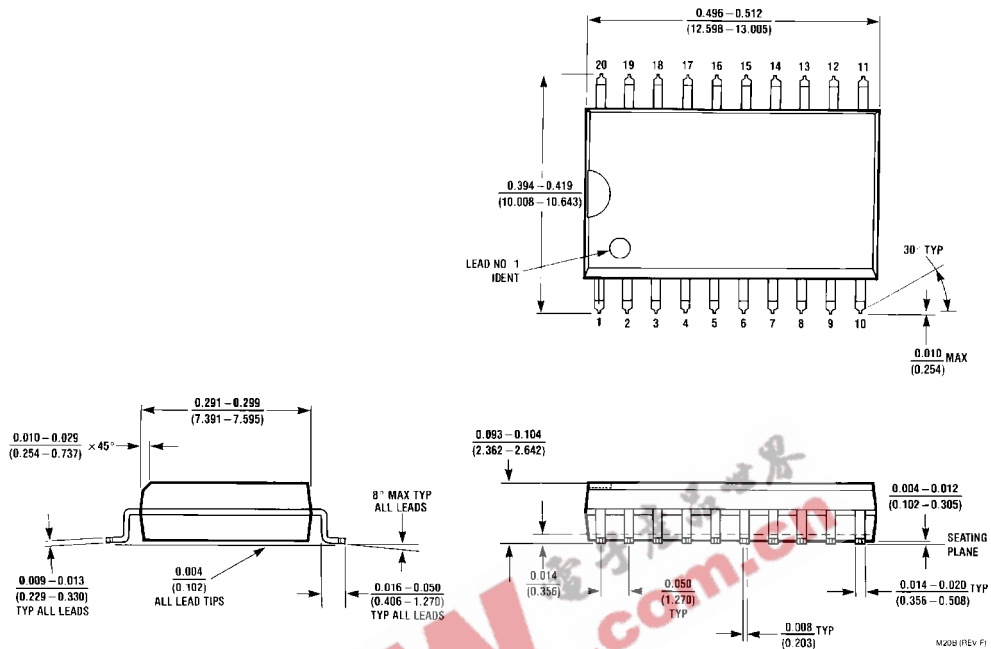**Note 7:** Parameter guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	V_CC (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	T_A = −40°C to +85°C Min	T_A = −40°C to +85°C Max	Units	Conditions	
t_PLH	Propagation Delay	5.0 ± 0.5		5.4	7.4	1.0	8.5	ns		C_L = 15 pF
t_PHL	Time			5.9	8.4	1.0	9.5			C_L = 50 pF
t_PZL	3-STATE Output	5.0 ± 0.5		7.7	10.4	1.0	12.5	ns	R_L = 1 kΩ	C_L = 15 pF
t_PZH	Enable Time			8.2	11.4	1.0	13.5			C_L = 50 pF
t_PLZ t_PHZ	3-STATE Output Disable Time	5.0 ± 0.5		8.8	11.4	1.0	13.0	ns	R_L = 1 kΩ	C_L = 50 pF
t_OSLH t_OSHL	Output to Output Skew	5.0 ± 0.5			1.0		1.0	ns	(Note 8)	
C_IN	Input Capacitance			4	10		10	pF	V_CC = Open	
C_OUT	Output Capacitance			9				pF	V_CC = 5.0V	
C_PD	Power Dissipation Capacitance			18				pF	(Note 9)	

Note 8: Parameter guaranteed by design. $t_{OSLH} = |t_{PLH\,max} - t_{PLH\,min}|$; $t_{OSHL} = |t_{PHL\,max} - t_{PHL\,min}|$

Note 9: C_PD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = $C_{PD} * V_{CC} * f_{IN} + I_{CC}/8$ (per F/F). The total C_{PD} when n pcs. of the Octal D Flip-Flop operates can be calculated by the equation: C_{PD} (total) = 20 + 12n.

Physical Dimensions inches (millimeters) unless otherwise noted

0.496 − 0.512
(12.598 − 13.005)

20 19 18 17 16 15 14 13 12 11

0.394 − 0.419
(10.008 − 10.643)

LEAD NO. 1
IDENT

30° TYP

0.010 MAX
(0.254)

1 2 3 4 5 6 7 8 9 10

0.291 − 0.299
(7.391 − 7.595)

0.010 − 0.029
(0.254 − 0.737) × 45°

8° MAX TYP
ALL LEADS

0.093 − 0.104
(2.362 − 2.642)

0.004 − 0.012
(0.102 − 0.305)

SEATING
PLANE

0.009 − 0.013
(0.229 − 0.330)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.014
(0.356)

0.050
(1.270)
TYP

0.014 − 0.020 TYP
(0.356 − 0.508)

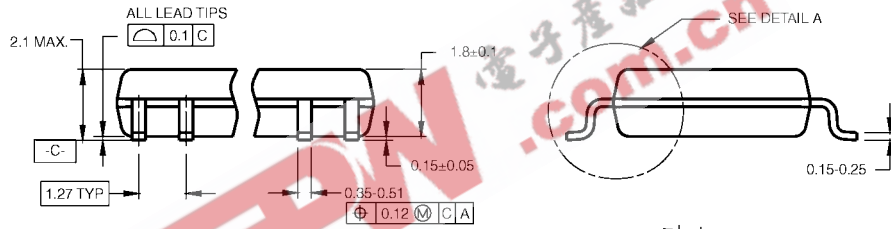0.008 TYP
(0.203)

M20B (REV F)

**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

12.6±0.10
-A-
0.40 TYP
20
11
7.8
3.9
5.3±0.10
-B-
PIN #1 IDENT.
1
10
△ 0.2 C B A
ALL LEAD TIPS

20 19   12 11
5.01 TYP
9.27 TYP
(2.13 TYP)
1   2   9   10
1.27 TYP   0.6 TYP

LAND PATTERN RECOMMENDATION

ALL LEAD TIPS
△ 0.1 C
2.1 MAX.
-C-
1.27 TYP
0.35-0.51
⊕ 0.12 Ⓜ C A
DIMENSIONS ARE IN MILLIMETERS

1.8±0.1
SEE DETAIL A
0.15±0.05
0.15-0.25
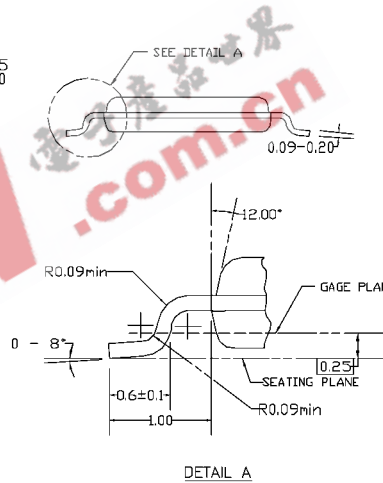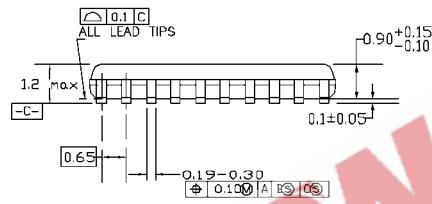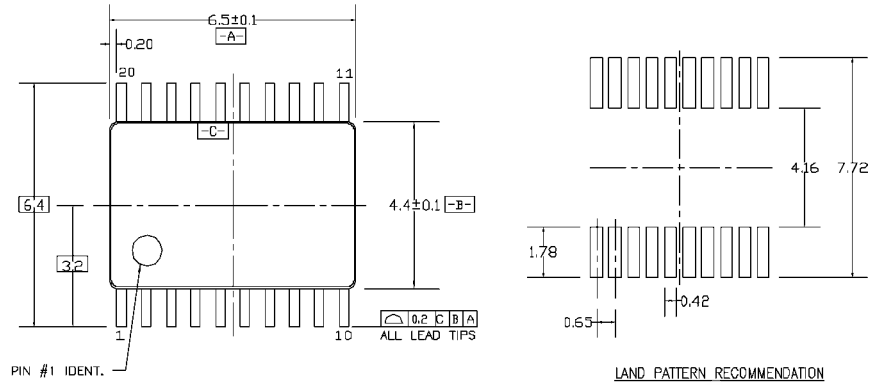
NOTES:
A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

7° TYP
GAGE PLANE
0°-8° TYP
0.25
0.60±0.15
1.25
SEATING PLANE

DETAIL A

Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

6.5±0.1
-A-

-0.20

20   11

-C-

6,4   4.4±0.1 -B-

3,2

1   10

□ 0.2 C B A
ALL LEAD TIPS

PIN #1 IDENT.

4.16   7.72

1.78

0.65   0.42

0.65

LAND PATTERN RECOMMENDATION

□ 0.1 C
ALL LEAD TIPS

0.90 +0.15 -0.10

1.2 max

-C-

0.1±0.05

0.65

0.19-0.30

⊕ 0.10 Ⓜ A B Ⓢ C Ⓢ

DIMENSIONS ARE IN MILLIMETERS

SEE DETAIL A

0.09-0.20

12.00°

R0.09min   GAGE PLANE

0 - 8°

0.25

SEATING PLANE

0.6±0.1   R0.09min

1.00

DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A

N20A (REV G)

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com