



# 74ACT16373

## 16-BIT D-TYPE LATCH WITH 3-STATE OUTPUTS (NON INVERTED)

- HIGH SPEED:  $t_{PD} = 5.3\text{ns}$  (TYP.) at  $V_{CC} = 5\text{V}$
- LOW POWER DISSIPATION:  
 $I_{CC} = 8\mu\text{A}$ (MAX.) at  $T_A=25^\circ\text{C}$
- COMPATIBLE WITH TTL OUTPUTS  
 $V_{IH} = 2\text{V}$  (MIN.),  $V_{IL} = 0.8\text{V}$  (MAX.)
- $50\Omega$  TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 24\text{mA}$  (MIN)
- OPERATING VOLTAGE RANGE:  
 $V_{CC}$  (OPR) = 4.5V to 5.5V
- IMPROVED LATCH-UP IMMUNITY



### ORDER CODES

PACKAGE	TUBE	T & R
TSSOP		74ACT16373TTR

### DESCRIPTION

The 74ACT16373 is an advanced high-speed CMOS 16-BIT D-TYPE LATCH (3-STATE) fabricated with sub-micron silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

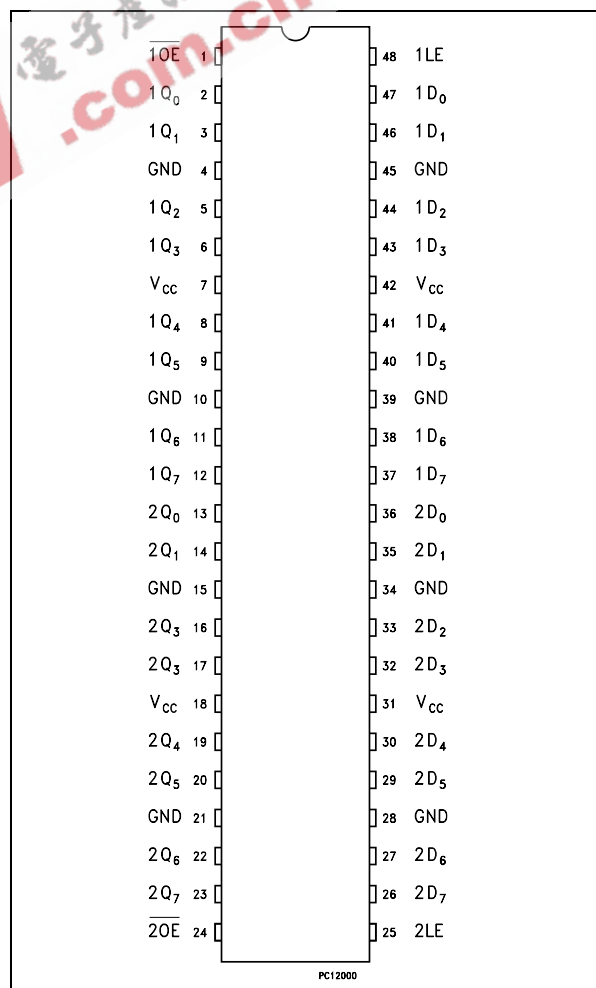
This 16 bit D-Type latch is controlled by two latch enable inputs (LE) and two output enable inputs (OE). The device can be used as two 8-bit latches or one 16-bit latch.

While the LE input is held at a high level, the Q outputs will follow the data inputs precisely. When the LE is taken low, the Q outputs will be latched precisely at the levels set up at the D inputs. While the (OE) input is low, the outputs will be in a normal logic state (high or low logic level) and while OE is in high level the outputs will be in a high impedance state.

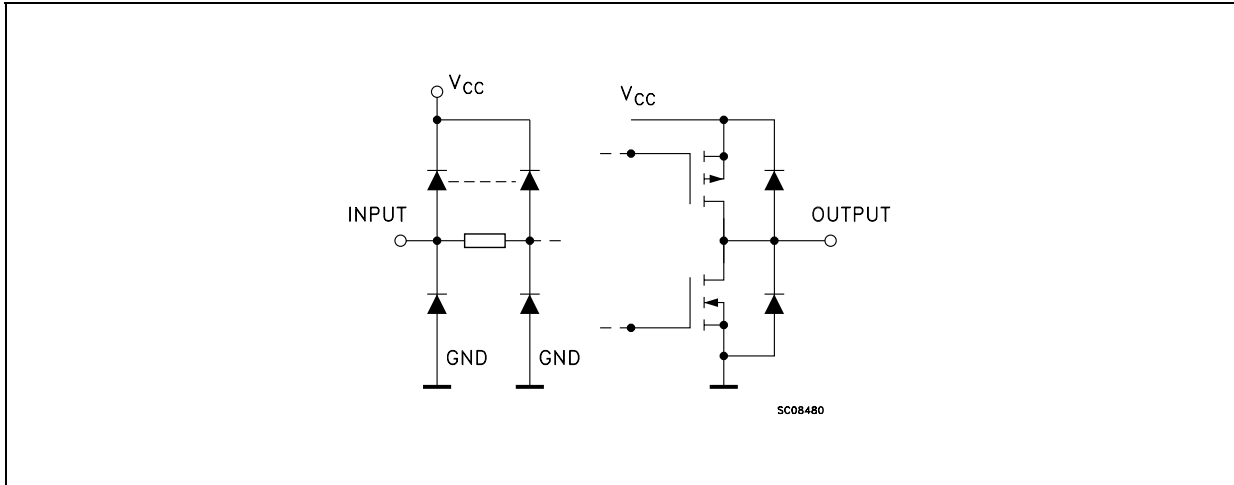
This device is designed to interface directly High Speed CMOS systems with TTL and NMOS components.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

### PIN CONNECTION



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

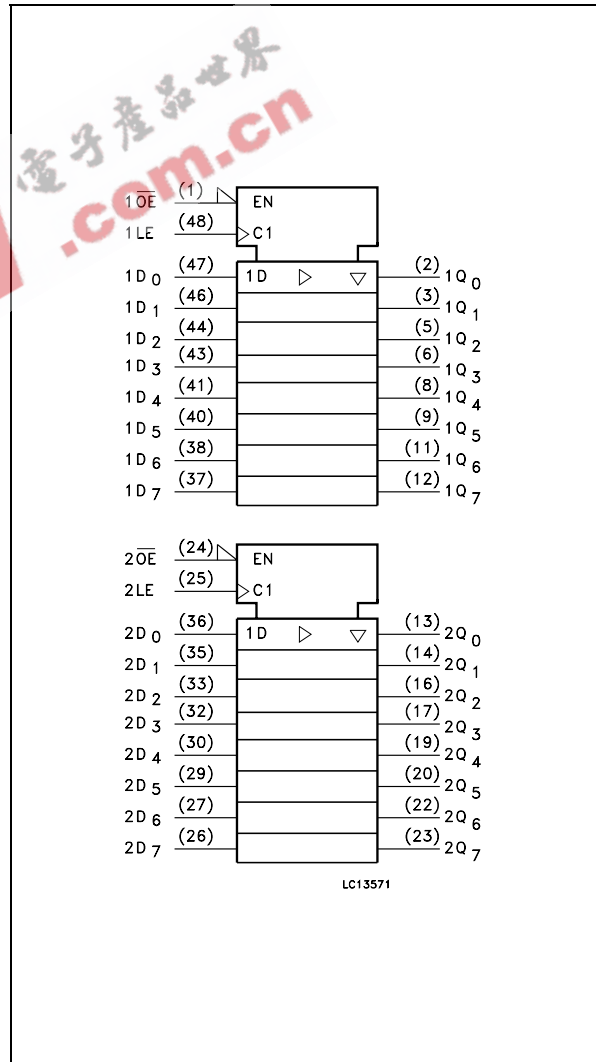
PIN No	SYMBOL	NAME AND FUNCTION
1	1OE	3 State Output Enable Input (Active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Q0 to 1Q7	3-State Outputs
13, 14, 16, 17, 19, 20, 22, 23	2Q0 to 2Q7	3-State Outputs
24	2OE	3 State Output Enable Input (Active LOW)
25	2LE	Latch Enable Input
36, 35, 33, 32, 30, 29, 27, 26	2D0 to 2D7	Data Inputs
47, 46, 44, 43, 41, 40, 38, 37	1D0 to 1D7	Data Inputs
48	1LE	Latch Enable Input
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	VCC	Positive Supply Voltage

TRUTH TABLE

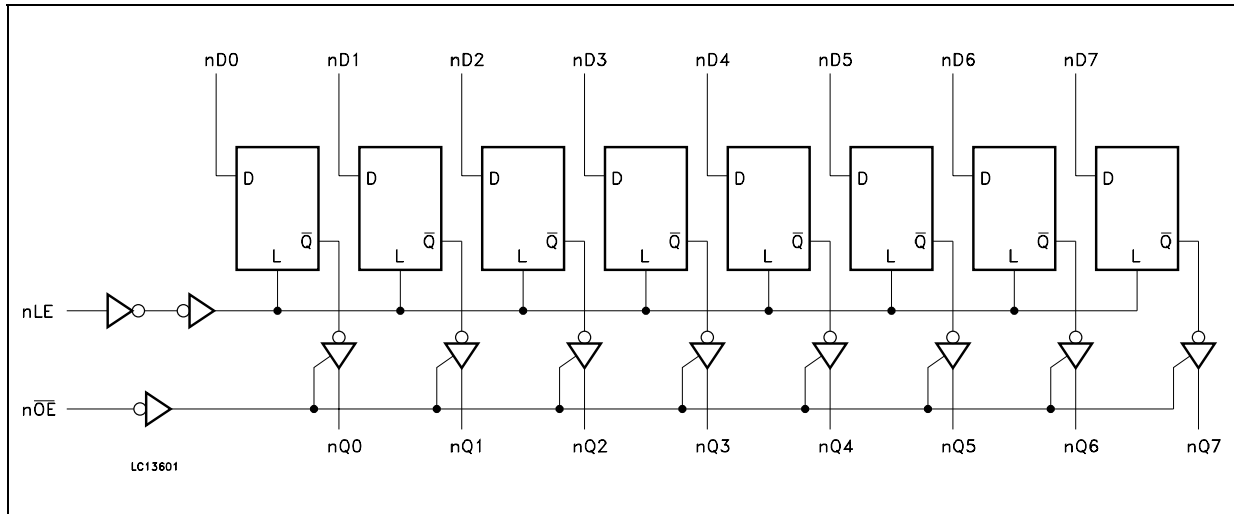
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
H	X	X	Z
L	L	X	NO CHANGE *
L	H	L	L
L	H	H	H

X : Don't Care  
 Z : High Impedance  
 \* : Q outputs are latched at the time when the LE input is taken low logic level.

IEC LOGIC SYMBOLS



## LOGIC DIAGRAM



This logic diagram has not to be used to estimate propagation delays

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to +7	V
$V_I$	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
$V_O$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	$\pm 20$	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Current	$\pm 50$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 400$	mA
$T_{stg}$	Storage Temperature	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (10 sec)	300	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	4.5 to 5.5	V
$V_I$	Input Voltage	0 to $V_{CC}$	V
$V_O$	Output Voltage	0 to $V_{CC}$	V
$T_{op}$	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time $V_{CC} = 4.5$ to $5.5V$ (note 1)	8	ns/V

1)  $V_{IN}$  from 0.8V to 2.0V

## DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
				$T_A = 25^\circ C$			$-40$ to $85^\circ C$		$-55$ to $125^\circ C$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$V_{IH}$	High Level Input Voltage	4.5	$V_O = 0.1 V$ or $V_{CC} - 0.1V$	2.0	1.5		2.0		2.0		V
		5.5		2.0	1.5		2.0		2.0		
$V_{IL}$	Low Level Input Voltage	4.5	$V_O = 0.1 V$ or $V_{CC} - 0.1V$		1.5	0.8		0.8		0.8	V
		5.5			1.5	0.8		0.8		0.8	
$V_{OH}$	High Level Output Voltage	4.5	$I_O = -50 \mu A$	4.4	4.49		4.4		4.4		V
		5.5	$I_O = -50 \mu A$	5.4	5.49		5.4		5.4		
		4.5	$I_O = -24 mA$	3.86			3.76		3.7		
		5.5	$I_O = -24 mA$	4.86			4.76		4.7		
$V_{OL}$	Low Level Output Voltage	4.5	$I_O = 50 \mu A$		0.001	0.1		0.1		0.1	V
		5.5	$I_O = 50 \mu A$		0.001	0.1		0.1		0.1	
		4.5	$I_O = 24 mA$			0.36		0.44		0.5	
		5.5	$I_O = 24 mA$			0.36		0.44		0.5	
$I_I$	Input Leakage Current	5.5	$V_I = V_{CC}$ or GND			$\pm 0.1$		$\pm 1$		$\pm 1$	$\mu A$
$I_{OZ}$	High Impedance Output Leakage Current	5.5	$V_I = V_{IH}$ or $V_{IL}$ $V_O = V_{CC}$ or GND			$\pm 0.5$		$\pm 5$		$\pm 10$	$\mu A$
$I_{CCT}$	Max $I_{CC}$ /Input	5.5	$V_I = V_{CC} - 2.1V$		0.6			1.5		1.6	mA
$I_{CC}$	Quiescent Supply Current	5.5	$V_I = V_{CC}$ or GND			8		80		160	$\mu A$
$I_{OLD}$	Dynamic Output Current (note 1, 2)	5.5	$V_{OLD} = 1.65 V$ max					75		50	mA
$I_{OHD}$			$V_{OHD} = 3.85 V$ min					-75		-50	mA

1) Maximum test duration 2ms, one output loaded at time

2) Incident wave switching is guaranteed on transmission lines with impedances as low as  $50\Omega$

**AC ELECTRICAL CHARACTERISTICS** ( $C_L = 50 \text{ pF}$ ,  $R_L = 500 \Omega$ , Input  $t_r = t_f = 3\text{ns}$ )

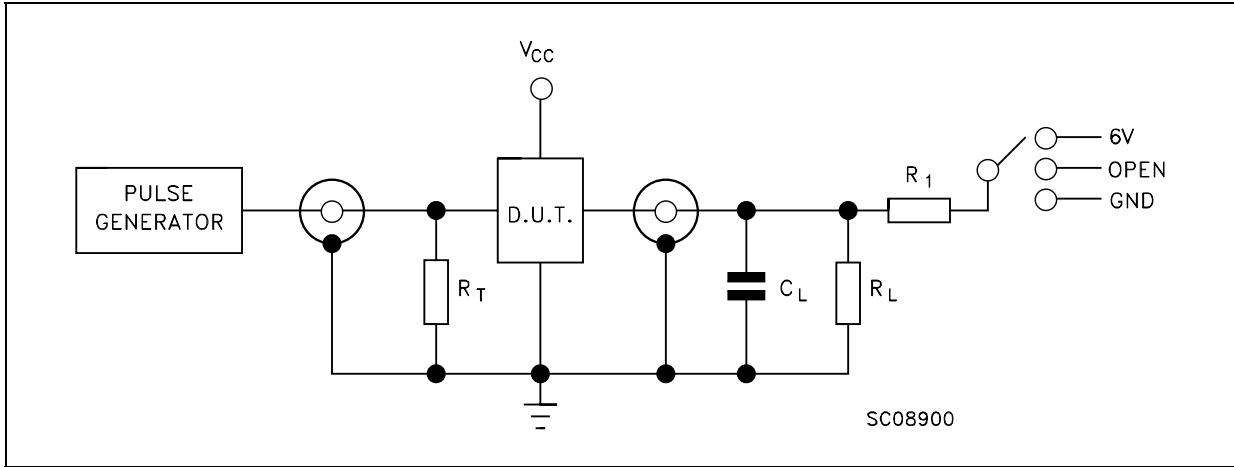
Symbol	Parameter	Test Condition		Value						Unit	
		$V_{CC}$ (V)		$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$t_{PLH}$	Propagation Delay Time LE to Q	5.0(*)			4.2	6.5		12.8		13.7	ns
$t_{PHL}$					5.0	7.7		12.2		13.0	
$t_{PLH}$	Propagation Delay Time D to Q	5.0(*)			4.1	6.3		11.1		11.8	ns
$t_{PHL}$					5.3	8.5		12.3		13.0	
$t_{PZL}$	Output Enable Time	5.0(*)			5.7	6.5		14.2		15.1	ns
$t_{PZH}$					5.0	7.7		12.1		13.0	
$t_{PLZ}$	Output Disable Time	5.0(*)			5.6	8.2		9.4		9.8	ns
$t_{PHZ}$					5.0	7.0		10.7		11.0	
$t_{W(H)}$	LE Minimum Pulse Width HIGH	5.0(*)		2.2	1.7		2.6		2.6	ns	
$t_s$	Setup Time D to LE, HIGH or LOW	5.0(*)		1.2	<1.0		1.4		1.4	ns	
$t_h$	Hold Time D to LE, HIGH or LOW	5.0(*)		1.3	<1.0		1.6		1.6	ns	

(\*) Voltage range is  $5.0\text{V} \pm 0.5\text{V}$ **CAPACITIVE CHARACTERISTICS**

Symbol	Parameter	Test Condition		Value						Unit	
		$V_{CC}$ (V)		$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$C_{IN}$	Input Capacitance	5.0			3.5						pF
$C_{OUT}$	Output Capacitance	5.0			11						pF
$C_{PD}$	Power Dissipation Capacitance (note 1)	5.0	$f_{IN} = 10\text{MHz}$		31						pF

1)  $C_{PD}$  is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/16$  (per circuit)

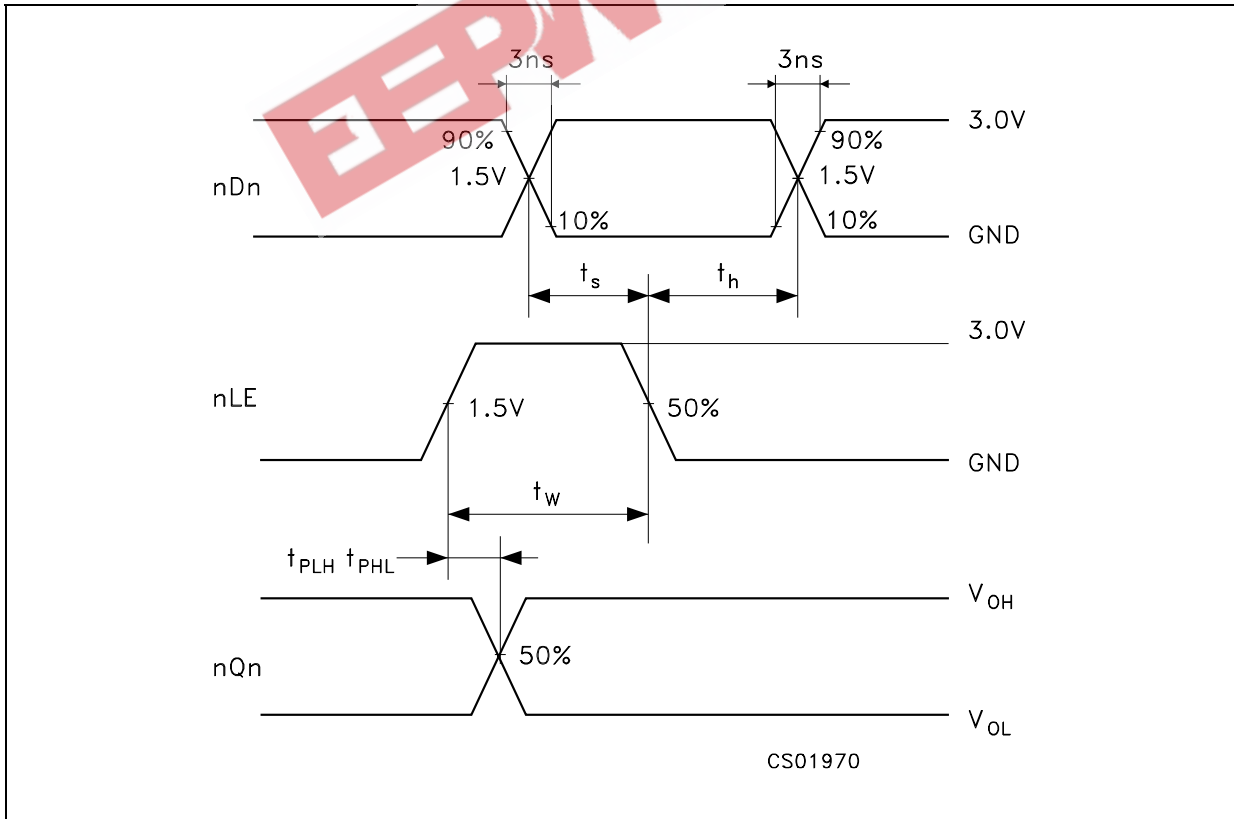
TEST CIRCUIT

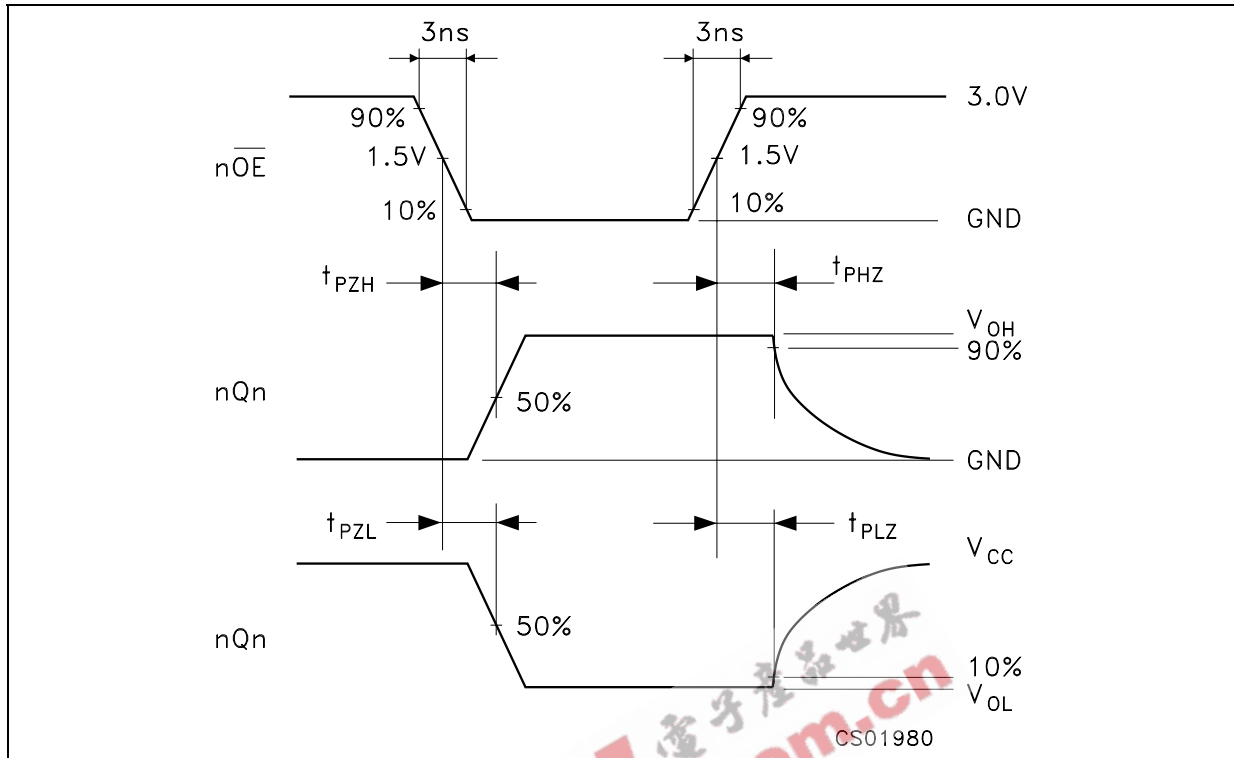
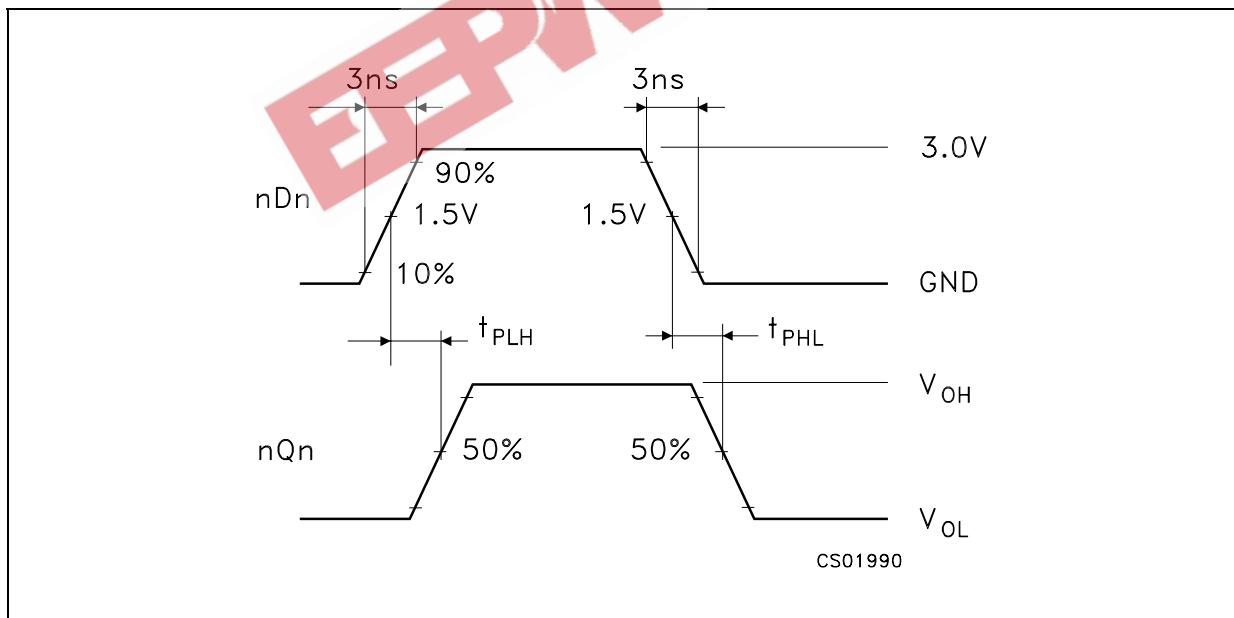


Test	Switch
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	$2V_{CC}$
$t_{PZH}$ , $t_{PHZ}$	GND

$C_L = 50\text{pF}$  or equivalent (includes jig and probe capacitance)  
 $R_L = R_1 = 500\Omega$  or equivalent  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

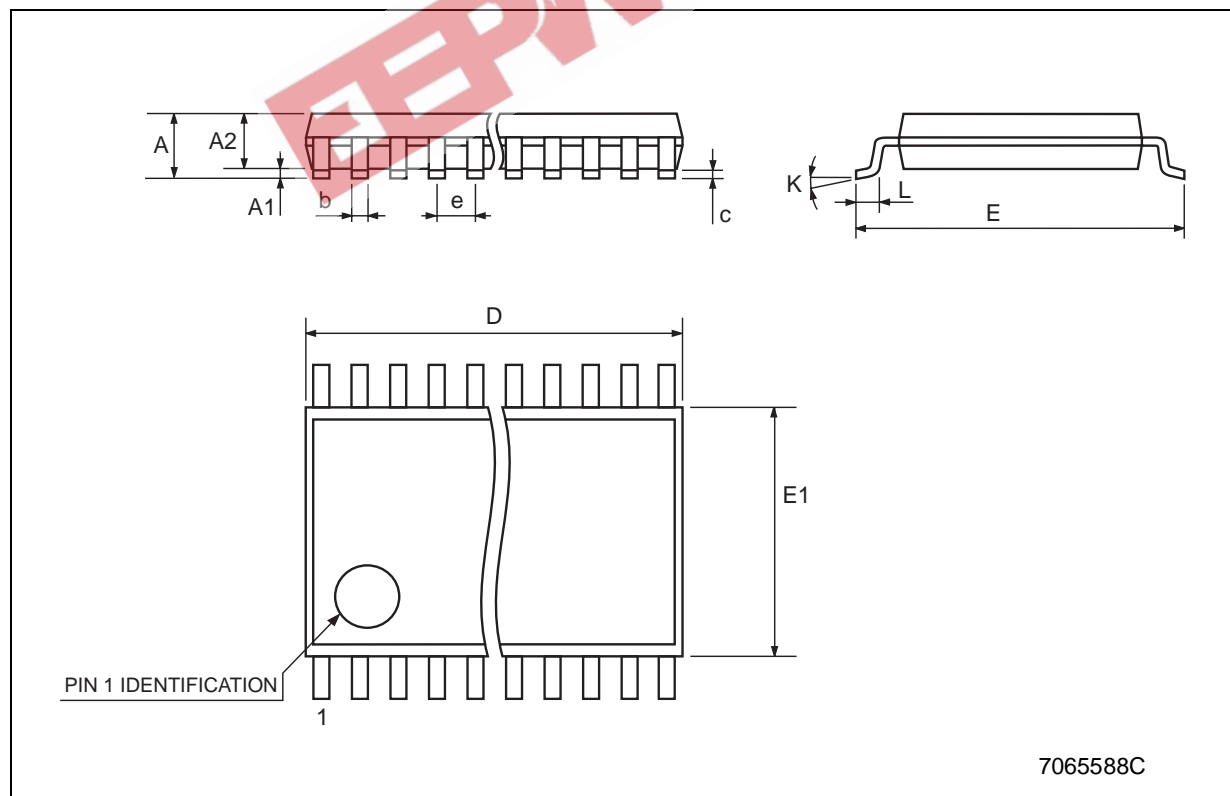
**WAVEFORM 1: PROPAGATION DELAYS, PULSE WIDTH, SETUP AND HOLD TIMES** ( $f=1\text{MHz}$ ; 50% duty cycle)



**WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIMES** ( $f=1\text{MHz}$ ; 50% duty cycle)**WAVEFORM 3: PROPAGATION DELAYS TIME** ( $f=1\text{MHz}$ ; 50% duty cycle)

## TSSOP48 MECHANICAL DATA

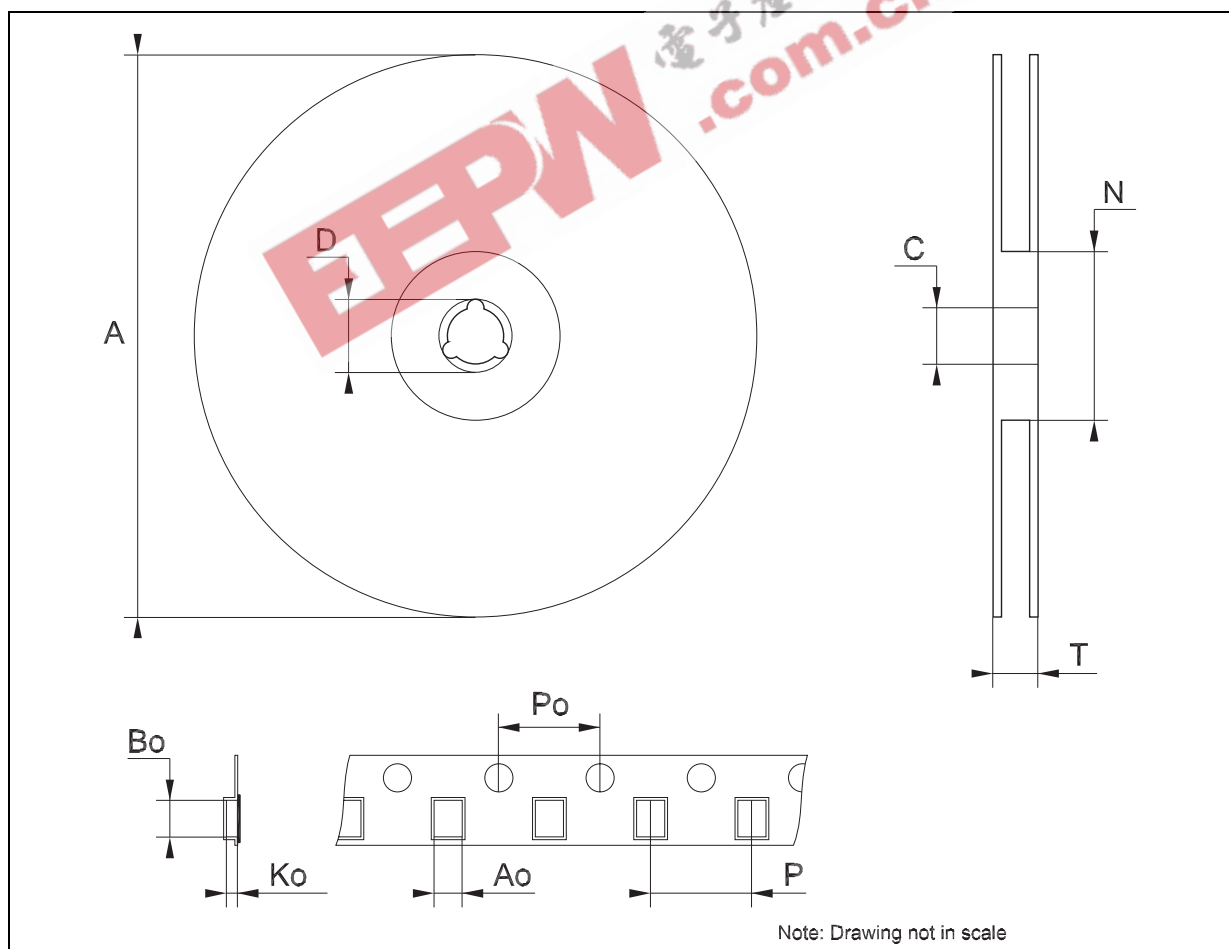
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.17		0.27	0.0067		0.011
c	0.09		0.20	0.0035		0.0079
D	12.4		12.6	0.488		0.496
E		8.1 BSC			0.318 BSC	
E1	6.0		6.2	0.236		0.244
e		0.5 BSC			0.0197 BSC	
K	0°		8°	0°		8°
L	0.50		0.75	0.020		0.030





### Tape & Reel TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	8.7		8.9	0.343		0.350
Bo	13.1		13.3	0.516		0.524
Ko	1.5		1.7	0.059		0.067
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



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