

## 74ABT374

### Octal D-Type Flip-Flop with 3-STATE Outputs

#### General Description

The ABT374 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable (OE) are common to all flip-flops.

#### Features

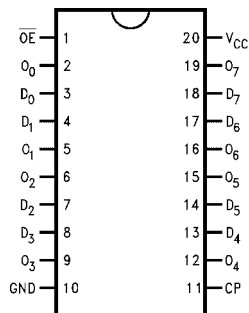
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- 3-STATE outputs for bus-oriented applications
- Output sink capability of 64 mA, source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability

#### Ordering Code:

Order Number	Package Number	Package Description
74ABT374CSC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74ABT374CSJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ABT374CMSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74ABT374CMTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ABT374CPC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

#### Connection Diagram



#### Pin Descriptions

Pin Names	Description
D <sub>0</sub> -D <sub>7</sub>	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{OE}$	3-STATE Output Enable Input (Active LOW)
O <sub>0</sub> -O <sub>7</sub>	3-STATE Outputs

## Functional Description

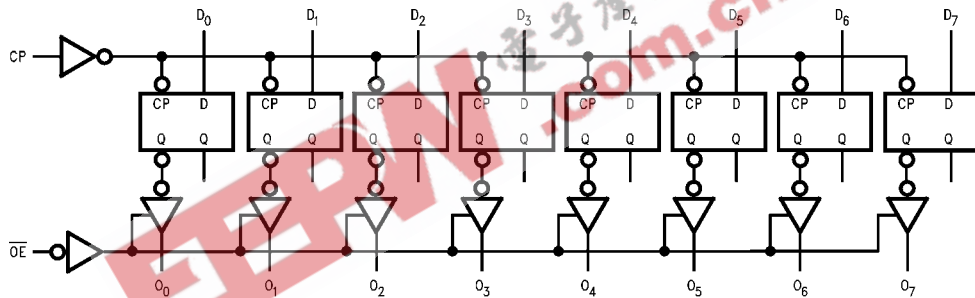
The ABT374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs are in a high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

## Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	↗	L	L	Z	Load
H	↗	H	H	Z	Load
L	↗	L	L	L	Data Available
L	↗	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance  
 ↗ = LOW-to-HIGH Transition  
 NC = No Change

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	-0.5V to 5.5V
in the HIGH State	-0.5V to V <sub>CC</sub>
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Recommended Operating Conditions**

Free Air Ambient Temperature	-40°C to +85°C
Supply Voltage	+4.5V to +5.5V
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100mV/ns

DC Latchup Source Current:

$\overline{OE}$ Pin (Across Comm Operating Range)	-150 mA
Other Pins	-500 mA
Over Voltage Latchup (I/O)	10V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs

**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.5			V	Min	I <sub>OH</sub> = -3 mA
		2.0			V	Min	I <sub>OH</sub> = -32 mA
V <sub>OL</sub>	Output LOW Voltage			0.55	V	Min	I <sub>OL</sub> = 64 mA
I <sub>IH</sub>	Input HIGH Current			1	μA	Max	V <sub>IN</sub> = 2.7V (Note 4)
				1	μA	Max	V <sub>IN</sub> = V <sub>CC</sub>
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>IL</sub>	Input LOW Current			-1	μA	Max	V <sub>IN</sub> = 0.5V (Note 4)
				-1	μA	Max	V <sub>IN</sub> = 0.0V
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA, All Other Pins Grounded
I <sub>OZH</sub>	Output Leakage Current			10	μA	0 - 5.5V	V <sub>OUT</sub> = 2.7V; $\overline{OE}$ = 2.0V
I <sub>OZL</sub>	Output Leakage Current			-10	μA	0 - 5.5V	V <sub>OUT</sub> = 0.5V; $\overline{OE}$ = 2.0V
I <sub>OS</sub>	Output Short-Circuit Current	-100		-275	mA	Max	V <sub>OUT</sub> = 0.0V
I <sub>CEX</sub>	Output High Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>ZZ</sub>	Bus Drainage Test			100	μA	0.0	V <sub>OUT</sub> = 5.5V; All Others V <sub>CC</sub> or GND
I <sub>CCH</sub>	Power Supply Current			50	μA	Max	All Outputs HIGH
I <sub>CCL</sub>	Power Supply Current			30	mA	Max	All Outputs LOW
I <sub>CCZ</sub>	Power Supply Current			50	μA	Max	$\overline{OE}$ = V <sub>CC</sub> ; All Others at V <sub>CC</sub> or GND
I <sub>CCT</sub>	Additional I <sub>CC</sub> /Input	Outputs Enabled		2.5	mA		V <sub>I</sub> = V <sub>CC</sub> - 2.1V
		Outputs 3-STATE		2.5	mA	Max	Enable Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V
		Outputs 3-STATE		2.5	mA		Data Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V
							All Others at V <sub>CC</sub> or GND
I <sub>CCD</sub>	Dynamic I <sub>CC</sub> (Note 4)	No Load		0.30	mA/MHz	Max	Outputs OPEN $\overline{OE}$ = GND, (Note 3) One Bit Toggling, 50% Duty Cycle

**Note 3:** For 8-bit toggling, I<sub>CCD</sub> < 0.8 mA/MHz.

**Note 4:** Guaranteed, but not tested.

## DC Electrical Characteristics

(SOIC package)

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
							C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500Ω
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>		0.5	0.8	V	5.0	T <sub>A</sub> = 25°C (Note 5)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	-1.3	-0.9		V	5.0	T <sub>A</sub> = 25°C (Note 5)
V <sub>OHV</sub>	Minimum HIGH Level Dynamic Output Voltage	2.5	3.0		V	5.0	T <sub>A</sub> = 25°C (Note 6)
V <sub>IHD</sub>	Minimum HIGH Level Dynamic Input Voltage	2.0	1.6		V	5.0	T <sub>A</sub> = 25°C (Note 7)
V <sub>ILD</sub>	Maximum LOW Level Dynamic Input Voltage		1.3	0.8	V	5.0	T <sub>A</sub> = 25°C (Note 7)

**Note 5:** Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output at Low. Guaranteed, but not tested.

**Note 6:** Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

**Note 7:** Max number of data inputs (n) switching. n – 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>). Guaranteed, but not tested.

## AC Electrical Characteristics

(SOIC and SSOP Package)

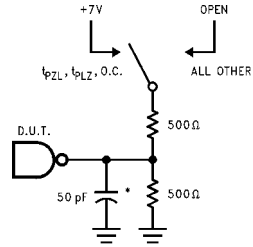
Symbol	Parameter	T <sub>A</sub> = +25°C			T <sub>A</sub> = -55°C to +125°C		T <sub>A</sub> = -40°C to +85°C		Units
		V <sub>CC</sub> = +5.0V			V <sub>CC</sub> = 4.5V to 5.5V		V <sub>CC</sub> = 4.5V to 5.5V		
		C <sub>L</sub> = 50 pF			C <sub>L</sub> = 50 pF		C <sub>L</sub> = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency	150	200		150	150			MHz
t <sub>PLH</sub>	Propagation Delay	2.0	3.2	5.0	1.4	6.6	2.0	5.0	ns
t <sub>PHL</sub>	CP to O <sub>n</sub>	2.0	3.3	5.0	2.0	7.6	2.0	5.0	ns
t <sub>PZH</sub>	Output Enable Time	1.5	3.1	5.3	0.8	5.7	1.5	5.3	ns
t <sub>PZL</sub>		1.5	3.1	5.3	1.5	7.2	1.5	5.3	ns
t <sub>PHZ</sub>	Output Disable Time	1.5	3.6	5.4	1.3	7.2	1.5	5.4	ns
t <sub>PLZ</sub>		1.5	3.4	5.4	1.0	7.0	1.5	5.4	ns

## AC Operating Requirements

Symbol	Parameter	T <sub>A</sub> = +25°C		T <sub>A</sub> = -55°C to +125°C		T <sub>A</sub> = -40°C to +85°C		Units
		V <sub>CC</sub> = +5.0V		V <sub>CC</sub> = 4.5V to 5.5V		V <sub>CC</sub> = 4.5V to 5.5V		
		C <sub>L</sub> = 50 pF		C <sub>L</sub> = 50 pF		C <sub>L</sub> = 50 pF		
		Min	Max	Min	Max	Min	Max	
t <sub>S</sub> (H)	Setup Time, HIGH	1.5		2.5		1.0		ns
t <sub>S</sub> (L)	or LOW D <sub>n</sub> to CP	1.5		2.5		1.5		ns
t <sub>H</sub> (H)	Hold Time, HIGH	1.0		2.5		1.0		ns
t <sub>H</sub> (L)	or LOW D <sub>n</sub> to CP	1.0		2.5		1.0		ns
t <sub>W</sub> (H)	Pulse Width, CP	3.0		3.3		3.0		ns
t <sub>W</sub> (L)	HIGH or LOW	3.0		3.3		3.0		ns

Extended AC Electrical Characteristics								
(SOIC Package)								
Symbol	Parameter	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 50\text{ pF}$ 8 Outputs Switching (Note 8)		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 250\text{ pF}$ (Note 9)		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 250\text{ pF}$ 8 Outputs Switching (Note 10)		Units
		Min	Max	Min	Max	Min	Max	
$t_{PLH}$	Propagation Delay	1.5	5.7	2.0	7.8	2.0	10.0	ns
$t_{PHL}$	CP to $O_n$	1.5	5.7	2.0	7.8	2.0	10.0	
$t_{PZH}$	Output Enable Time	1.5	6.2	2.0	8.0	2.0	10.5	ns
$t_{PZL}$		1.5	6.2	2.0	8.0	2.0	10.5	
$t_{PHZ}$	Output Disable Time	1.0	5.5	(Note 11)		(Note 11)		ns
$t_{PZL}$		1.0	5.5					
<p><b>Note 8:</b> This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).</p> <p><b>Note 9:</b> This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.</p> <p><b>Note 10:</b> This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.</p> <p><b>Note 11:</b> The 3-STATE delay Time is dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.</p>								
Skew (Note 16)								
(SOIC Package)								
Symbol	Parameter	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V} - 5.5\text{V}$ $C_L = 50\text{ pF}$ 8 Outputs Switching (Note 12)		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V} - 5.5\text{V}$ $C_L = 250\text{ pF}$ 8 Outputs Switching (Note 13)		Units		
		Max	Max	Max	Max			
$t_{OSHL}$ (Note 14)	Pin to Pin Skew HL Transitions	1.0		1.8		ns		
$t_{OSLH}$ (Note 14)	Pin to Pin Skew LH Transitions	1.0		1.8				
$t_{PS}$ (Note 13)	Duty Cycle LH-HL Skew	1.8		4.3		ns		
$t_{OST}$ (Note 14)	Pin to Pin Skew LH/HL Transitions	2.0		4.3				
$t_{PV}$ (Note 15)	Device to Device Skew LH/HL Transitions	2.5		4.6		ns		
<p><b>Note 12:</b> This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.</p> <p><b>Note 13:</b> This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.</p> <p><b>Note 14:</b> Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW (<math>t_{OSHL}</math>), LOW-to-HIGH (<math>t_{OSLH}</math>), or any combination switching LOW-to-HIGH and/or HIGH-to-LOW (<math>t_{OST}</math>). This specification is guaranteed but not tested.</p> <p><b>Note 15:</b> Propagation delay variation for a given set of conditions (i.e., temperature and <math>V_{CC}</math>) from device to device. This specification is guaranteed but not tested.</p> <p><b>Note 16:</b> This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).</p>								
Capacitance								
Symbol	Parameter	Typ	Units	Conditions ( $T_A = 25^\circ\text{C}$ )				
$C_{IN}$	Input Capacitance	5.0	pF	$V_{CC} = 0\text{V}$				
$C_{OUT}$ (Note 17)	Output Capacitance	9.0	pF	$V_{CC} = 5.0\text{V}$				
<p><b>Note 17:</b> <math>C_{OUT}</math> is measured at frequency <math>f = 1\text{ MHz}</math>, per MIL-STD-883, Method 3012.</p>								

### AC Loading



\*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

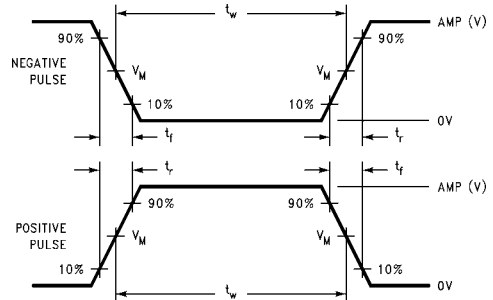


FIGURE 2.  $V_M = 1.5V$

#### Input Pulse Requirements

Amplitude	Rep. Rate	$t_w$	$t_r$	$t_f$
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

### AC Waveforms

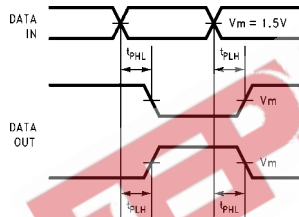


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

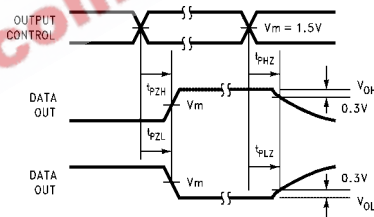


FIGURE 6. 3-STATE Output HIGH and LOW Enable and Disable Times

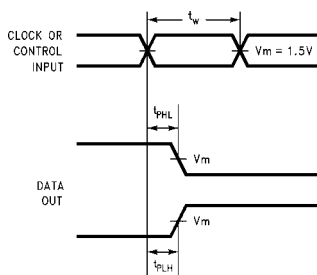


FIGURE 5. Propagation Delay, Pulse Width Waveforms

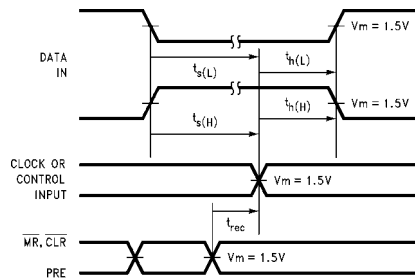
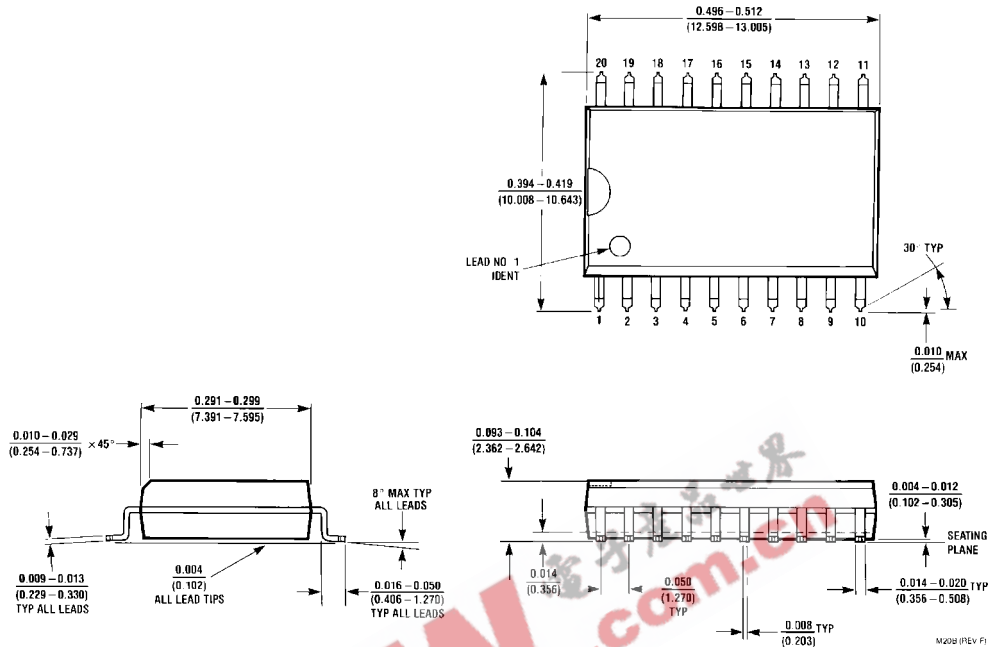


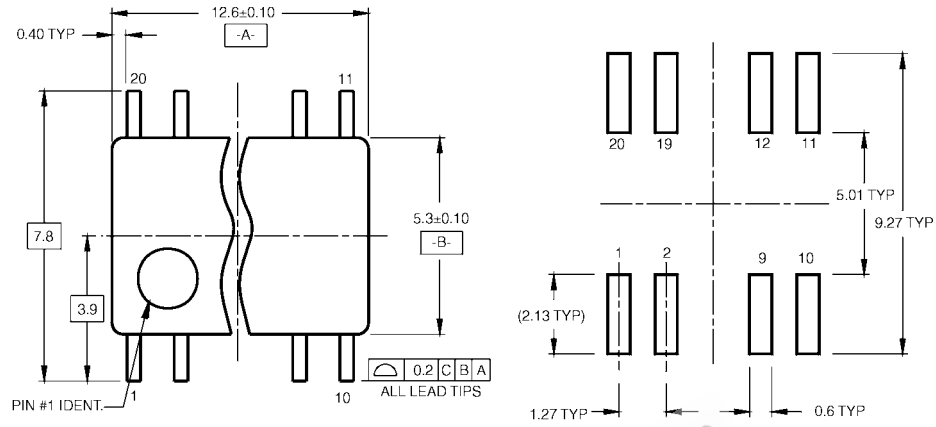
FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

**Physical Dimensions** inches (millimeters) unless otherwise noted

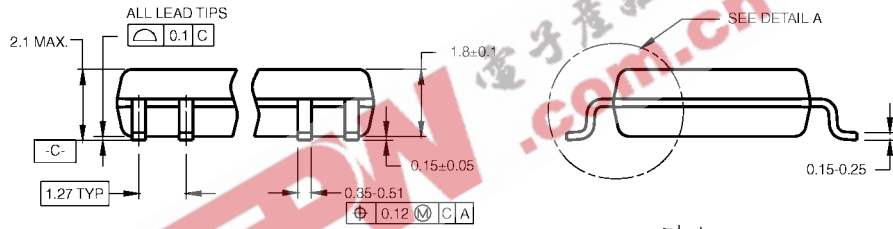


**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body  
Package Number M20B**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION

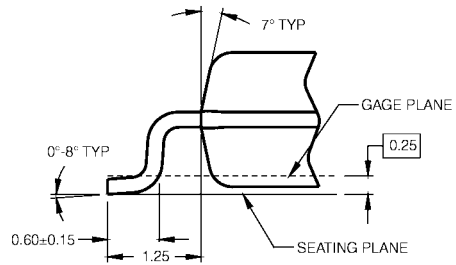


DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1996.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

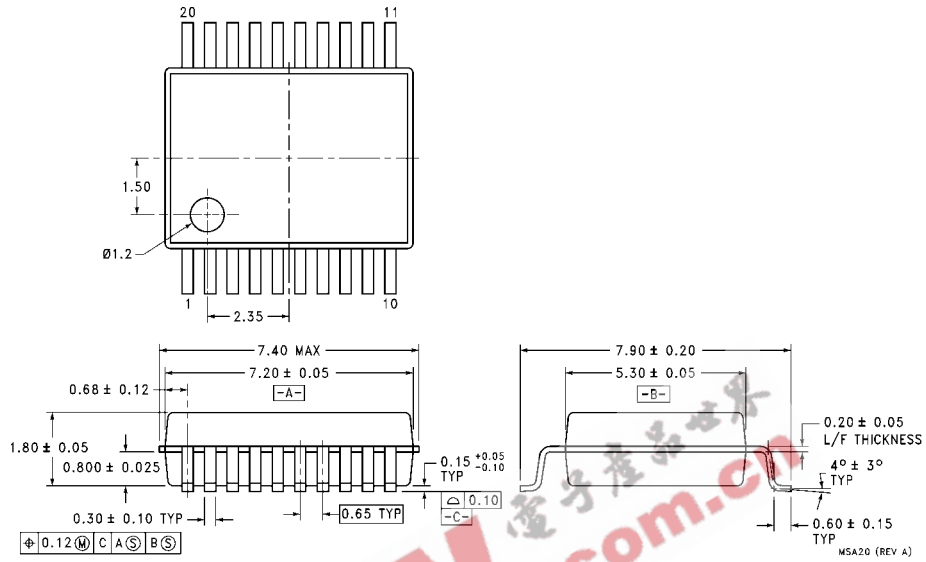


DETAIL A

**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M20D**

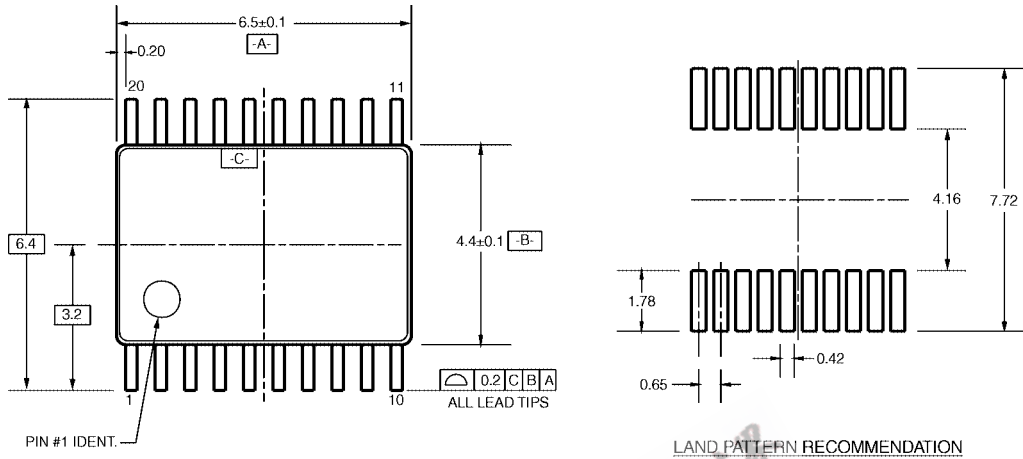


**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



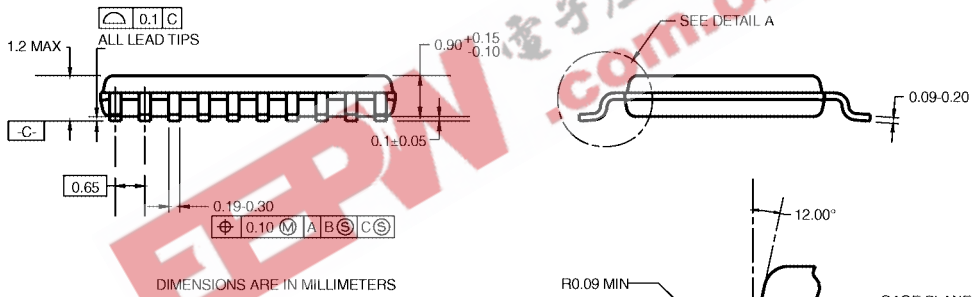
**20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide**  
**Package Number MSA20**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



PIN #1 IDENT.

LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS

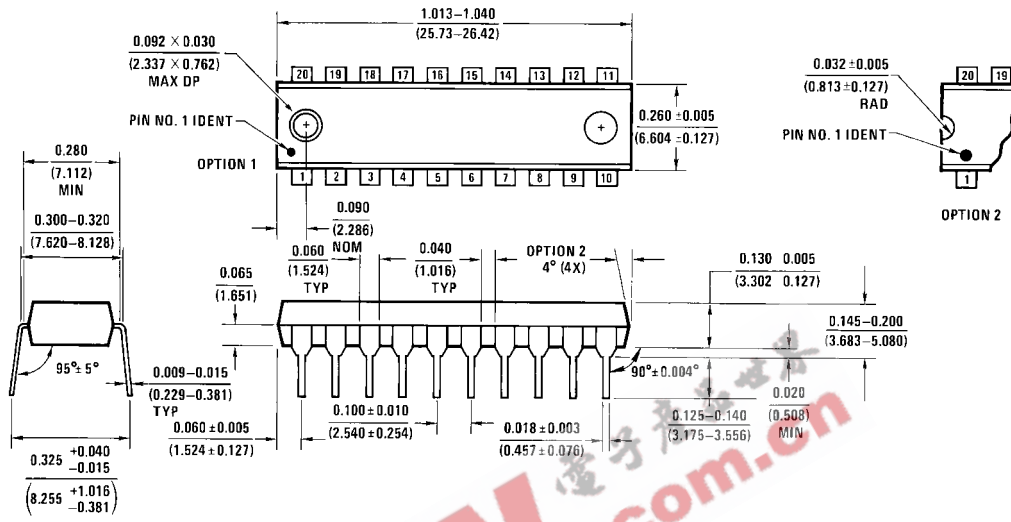
- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
  - D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20RevD1

DETAIL A

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC20**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MO-001, 0.300" Wide Package Number N20A**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)