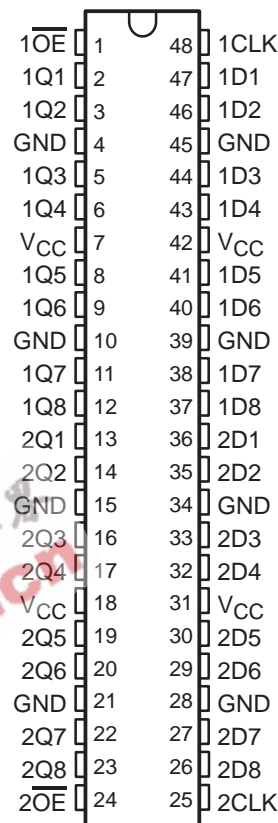


# 54AC16374, 74AC16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCAS123B – MARCH 1990 – REVISED APRIL 1996

- Members of the Texas Instruments *Widebus*™ Family
- 3-State True Outputs
- Full Parallel Access for Loading
- Flow-Through Architecture Optimizes PCB Layout
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- *EPIC*™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings

54AC16374 . . . WD PACKAGE  
74AC16374 . . . DL PACKAGE  
(TOP VIEW)



## description

The 'AC16374 are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 'AC16374 can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

$\overline{OE}$  does not affect the internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74AC16374 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54AC16374 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The 74AC16374 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .



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 **TEXAS  
INSTRUMENTS**

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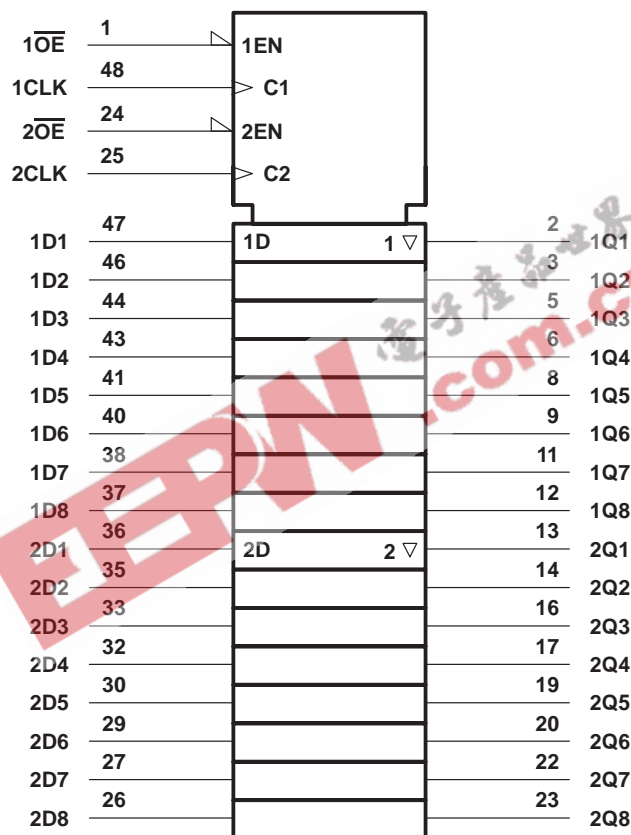
# 54AC16374, 74AC16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCAS123B – MARCH 1990 – REVISED APRIL 1996

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	X	X	$Q_0$
L	↓	X	$Q_0$
H	X	X	Z

logic symbol†

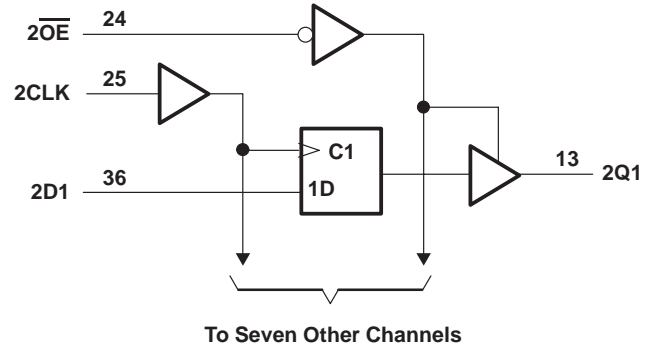
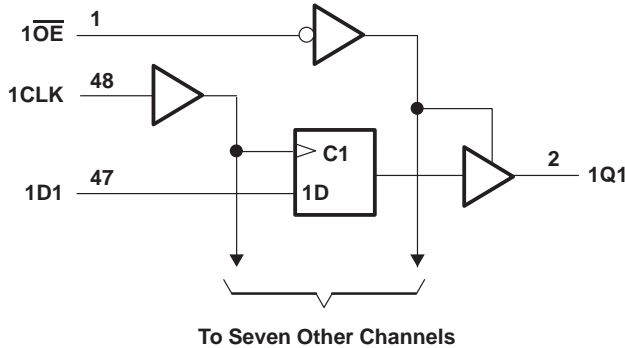


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# 54AC16374, 74AC16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 400$ mA
Maximum power package dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DL package .....	1.2 W
Storage temperature range, $T_{stg}$ .....	$-65^\circ\text{C}$ to $150^\circ\text{C}$

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of  $150^\circ\text{C}$  and a board trace length of 750 mils.

# 54AC16374, 74AC16374

## 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCAS123B – MARCH 1990 – REVISED APRIL 1996

### recommended operating conditions (see Note 3)

		54AC16374			74AC16374			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	3	5	5.5	3	5	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 3 V		2.1	2.1		V	
		V <sub>CC</sub> = 4.5 V		3.15	3.15			
		V <sub>CC</sub> = 5.5 V		3.85	3.85			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 3 V			0.9		V	
		V <sub>CC</sub> = 4.5 V			1.35			
		V <sub>CC</sub> = 5.5 V			1.65			
V <sub>I</sub>	Input voltage	0		V <sub>CC</sub>	0	V <sub>CC</sub>	V	
V <sub>O</sub>	Output voltage	0		V <sub>CC</sub>	0	V <sub>CC</sub>	V	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 3 V			-4		mA	
		V <sub>CC</sub> = 4.5 V			-24			
		V <sub>CC</sub> = 5.5 V			-24			
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 3 V			12		mA	
		V <sub>CC</sub> = 4.5 V			24			
		V <sub>CC</sub> = 5.5 V			24			
Δt/Δv	Input transition rise or fall rate	0		10	0	10	ns/V	
T <sub>A</sub>	Operating free-air temperature	-55		125	-40	85	°C	

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			54AC16374		74AC16374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	3 V	2.9			2.9		2.9	V	
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		2.48		
		4.5 V	3.94			3.8		3.8		
		5.5 V	4.94			4.8		4.8		
I <sub>OH</sub> = -75 mA <sup>†</sup>	5.5 V				3.85		3.85			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	3 V				0.1		0.1	V	
		4.5 V				0.1		0.1		
		5.5 V				0.1		0.1		
	I <sub>OL</sub> = 12 mA	3 V				0.36		0.44		
		4.5 V				0.36		0.44		
		5.5 V				0.36		0.44		
I <sub>OL</sub> = 75 mA <sup>†</sup>	5.5 V					1.65	1.65			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1	±1	μA	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±0.5		±5	±5	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			8		80	80	μA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V			3				pF	
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V			11				pF	

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

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# 54AC16374, 74AC16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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**timing requirements over recommended operating free-air temperature range**  
**V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

		T <sub>A</sub> = 25°C		54AC16374		74AC16374		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	0	60	0	60	0	60	MHz
t <sub>w</sub>	Pulse duration	CLK high or low		8.3		8.3		ns
t <sub>su</sub>	Setup time, data before CLK↑			7.5		7.5		ns
t <sub>h</sub>	Hold time, data after CLK↑			0		0		ns

**timing requirements over recommended operating free-air temperature range**  
**V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

		T <sub>A</sub> = 25°C		54AC16374		74AC16374		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	0	100	0	100	0	100	MHz
t <sub>w</sub>	Pulse duration	CLK high or low		5		5		ns
t <sub>su</sub>	Setup time, data before CLK↑			5		5		ns
t <sub>h</sub>	Hold time, data after CLK↑			0		0		ns

**switching characteristics over recommended operating free-air temperature range**  
**V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			54AC16374		74AC16374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			60			60		60	MHz	
t <sub>PLH</sub>	CLK	Q	4.9	12.2	15	4.9	17	4.9	17	ns
t <sub>PHL</sub>			4.8	11.9	14.3	4.8	15.7	4.8	15.7	
t <sub>PZH</sub>	$\overline{OE}$	Q	4.3	11.9	14.7	4.3	16.8	4.3	16.8	ns
t <sub>PZL</sub>			5.3	15.5	18.7	5.3	21.2	5.3	21.2	
t <sub>PHZ</sub>	$\overline{OE}$	Q	4	7.3	9	4	9.8	4	9.8	ns
t <sub>PLZ</sub>			3.8	7.1	8.8	3.8	9.4	3.8	9.4	

**switching characteristics over recommended operating free-air temperature range**  
**V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			54AC16374		74AC16374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			100			100		100	MHz	
t <sub>PLH</sub>	CLK	Q	3.8	7.6	9.5	3.8	10.8	3.8	10.8	ns
t <sub>PHL</sub>			3.8	7.6	9.5	3.8	10.6	3.8	10.6	
t <sub>PZH</sub>	$\overline{OE}$	Q	3.2	7.2	9	3.2	10.2	3.2	10.2	ns
t <sub>PZL</sub>			3.8	8.7	10.7	3.8	12.1	3.8	12.1	
t <sub>PHZ</sub>	$\overline{OE}$	Q	3.7	6	7.5	3.7	8.2	3.7	8.2	ns
t <sub>PLZ</sub>			3.5	5.8	7.3	3.5	7.9	3.5	7.9	

**operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C**

PARAMETER		TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per flip-flop	C <sub>L</sub> = 50 pF, f = 1 MHz	49	pF
			32	

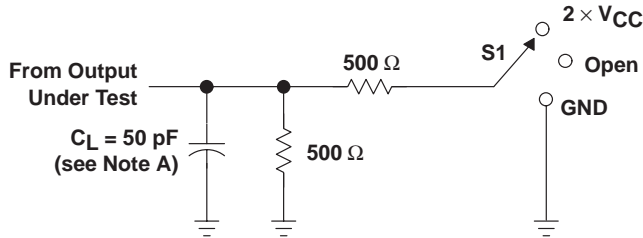
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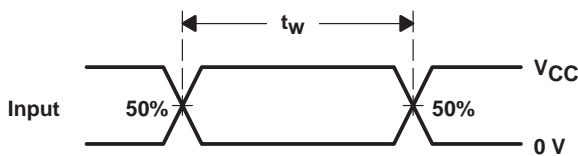
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## PARAMETER MEASUREMENT INFORMATION

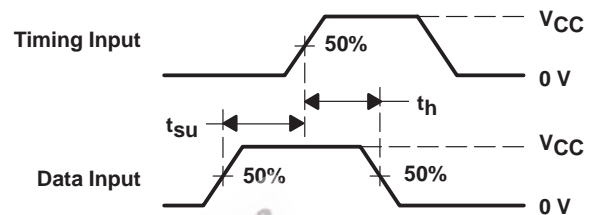


LOAD CIRCUIT

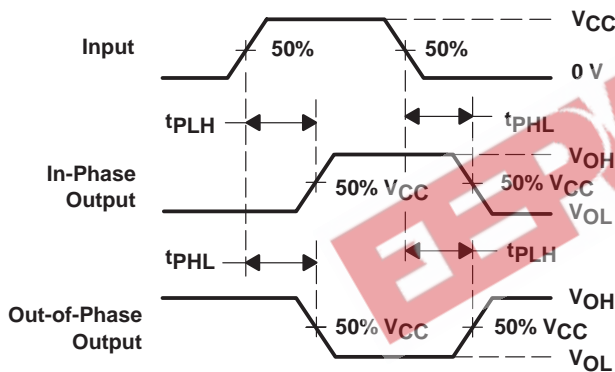
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



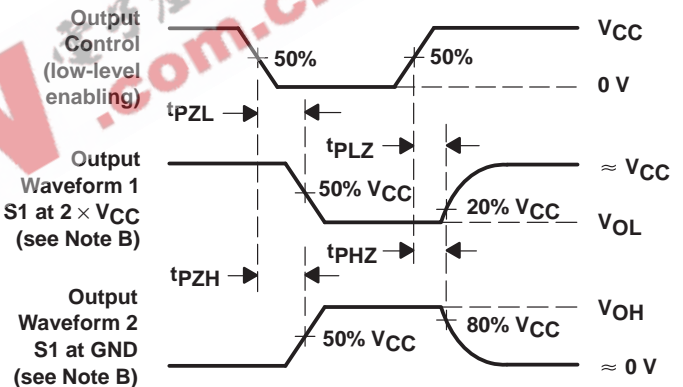
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ .  
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74AC16374DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AC16374DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AC16374DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AC16374DLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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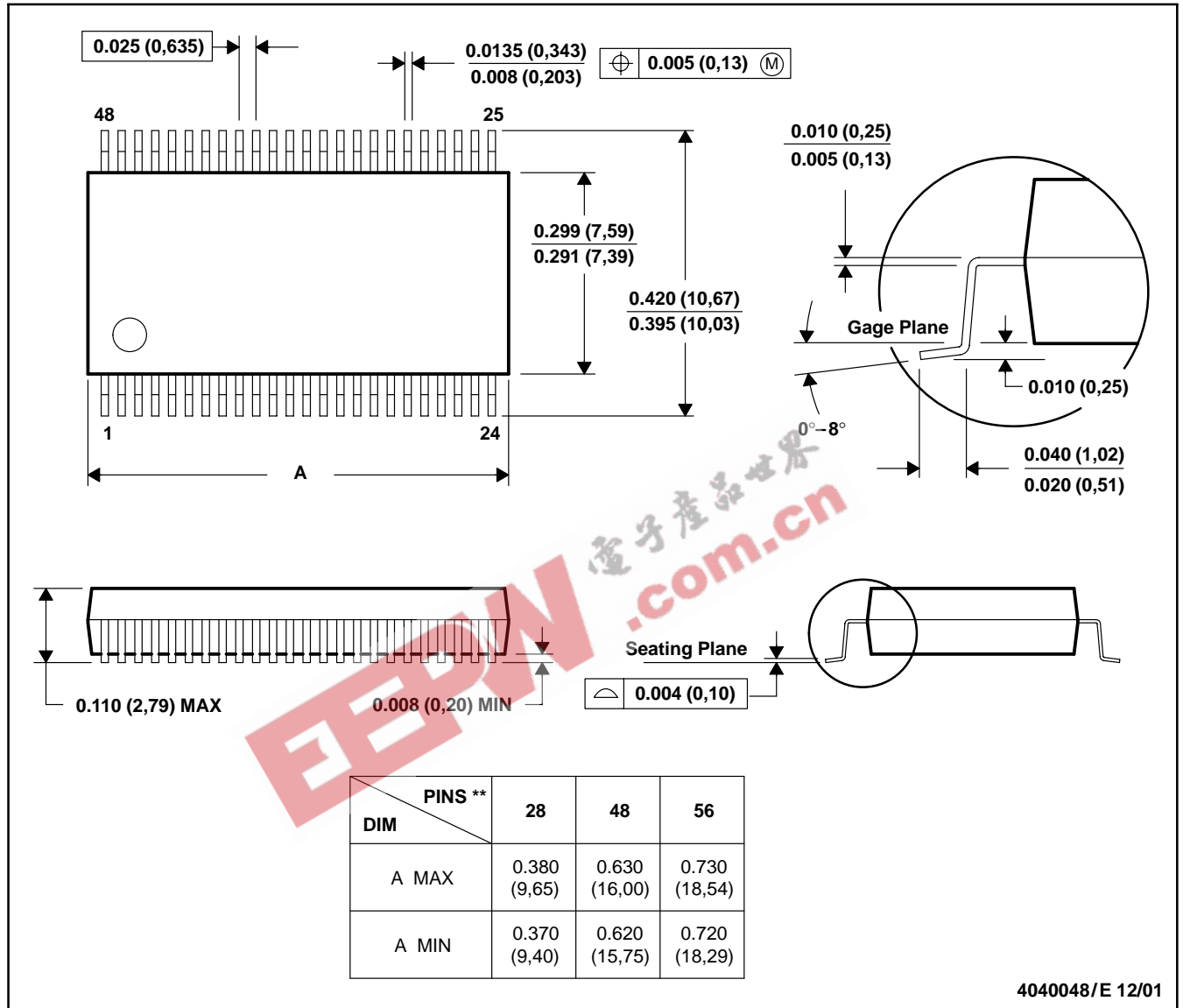
# MECHANICAL DATA

MSS0001C – JANUARY 1995 – REVISED DECEMBER 2001

## DL (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118



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Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
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