

8-INPUT MULTIPLEXER/REGISTER WITH TRANSPARENT LATCHES; 3-STATE

FEATURES

- Transparent data latches
- Transparent address latch
- Easily expanding
- Complementary outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT354 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT354 data selectors/multiplexers contain full on-chip binary decoding, to select one-of-eight data sources. The data select address is stored in transparent latches that are enabled by a LOW on the latch enable input ($\overline{LE}$).

The transparent 8-bit data latches are enabled when the active LOW data enable input ($\overline{E}$) is LOW. When the output enable input $\overline{OE}_1 = \text{HIGH}$, $\overline{OE}_2 = \text{HIGH}$ or $\overline{OE}_3 = \text{LOW}$, the outputs go to the high impedance OFF-state. Operation of these output enable inputs does not affect the state of the latches.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $D_n, \overline{E}$ to $Y, \overline{Y}$ $S_n, \overline{LE}$ to $Y, \overline{Y}$	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	20 24	22 27	ns ns
C_I	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per latch	notes 1 and 2	68	71	pF

GND = 0 V; $T_{amb} = 25^\circ\text{C}$; $t_r = t_f = 6 \text{ ns}$

Notes

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz
 f_o = output frequency in MHz
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
 C_L = output load capacitance in pF
 V_{CC} = supply voltage in V

2. For HC, the condition is $V_I = \text{GND to } V_{CC}$
For HCT the condition is $V_I = \text{GND to } V_{CC} - 1.5 \text{ V}$

PACKAGE OUTLINES

20-lead DIL; plastic (SOT146).

20-lead mini-pack; plastic (SO20; SOT163A).

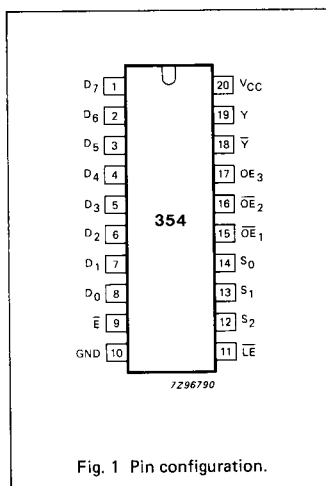


Fig. 1 Pin configuration.

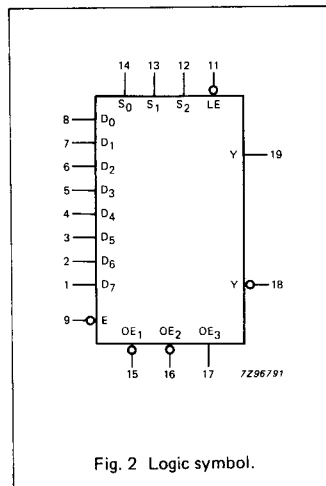


Fig. 2 Logic symbol.

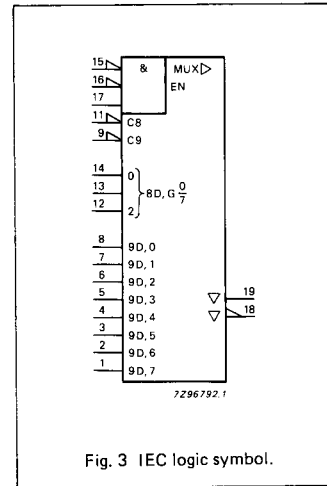


Fig. 3 IEC logic symbol.

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8, 7, 6, 5, 4, 3, 2, 1	D ₀ to D ₇	data inputs
9	$\bar{E}$	data enable input (active LOW)
10	GND	ground (0 V)
11	$\bar{LE}$	address latch enable input (active LOW)
14, 13, 12	S ₀ , S ₁ , S ₂	select inputs
15, 16	$\bar{OE}_1$, $\bar{OE}_2$	output enable inputs (active LOW)
17	OE ₃	output enable input (active HIGH)
18	$\bar{Y}$	3-state multiplexer output (active LOW)
19	Y	3-state multiplexer output (active HIGH)
20	V _{CC}	positive supply voltage

FUNCTION TABLE

INPUTS							OUTPUTS		DESCRIPTION	
ADDRESS *			$\bar{E}$	OUTPUT ENABLE			Y	$\bar{Y}$		
S ₂	S ₁	S ₀		$\bar{OE}_1$	$\bar{OE}_2$	OE ₃				
X X X	X X X	X X X	X X X	H X X	X H X	X X L	Z Z Z	Z Z Z	outputs in high impedance OFF-state	
L L L	L H H	L H H	L L L	L L L	L L L	H H H	D ₀ D ₁ D ₂ D ₃	$\bar{D}_0$ $\bar{D}_1$ $\bar{D}_2$ $\bar{D}_3$	data latch is transparent	
H H H	L L H H	L H L H	L L L L	L L L L	L L L L	H H H H	D ₄ D ₅ D ₆ D ₇	$\bar{D}_4$ $\bar{D}_5$ $\bar{D}_6$ $\bar{D}_7$		
L L L L	L L H H	L H L H	H H L H	L L L L	L L L L	H H H H	D _{0n} D _{1n} D _{2n} D _{3n}	$\bar{D}_{0n}$ $\bar{D}_{1n}$ $\bar{D}_{2n}$ $\bar{D}_{3n}$		data is latched
H H H H	L L H H	L H L H	H H L H	L L L L	L L L L	H H H H	D _{4n} D _{5n} D _{6n} D _{7n}	$\bar{D}_{4n}$ $\bar{D}_{5n}$ $\bar{D}_{6n}$ $\bar{D}_{7n}$		

D₀ to D₇ = data at inputs D₀ to D₇

D_{0n} to D_{7n} = data at inputs D₀ to D₇ before the most recent LOW-to-HIGH transition of $\bar{E}$

H = HIGH voltage level

L = LOW voltage level

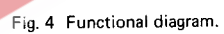
X = don't care

Z = high impedance OFF-state

* This column shows the input address set-up with $\bar{LE}$ = LOW (address latch is transparent).

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS	
		74HC									V _{CC} V	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} / t _{PLH}	propagation delay D _N to Y, $\bar{Y}$		61 22 18	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 7	
t _{PHL} / t _{PLH}	propagation delay $\bar{E}$ to Y, $\bar{Y}$		63 23 18	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 6	
t _{PHL} / t _{PLH}	propagation delay S _N to Y, $\bar{Y}$		77 28 22	260 52 44		325 65 55		390 78 66	ns	2.0 4.5 6.0	Fig. 8	
t _{PHL} / t _{PLH}	propagation delay $\bar{L}\bar{E}$ to Y, $\bar{Y}$		77 28 22	290 58 49		365 73 62		435 87 74	ns	2.0 4.5 6.0	Fig. 9	
t _{PZH} / t _{PZL}	3-state output enable time $\bar{OE}_N$ to Y, $\bar{Y}$		39 14 11	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 12	
t _{PZH} / t _{PZL}	3-state output enable time OE ₃ to Y, $\bar{Y}$		44 16 13	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig. 12	
t _{PHZ} / t _{PLZ}	3-state output disable time $\bar{OE}_N$ to Y, $\bar{Y}$		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 12	
t _{PHZ} / t _{PLZ}	3-state output disable time OE ₃ to Y, $\bar{Y}$		55 20 16	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 12	
t _{THL} / t _{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Figs 7, 8 and 9	
t _W	data enable pulse width $\bar{E}$ LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6	
t _W	latch enable pulse width $\bar{L}\bar{E}$ LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9	
t _{su}	set-up time D _N to $\bar{E}$	50 10 9	11 4 3		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10	
t _{su}	set-up time S _N to $\bar{L}\bar{E}$	50 10 9	14 5 4		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10	

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HCT							V _{CC} V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay D _N to Y, $\bar{Y}$		25	47		59		71	ns	4.5	Fig. 7
t _{PHL} / t _{PLH}	propagation delay $\bar{E}$ to Y, $\bar{Y}$		26	54		68		81	ns	4.5	Fig. 6
t _{PHL} / t _{PLH}	propagation delay S _N to Y, $\bar{Y}$		30	59		74		89	ns	4.5	Fig. 8
t _{PHL} / t _{PLH}	propagation delay $\bar{LE}$ to Y, $\bar{Y}$		31	63		79		95	ns	4.5	Fig. 9
t _{PZH} / t _{PZL}	3-state output enable time $\bar{OE}_N$ to Y, $\bar{Y}$		18	34		43		51	ns	4.5	Fig. 12
t _{PZH} / t _{PZL}	3-state output enable time $\bar{OE}_3$ to Y, $\bar{Y}$		18	34		43		51	ns	4.5	Fig. 12
t _{PHZ} / t _{PLZ}	3-state output disable time $\bar{OE}_N$ to Y, $\bar{Y}$		18	33		41		50	ns	4.5	Fig. 12
t _{PHZ} / t _{PLZ}	3-state output disable time $\bar{OE}_3$ to Y, $\bar{Y}$		21	39		49		59	ns	4.5	Fig. 12
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Figs 7, 8 and 9
t _W	data enable pulse width $\bar{E}$ LOW	16	6		20		24		ns	4.5	Fig. 6
t _W	latch enable pulse width $\bar{LE}$ LOW	16	6		20		24		ns	4.5	Fig. 9
t _{su}	set-up time D _N to $\bar{E}$	10	4		13		15		ns	4.5	Fig. 11
t _{su}	set-up time S _N to $\bar{LE}$	10	5		13		15		ns	4.5	Fig. 10
t _h	hold time D _N to $\bar{E}$	9	0		11		14		ns	4.5	Fig. 11
t _h	hold time S _N to $\bar{LE}$	9	-3		11		14		ns	4.5	Fig. 10

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SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS	
		74HC									V _{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _h	hold time D _n to $\overline{E}$	5 5 5	−6 −2 −2		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 11	
t _h	hold time S _n to $\overline{LE}$	5 5 5	−8 −3 −2		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 10	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D _n , S _n	0.2
OE ₃	0.25
$\overline{LE}$	0.5
$\overline{E}$, $\overline{OE}_n$	1.0

AC WAVEFORMS (Cont'd)

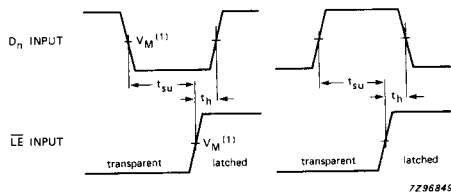


Fig. 10 Waveforms showing the set-up and hold times for the select input (S_n) to the address latch enable input ($\overline{LE}$).

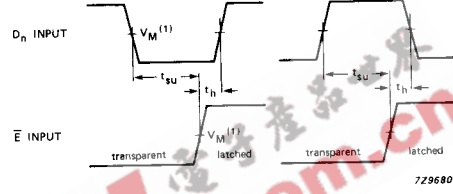


Fig. 11 Waveforms showing the set-up and hold times for the data input (D_n) to the data enable input ($\overline{E}$).

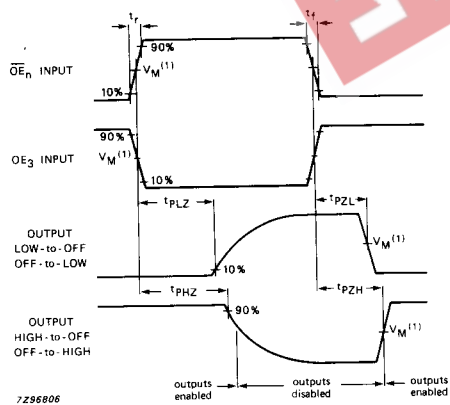


Fig. 12 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$
HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.