



September 2000
Revised August 2001

74LVTH32952 Low Voltage 32-Bit Registered Transceiver with 3-STATE Outputs (Preliminary)

General Description

The LVTH32952 is a 32-bit registered transceiver. Four 8-bit back to back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable, and output enable signals are provided for each register.

The LVTH32952 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

The registered transceiver is designed for low voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment.

The LVTH32952 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink $-32\text{ mA}/+64\text{ mA}$
- ESD performance:
 - Human-body model > 2000V
 - Machine model > 200V
 - Charged-device model > 1000V
- Packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

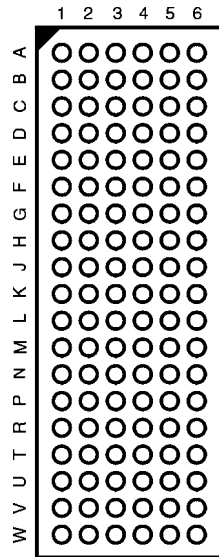
Ordering Code:

Order Number	Package Number	Package Description
74LVTH32952GX (Note 1)	BGA114A (Preliminary)	114-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL]

Note 1: BGA package available in Tape and Reel only.

74LVTH32952 Low Voltage 32-Bit Registered Transceiver with 3-STATE Outputs (Preliminary)

Connection Diagram



(Top Thru View)

Pin Descriptions

Pin Names	Description
A ₀ -A ₃₁	Data Register A Inputs B-Register 3-STATE Outputs
B ₀ -B ₃₁	Data Register B Inputs A-Register 3-STATE Outputs
CPAB _n , CPBA _n	Clock Pulse Inputs
\overline{CEA}_n , \overline{CEB}_n	Clock Enable
\overline{OEAB}_n , \overline{OEBA}_n	Output Enable Inputs

Pin Assignments for FBGA

	1	2	3	4	5	6
A	A ₀	\overline{CEA}_1	CPAB ₁	CPBA ₁	\overline{CEB}_1	B ₀
B	A ₂	A ₁	\overline{OEAB}_1	\overline{OEBA}_1	B ₁	B ₂
C	A ₄	A ₃	GND	GND	B ₃	B ₄
D	A ₆	A ₅	V _{CC1}	V _{CC1}	B ₅	B ₆
E	A ₈	A ₇	GND	GND	B ₇	B ₈
F	A ₁₀	A ₉	GND	GND	B ₉	B ₁₀
G	A ₁₂	A ₁₁	V _{CC1}	V _{CC1}	B ₁₁	B ₁₂
H	A ₁₃	A ₁₄	GND	GND	B ₁₄	B ₁₃
J	A ₁₅	\overline{CEA}_2	CPAB ₂	CPBA ₂	\overline{CEB}_2	B ₁₅
K	NC	CPAB ₃	\overline{OEAB}_2	\overline{OEBA}_2	CPBA ₃	NC
L	A ₁₆	\overline{CEA}_3	\overline{OEAB}_3	\overline{OEBA}_3	\overline{CEB}_3	B ₁₆
M	A ₁₈	A ₁₇	GND	GND	B ₁₇	B ₁₈
N	A ₂₀	A ₁₉	V _{CC2}	V _{CC2}	B ₁₉	B ₂₀
P	A ₂₂	A ₂₁	GND	GND	B ₂₁	B ₂₂
R	A ₂₄	A ₂₃	GND	GND	B ₂₃	B ₂₄
T	A ₂₆	A ₂₅	V _{CC2}	V _{CC2}	B ₂₅	B ₂₆
U	A ₂₈	A ₂₇	GND	GND	B ₂₇	B ₂₈
V	A ₂₉	A ₃₀	CPAB ₄	CPBA ₄	B ₃₀	B ₂₉
W	A ₃₁	\overline{CEA}_4	\overline{OEAB}_4	\overline{OEBA}_4	\overline{CEB}_4	B ₃₁

Truth Table

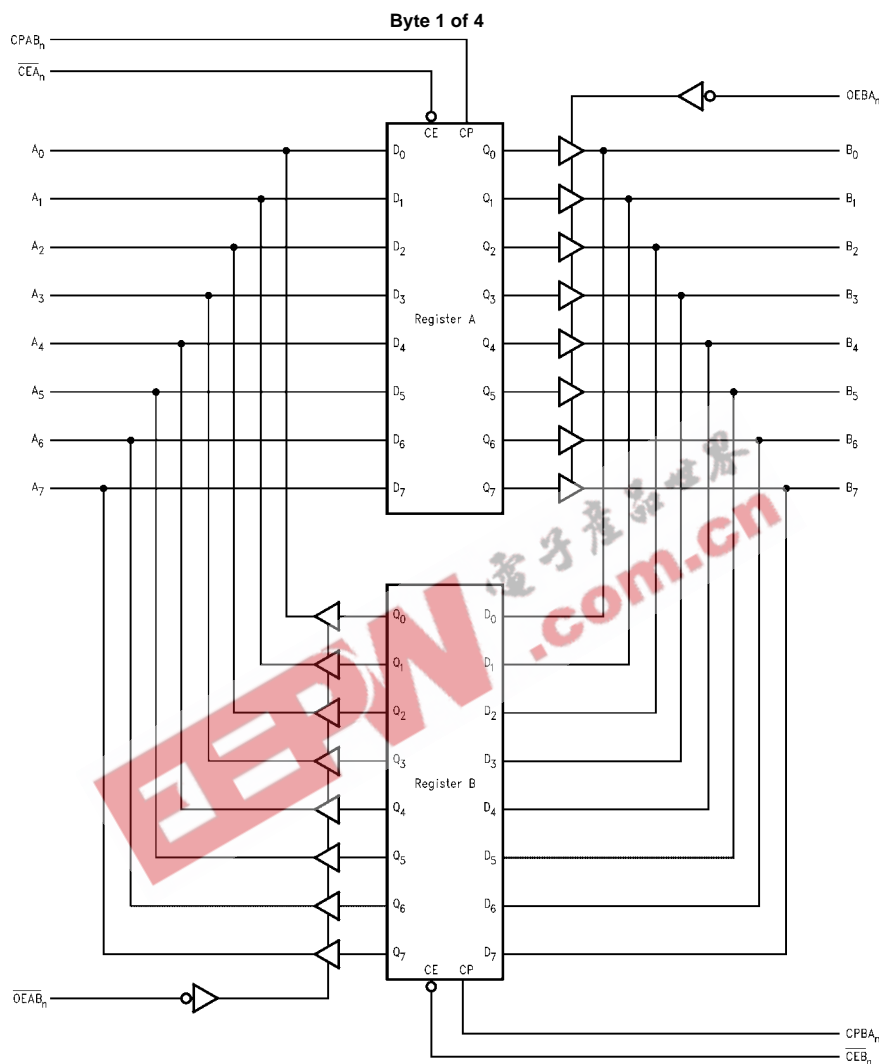
(Note 2)

Inputs				Internal Register	Output
A	CPAB _n	\overline{CEA}_n	\overline{OEAB}_n	Value	B
X	X	H	L	NC	B ₀
X	X	H	H	NC	Z
L	↗	L	L	L	L
L	↗	L	H	L	Z
H	↗	L	L	H	H
H	↗	L	H	H	Z
X	L	X	L	NC	B ₀
X	H	X	L	NC	B ₀
X	L	X	H	NC	Z
X	H	X	H	NC	Z

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = Output High Impedance
 ↗ = LOW-to-HIGH Transition.
 NC = No Change (state established by last valid CP)
 B₀ = State established by last valid CP

Note 2: A to B data flow shown; B to A flow control is the same, but uses \overline{OEBA}_n , CPBA_n and \overline{CEB}_n .

Logic Diagram



$n = 1$ for Byte 1, $n = 2$ for Byte 2, etc.

Byte 1: $A_0 - A_7, B_0 - B_7$

Byte 2: $A_8 - A_{15}, B_8 - B_{15}$

Byte 3: $A_{16} - A_{23}, B_{16} - B_{23}$

Byte 4: $A_{24} - A_{31}, B_{24} - B_{31}$

V_{CC1} is associated with Bytes 1 and 2

V_{CC2} is associated with Bytes 3 and 4

Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 3)				
Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	-0.5 to +4.6		V
V_I	DC Input Voltage	-0.5 to +7.0		V
V_O	DC Output Voltage	-0.5 to +7.0	Output in 3-STATE	V
		-0.5 to +7.0	Output in HIGH or LOW State (Note 4)	V
I_{IK}	DC Input Diode Current	-50	$V_I < GND$	mA
I_{OK}	DC Output Diode Current	-50	$V_O < GND$	mA
I_O	DC Output Current	64	$V_O > V_{CC}$ Output at HIGH State	mA
		128	$V_O > V_{CC}$ Output at LOW State	
I_{CC}	DC Supply Current per Supply Pin	± 64		mA
I_{GND}	DC Ground Current per Ground Pin	± 128		mA
T_{STG}	Storage Temperature	-65 to +150		$^{\circ}C$

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	2.7	3.6	V
V_I	Input Voltage	0	5.5	V
I_{OH}	HIGH Level Output Current		-32	mA
I_{OL}	LOW Level Output Current		64	
T_A	Free-Air Operating Temperature	-40	+85	$^{\circ}C$
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8V-2.0V$, $V_{CC} = 3.0V$	0	10	ns/V

Note 3: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

Note 4: I_O Absolute Maximum Rating must be observed.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = -40^{\circ}C$ to $+85^{\circ}C$		Units	Conditions	
			Min	Max			
V_{IK}	Input Clamp Diode Voltage	2.7		-1.2	V	$I_I = -18$ mA	
V_{IH}	Input HIGH Voltage	2.7-3.6	2.0		V	$V_O \leq 0.1V$ or	
V_{IL}	Input LOW Voltage	2.7-3.6		0.8		$V_O \geq V_{CC} - 0.1V$	
V_{OH}	Output HIGH Voltage	2.7-3.6	$V_{CC} - 0.2$		V	$I_{OH} = -100$ μA	
		2.7	2.4		V	$I_{OH} = -8$ mA	
		3.0	2.0		V	$I_{OH} = -32$ mA	
V_{OL}	Output LOW Voltage	2.7		0.2	V	$I_{OL} = 100$ μA	
		2.7		0.5	V	$I_{OL} = 24$ mA	
		3.0		0.4	V	$I_{OL} = 16$ mA	
		3.0		0.5	V	$I_{OL} = 32$ mA	
		3.0		0.55	V	$I_{OL} = 64$ mA	
$I_{I(HOLD)}$	Bushold Input Minimum Drive	3.0	75		μA	$V_I = 0.8V$	
			-75		μA	$V_I = 2.0V$	
$I_{I(OD)}$	Bushold Input Over-Drive Current to Change State	3.0	500		μA	(Note 5)	
			-500		μA	(Note 6)	
I_I	Input Current	3.6		10	μA	$V_I = 5.5V$	
		Control Pins	3.6		± 1	μA	$V_I = 0V$ or V_{CC}
					-5	μA	$V_I = 0V$
		Data Pins	3.6		1	μA	$V_I = V_{CC}$
I_{OFF}	Power Off Leakage Current	0		± 100	μA	$0V \leq V_I$ or $V_O \leq 5.5V$	
$I_{PU/PD}$	Power Up/Down 3-STATE Output Current	0-1.5V		± 100	μA	$V_O = 0.5V$ to $3.0V$ $V_I = GND$ or V_{CC}	
I_{OZL}	3-STATE Output Leakage Current	3.6		-5	μA	$V_O = 0.0V$	
I_{OZH}	3-STATE Output Leakage Current	3.6		5	μA	$V_O = 3.6V$	
I_{OZH^+}	3-STATE Output Leakage Current	3.6		10	μA	$V_{CC} < V_O \leq 5.5V$	

DC Electrical Characteristics (Continued)							
Symbol	Parameter	V _{CC} (V)	T _A = -40°C to +85°C		Units	Conditions	
			Min	Max			
I _{CCH}	Power Supply Current	V _{CC1} or V _{CC2}	3.6	0.19	mA	Outputs High	
I _{CCL}	Power Supply Current	V _{CC1} or V _{CC2}	3.6	5	mA	Outputs Low	
I _{CCZ}	Power Supply Current	V _{CC1} or V _{CC2}	3.6	0.19	mA	Outputs Disabled	
I _{CCZ+}	Power Supply Current	V _{CC1} or V _{CC2}	3.6	0.19	mA	V _{CC} ≤ V _O ≤ 5.5V, Outputs Disabled	
ΔI _{CC}	Increase in Power Supply Current (Note 7)	V _{CC1} or V _{CC2}	3.6	0.2	mA	One Input at V _{CC} - 0.6V Other Inputs at V _{CC} or GND	
<p>Note 5: An external driver must source at least the specified current to switch from LOW-to-HIGH.</p> <p>Note 6: An external driver must sink at least the specified current to switch from HIGH-to-LOW.</p> <p>Note 7: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.</p>							
Dynamic Switching Characteristics (Note 8)							
Symbol	Parameter	V _{CC} (V)	T _A = 25°C			Units	Conditions C _L = 50 pF, R _L = 500Ω
			Min	Typ	Max		
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3		0.8	V	(Note 9)	
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3		-0.8	V	(Note 9)	
<p>Note 8: Characterized in SSOP package. Guaranteed parameter, but not tested.</p> <p>Note 9: Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. Output under test held LOW.</p>							
AC Electrical Characteristics							
Symbol	Parameter	T _A = -40°C to +85°C C _L = 50 pF, R _L = 500Ω				Units	
		V _{CC} = 3.3 ± 0.3V		V _{CC} = 2.7V			
		Min	Max	Min	Max		
f _{MAX}	Maximum Clock Frequency	150		150		MHz	
t _{PLH}	Propagation Delay	1.3	4.4	1.3	4.7	ns	
t _{PHL}	CPBA or CPAB to A or B	1.3	4.8	1.3	5.0	ns	
t _{PZH}	Output Enable Time	1.0	4.3	1.0	4.9	ns	
t _{PZL}	$\overline{\text{OE}}$ to A or B	1.0	4.8	1.0	5.7	ns	
t _{PHZ}	Output Disable Time	2.1	5.7	2.1	6.2	ns	
t _{PLZ}	$\overline{\text{OE}}$ to A or B	2.1	5.1	2.1	5.3	ns	
t _W	Pulse Width, CPAB or CPBA HIGH or LOW	3.3		3.3		ns	
t _S	Setup Time	A or B before CPAB or CPBA	1.7		2.5	ns	
		CEA or CEB before CPAB or CPBA	2.0		2.8	ns	
t _H	Hold Time	A or B after CPAB or CPBA	0.8		0.0	ns	
		CEA or CEB after CPAB or CPBA	0.4		0.0	ns	
Capacitance (Note 10)							
Symbol	Parameter	Conditions	Typical	Units			
C _{IN}	Input Capacitance	V _{CC} = OPEN, V _I = 0V or V _{CC}	4	pF			
C _{I/O}	Input/Output Capacitance	V _{CC} = 3.0V, V _O = 0V or V _{CC}	8	pF			
<p>Note 10: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.</p>							

