

## 8-bit bus interface latch with set and reset (3-State)

### 74ABT845

#### FEATURES

- High speed parallel latches
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Broadside pinout
- Output capability: +64mA/-32mA
- Power-up 3-State
- Power-up reset
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

#### DESCRIPTION

The 74ABT845 consists of eight D-type latches with 3-State outputs. In addition to the LE, OE, MR and PRE pins, the 74ABT845 has two additional OE pins, making a total of three Output Enable (OE0, OE1, OE2) pins. The multiple Output enables allow multiuser control of the interface, e.g., CS, DMA, and RD/WR.

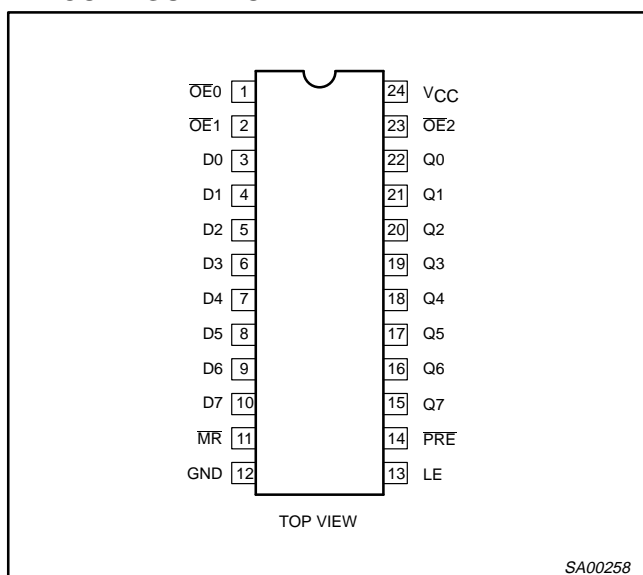
#### QUICK REFERENCE DATA

| SYMBOL                 | PARAMETER                     | CONDITIONS<br>$T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$ | TYPICAL | UNIT |
|------------------------|-------------------------------|--|---------|------|
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>Dn to Qn | $C_L = 50\text{pF}; V_{CC} = 5\text{V}$                              | 5.4     | ns   |
| $C_{IN}$               | Input capacitance             | $V_I = 0\text{V}$ or $V_{CC}$  | 4       | pF   |
| $C_{OUT}$              | Output capacitance            | Outputs disabled;<br>$V_O = 0\text{V}$ or $V_{CC}$                   | 7       | pF   |
| $I_{CCZ}$              | Total supply current          | Outputs disabled; $V_{CC} = 5.5\text{V}$                             | 500     | nA   |

#### ORDERING INFORMATION

| PACKAGES                    | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | DWG NUMBER |
|-----------------------------|-------------------|-----------------------|---------------|------------|
| 24-Pin Plastic DIP          | -40°C to +85°C    | 74ABT845 N            | 74ABT845 N    | SOT222-1   |
| 24-Pin plastic SO           | -40°C to +85°C    | 74ABT845 D            | 74ABT845 D    | SOT137-1   |
| 24-Pin Plastic SSOP Type II | -40°C to +85°C    | 74ABT845 DB           | 74ABT845 DB   | SOT340-1   |
| 24-Pin Plastic TSSOP Type I | -40°C to +85°C    | 74ABT845 PW           | 74ABT845PW DH | SOT355-1   |

#### PIN CONFIGURATION



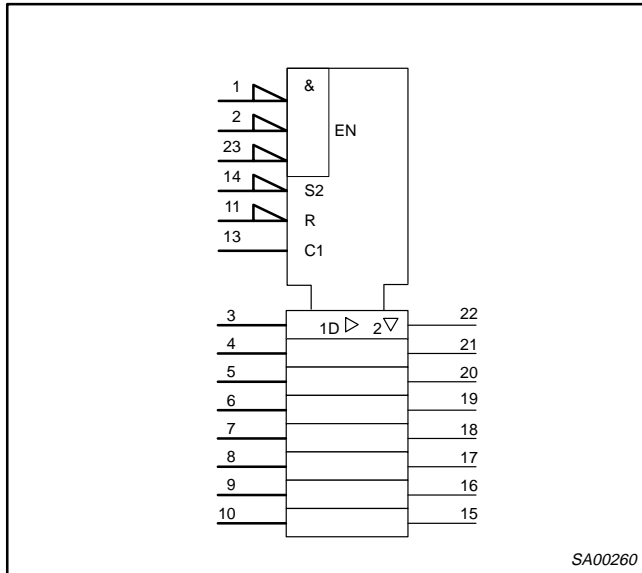
#### PIN DESCRIPTION

| PIN NUMBER                     | SYMBOL    | FUNCTION                          |
|--------------------------------|-----------|-----------------------------------|
| 1, 2, 23                       | OE0 – OE2 | Output enable inputs (active-Low) |
| 3, 4, 5, 6, 7, 8, 9, 10        | D0-D7     | Data inputs                       |
| 22, 21, 20, 19, 18, 17, 16, 15 | Q0-Q7     | Data outputs                      |
| 11                             | MR        | Master reset input (active-Low)   |
| 13                             | LE        | Latch enable input (active-High)  |
| 14                             | PRE       | Preset input (active-Low)         |
| 12                             | GND       | Ground (0V)                       |
| 24                             | VCC       | Positive supply voltage           |

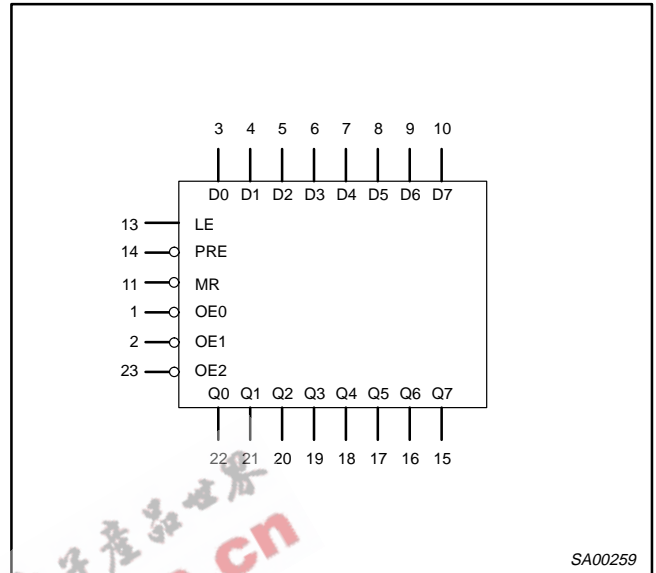
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### LOGIC SYMBOL (IEEE/IEC)



### LOGIC SYMBOL

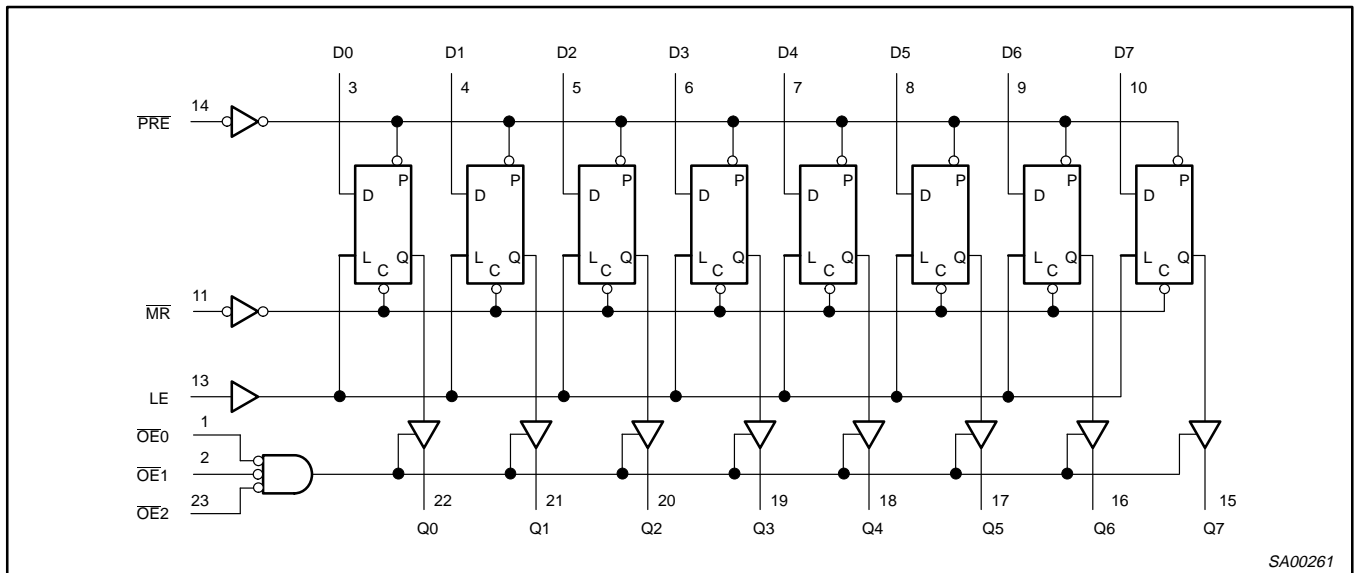


### FUNCTION TABLE

| INPUTS          |                 |    |    |                | OUTPUTS        | OPERATING MODE |
|-----------------|-----------------|----|----|----------------|----------------|----------------|
| OE <sub>n</sub> | PR <sub>E</sub> | MR | LE | D <sub>n</sub> | Q <sub>n</sub> |                |
| L               | L               | X  | X  | X              | H              | Preset         |
| L               | H               | L  | X  | X              | L              | Clear          |
| L               | H               | H  | H  | L              | L              | Transparent    |
| L               | H               | H  | H  | H              | H              |                |
| L               | H               | H  | ↓  | l              | L              | Latched        |
| L               | H               | H  | ↓  | h              | H              |                |
| H               | X               | X  | X  | X              | Z              | High impedance |
| L               | H               | H  | L  | X              | NC             | Hold           |

H = High voltage level  
 h = High voltage level one set-up time prior to the High-to-Low LE transition  
 L = Low voltage level  
 l = Low voltage level one set-up time prior to the High-to-Low LE transition  
 NC= No change  
 X = Don't care  
 Z = High impedance "off" state  
 ↓ = High-to-Low transition

### LOGIC DIAGRAM



# 8-bit bus interface latch with set and reset (3-State)

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## ABSOLUTE MAXIMUM RATINGS<sup>1,2</sup>

| SYMBOL    | PARAMETER                      | CONDITIONS                  | RATING       | UNIT |
|-----------|--------------------------------|-----------------------------|--------------|------|
| $V_{CC}$  | DC supply voltage              |                             | -0.5 to +7.0 | V    |
| $I_{IK}$  | DC input diode current         | $V_I < 0$                   | -18          | mA   |
| $V_I$     | DC input voltage <sup>3</sup>  |                             | -1.2 to +7.0 | V    |
| $I_{OK}$  | DC output diode current        | $V_O < 0$                   | -50          | mA   |
| $V_{OUT}$ | DC output voltage <sup>3</sup> | output in Off or High state | -0.5 to +5.5 | V    |
| $I_{OUT}$ | DC output current              | output in Low state         | 128          | mA   |
| $T_{stg}$ | Storage temperature range      |                             | -65 to 150   | °C   |

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL              | PARAMETER                            | LIMITS |          | UNIT |
|---------------------|--------------------------------------|--------|----------|------|
|                     |                                      | Min    | Max      |      |
| $V_{CC}$            | DC supply voltage                    | 4.5    | 5.5      | V    |
| $V_I$               | Input voltage                        | 0      | $V_{CC}$ | V    |
| $V_{IH}$            | High-level input voltage             | 2.0    |          | V    |
| $V_{IL}$            | Low-level input voltage              |        | 0.8      | V    |
| $I_{OH}$            | High-level output current            |        | -32      | mA   |
| $I_{OL}$            | Low-level output current             |        | 64       | mA   |
| $\Delta t/\Delta v$ | Input transition rise or fall rate   | 0      | 5        | ns/V |
| $T_{amb}$           | Operating free-air temperature range | -40    | +85      | °C   |

# 8-bit bus interface latch with set and reset (3-State)

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## DC ELECTRICAL CHARACTERISTICS

| SYMBOL             | PARAMETER  | TEST CONDITIONS  | LIMITS                   |       |      |                                   |      | UNIT |
|--------------------|--|--|--------------------------|-------|------|-----------------------------------|------|------|
|                    |  |  | T <sub>amb</sub> = +25°C |       |      | T <sub>amb</sub> = -40°C to +85°C |      |      |
|                    |  |  | Min                      | Typ   | Max  | Min                               | Max  |      |
| V <sub>IK</sub>    | Input clamp voltage                                  | V <sub>CC</sub> = 4.5V; I <sub>IK</sub> = -18mA  |                          | -0.9  | -1.2 |                                   | -1.2 | V    |
| V <sub>OH</sub>    | High-level output voltage                            | V <sub>CC</sub> = 4.5V; I <sub>OH</sub> = -3mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>                        | 2.5                      | 2.9   |      | 2.5                               |      | V    |
|                    |  | V <sub>CC</sub> = 5.0V; I <sub>OH</sub> = -3mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>                        | 3.0                      | 3.4   |      | 3.0                               |      | V    |
|                    |  | V <sub>CC</sub> = 4.5V; I <sub>OH</sub> = -32mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>                       | 2.0                      | 2.4   |      | 2.0                               |      | V    |
| V <sub>OL</sub>    | Low-level output voltage                             | V <sub>CC</sub> = 4.5V; I <sub>OL</sub> = 64mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>                        |                          | 0.42  | 0.55 |                                   | 0.55 | V    |
| V <sub>RST</sub>   | Power-up output low voltage <sup>3</sup>             | V <sub>CC</sub> = 5.5V; I <sub>O</sub> = 1mA; V <sub>I</sub> = GND or V <sub>CC</sub>                                      |                          | 0.13  | 0.55 |                                   | 0.55 | V    |
| I <sub>I</sub>     | Input leakage current                                | V <sub>CC</sub> = 5.5V; V <sub>I</sub> = GND or 5.5V   |                          | ±0.01 | ±1.0 |                                   | ±1.0 | μA   |
| I <sub>OFF</sub>   | Power-off leakage current                            | V <sub>CC</sub> = 0.0V; V <sub>O</sub> or V <sub>I</sub> ≤ 4.5V  |                          | ±5.0  | ±100 |                                   | ±100 | μA   |
| I <sub>PU/PD</sub> | Power-up/down 3-state output current <sup>4</sup>    | V <sub>CC</sub> = 2.1V; V <sub>O</sub> = 0.5V; V <sub>OE</sub> = V <sub>CC</sub> ; V <sub>I</sub> = GND or V <sub>CC</sub> |                          | ±5.0  | ±50  |                                   | ±50  | μA   |
| I <sub>OZH</sub>   | 3-State output High current                          | V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 2.7V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>                         |                          | 5.0   | 50   |                                   | 50   | μA   |
| I <sub>OZL</sub>   | 3-State output Low current                           | V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 0.5V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>                         |                          | -5.0  | -50  |                                   | -50  | μA   |
| I <sub>CEX</sub>   | Output High leakage current                          | V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 5.5V; V <sub>I</sub> = GND or V <sub>CC</sub>                                     |                          | 5.0   | 50   |                                   | 50   | μA   |
| I <sub>O</sub>     | Output current <sup>1</sup>                          | V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 2.5V  | -50                      | -80   | -180 | -50                               | -180 | mA   |
| I <sub>CCH</sub>   | Quiescent supply current                             | V <sub>CC</sub> = 5.5V; Outputs High, V <sub>I</sub> = GND or V <sub>CC</sub>  |                          | 0.5   | 250  |                                   | 250  | μA   |
| I <sub>CCL</sub>   |  | V <sub>CC</sub> = 5.5V; Outputs Low, V <sub>I</sub> = GND or V <sub>CC</sub>   |                          | 24    | 30   |                                   | 30   | mA   |
| I <sub>CCZ</sub>   |  | V <sub>CC</sub> = 5.5V; Outputs 3-State; V <sub>I</sub> = GND or V <sub>CC</sub>   |                          | 0.5   | 250  |                                   | 250  | μA   |
| ΔI <sub>CC</sub>   | Additional supply current per input pin <sup>2</sup> | V <sub>CC</sub> = 5.5V; one input at 3.4V, other inputs at V <sub>CC</sub> or GND  |                          | 0.5   | 1.5  |                                   | 1.5  | mA   |

### NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This parameter is valid for any V<sub>CC</sub> between 0V and 2.1V with a transition time of up to 10msec. For V<sub>CC</sub> = 2.1V to V<sub>CC</sub> = 5V ± 10%, a transition time of up to 100μsec is permitted.

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74ABT845

## AC CHARACTERISTICS

GND = 0V,  $t_R = t_F = 2.5\text{ns}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 500\Omega$ 

| SYMBOL                               | PARAMETER                        | WAVEFORM | LIMITS   |            |            |  |            | UNIT |
|--------------------------------------|----------------------------------|----------|--|------------|------------|--|------------|------|
|                                      |                                  |          | $T_{\text{amb}} = +25^\circ\text{C}$<br>$V_{\text{CC}} = +5.0\text{V}$ |            |            | $T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$<br>$V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$ |            |      |
|                                      |                                  |          | Min  | Typ        | Max        | Min  | Max        |      |
| $t_{\text{PLH}}$<br>$t_{\text{PHL}}$ | Propagation delay<br>Dn to Qn    | 1        | 1.0<br>2.2   | 3.9<br>5.4 | 5.4<br>6.8 | 1.0<br>2.2   | 6.2<br>7.8 | ns   |
| $t_{\text{PLH}}$<br>$t_{\text{PHL}}$ | Propagation delay<br>LE to Qn    | 2        | 2.0<br>2.8   | 5.1<br>6.4 | 6.6<br>7.9 | 2.0<br>2.8   | 7.5<br>8.9 | ns   |
| $t_{\text{PLH}}$<br>$t_{\text{PHL}}$ | Propagation delay<br>PRE to Qn   | 1        | 2.2<br>3.0   | 4.9<br>5.3 | 6.6<br>6.8 | 2.2<br>3.0   | 7.8<br>7.4 | ns   |
| $t_{\text{PLH}}$<br>$t_{\text{PHL}}$ | Propagation delay<br>MR to Qn    | 1        | 2.4<br>3.1   | 4.9<br>5.9 | 6.4<br>7.3 | 2.4<br>3.1   | 7.3<br>8.5 | ns   |
| $t_{\text{PZH}}$<br>$t_{\text{PZL}}$ | Output enable time<br>OEn to Qn  | 4<br>5   | 1.0<br>2.0   | 3.8<br>4.7 | 5.4<br>6.1 | 1.0<br>2.0   | 6.3<br>6.7 | ns   |
| $t_{\text{PHZ}}$<br>$t_{\text{PLZ}}$ | Output disable time<br>OEn to Qn | 4<br>5   | 1.9<br>2.2   | 4.6<br>4.7 | 6.2<br>6.4 | 1.9<br>2.2   | 7.2<br>7.0 | ns   |

## AC SETUP REQUIREMENTS

GND = 0V,  $t_R = t_F = 2.5\text{ns}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 500\Omega$ 

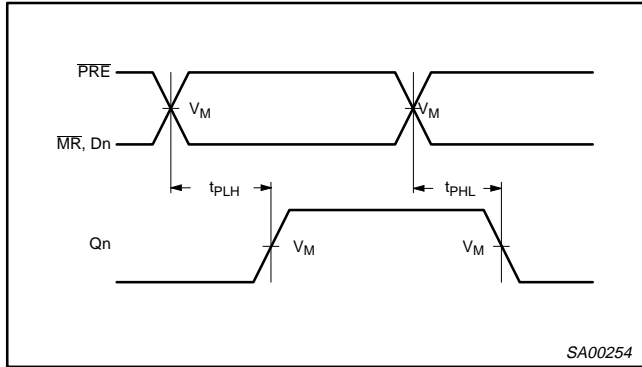
| SYMBOL                                 | PARAMETER                           | WAVEFORM | LIMITS   |              |  | UNIT |
|--|-------------------------------------|----------|--|--------------|--|------|
|  |                                     |          | $T_{\text{amb}} = +25^\circ\text{C}$<br>$V_{\text{CC}} = +5.0\text{V}$ |              | $T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$<br>$V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$ |      |
|  |                                     |          | Min  | Typ          | Min  |      |
| $t_{\text{s(H)}}$<br>$t_{\text{s(L)}}$ | Setup time, High or Low<br>Dn to LE | 3        | 2.8<br>3.5   | 1.0<br>1.4   | 2.8<br>3.5   | ns   |
| $t_{\text{h(H)}}$<br>$t_{\text{h(L)}}$ | Hold time, High or Low<br>Dn to LE  | 3        | 1.0<br>1.0   | -1.2<br>-0.6 | 1.0<br>1.0   | ns   |
| $t_{\text{w(H)}}$                      | LE pulse width, High                | 3        | 3.0  | 1.5          | 3.0  | ns   |
| $t_{\text{w(L)}}$                      | PRE pulse width, Low                | 6        | 3.5  | 2.0          | 3.5  | ns   |
| $t_{\text{w(L)}}$                      | MR pulse width, Low                 | 6        | 2.8  | 1.3          | 2.8  | ns   |
| $t_{\text{rec}}$                       | PRE recovery time                   | 6        | 3.0  | 1.4          | 3.0  | ns   |
| $t_{\text{rec}}$                       | MR recovery time                    | 6        | 3.4  | 1.6          | 3.4  | ns   |

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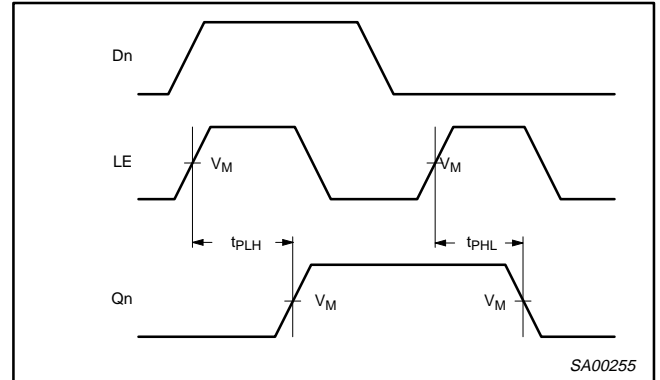
74ABT845

## AC WAVEFORMS

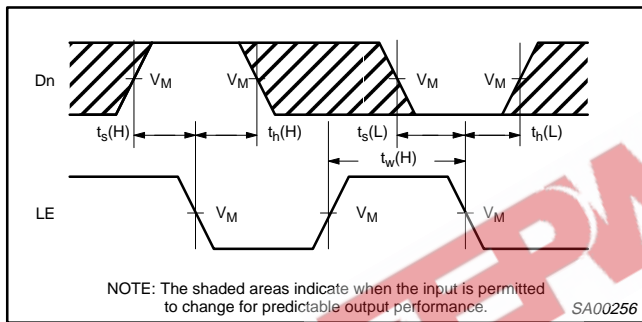
NOTE: For all waveforms,  $V_M = 1.5V$ .



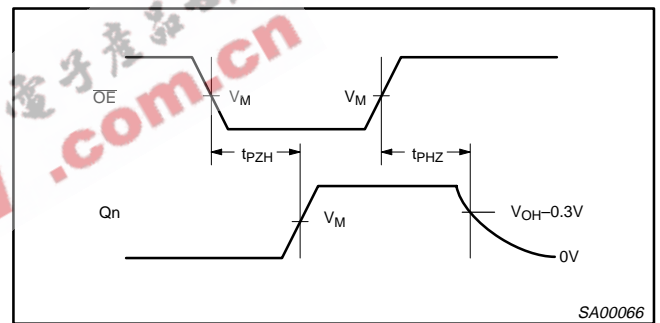
Waveform 1. Propagation Delay, Data to Output, Preset to Output, and Master Reset to Output



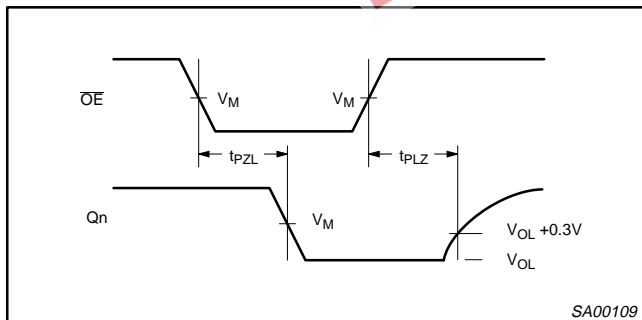
Waveform 2. Propagation Delay, Latch Enable to Output



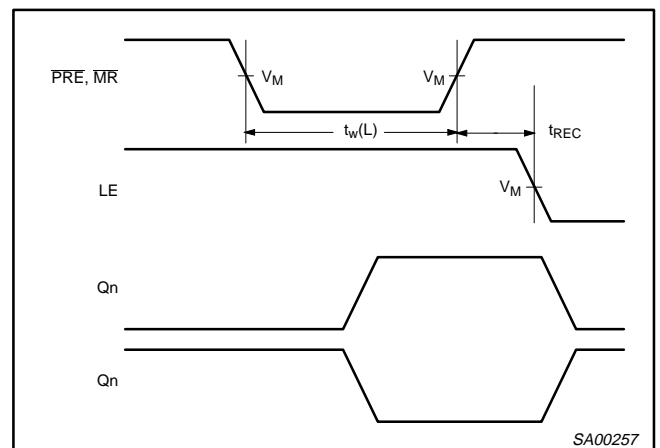
Waveform 3. Data Setup and Hold Times and Latch Enable Pulse Width



Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



Waveform 6. Master Reset and Preset Pulse Width and Master Reset and Preset to Latch Enable Recovery Time

# 8-bit bus interface latch with set and reset (3-State)

74ABT845

## TEST CIRCUIT AND WAVEFORM

**Test Circuit for 3-State Outputs**

**Input Pulse Definition**

$V_M = 1.5V$

**SWITCH POSITION**

| TEST      | SWITCH |
|-----------|--------|
| $t_{PLZ}$ | closed |
| $t_{PZL}$ | closed |
| All other | open   |

**DEFINITIONS**

$R_L$  = Load resistor; see AC CHARACTERISTICS for value.

$C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

$R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

| FAMILY | INPUT PULSE REQUIREMENTS |           |       |       |       |
|--------|--------------------------|-----------|-------|-------|-------|
|        | Amplitude                | Rep. Rate | $t_W$ | $t_R$ | $t_F$ |
| 74ABT  | 3.0V                     | 1MHz      | 500ns | 2.5ns | 2.5ns |

SA00012