

# 74ACT11543 OCTAL REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS136 – D3608, JULY 1990 – REVISED APRIL 1993

- Inputs Are TTL-Voltage Compatible
- 3-State True Outputs
- Back-to-Back Registers for Storage
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin  $V_{CC}$  and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C

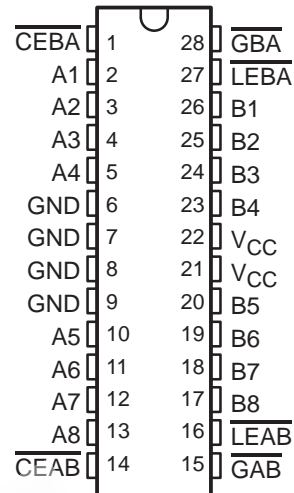
## description

This 8-bit registered transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch enable ( $\overline{LEAB}$  or  $\overline{LEBA}$ ) and output enable ( $\overline{GAB}$  or  $\overline{GBA}$ ) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ( $\overline{CEAB}$ ) input must be low in order to enter data from A or to output data to B. Having  $\overline{CEAB}$  low and  $\overline{LEAB}$  low makes the A-to-B latches transparent; a subsequent low-to-high transition of  $\overline{LEAB}$  puts the A latches in the storage mode. With  $\overline{CEAB}$  and  $\overline{GAB}$  both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B-to-A is similar, but requires the use of  $\overline{CEBA}$ ,  $\overline{LEBA}$ , and  $\overline{GBA}$  inputs.

The 74ACT11543 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

DW PACKAGE  
(TOP VIEW)



FUNCTION TABLE

INPUTS			LATCH STATUS A TO B†	OUTPUT BUFFERS B1 THRU B8
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{GAB}$		
H	X	X	Storing	Z
X	H		Storing	
X		H		Z
L	L	L	Transparent	Current A Data
L	H	L	Storing	Previous‡ A Data

† A-to-B data flow is shown: B-to-A flow control is the same except uses  $\overline{CEBA}$ ,  $\overline{LEBA}$ , and  $\overline{GBA}$ .

‡ Data present before low-to-high transition of  $\overline{LEAB}$ .

EPIC is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



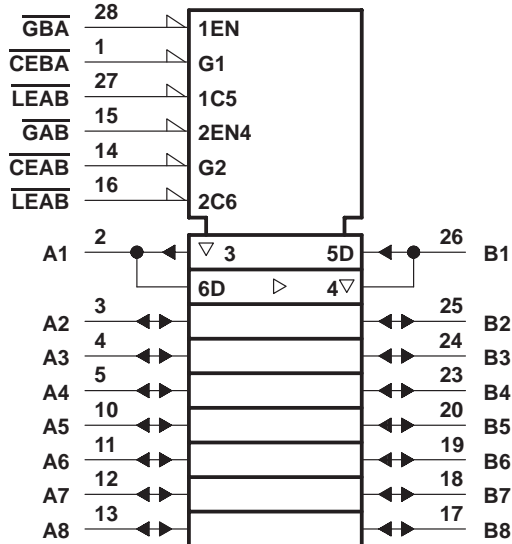
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1993, Texas Instruments Incorporated

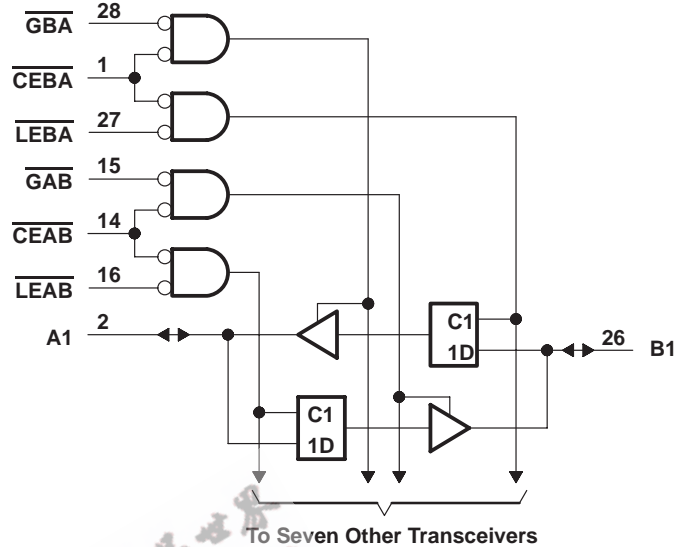
# 74ACT11543 OCTAL REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS136 – D3608, JULY 1990 – REVISED APRIL 1993

## logic symbol†



## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND	$\pm 200$ mA
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## recommended operating conditions

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	2			V
$V_{IL}$ Low-level input voltage			0.8	V
$V_I$ Input voltage	0		$V_{CC}$	V
$V_O$ Output voltage	0		$V_{CC}$	V
$I_{OH}$ High-level output current			-24	mA
$I_{OL}$ Low-level output current			24	mA
$\Delta t/\Delta v$ Input transition rise or fall rate	0		10	ns/V
$T_A$ Operating free-air temperature	-40		85	°C

**74ACT11543**  
**OCTAL REGISTERED TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

SCAS136 – D3608, JULY 1990 – REVISED APRIL 1993

**electrical characteristics over recommended operating free-air temperature range**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT	
			MIN	TYP	MAX				
V <sub>OH</sub>	I <sub>OH</sub> = – 50 μA	4.5 V	4.4			4.4		V	
		5.5 V	5.4			5.4			
	I <sub>OH</sub> = – 24 mA	4.5 V	3.94			3.8			
		5.5 V	4.94			4.8			
I <sub>OH</sub> = – 75 mA <sup>†</sup>	5.5 V				3.85				
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V	0.1			0.1		V	
		5.5 V	0.1			0.1			
	I <sub>OL</sub> = 24 mA	4.5 V	0.36			0.44			
		5.5 V	0.36			0.44			
I <sub>OL</sub> = 75 mA <sup>†</sup>	5.5 V				1.65				
I <sub>I</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V	± 0.1			± 1		μA
I <sub>OZ</sub>	A or B ports <sup>‡</sup>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V	± 0.5			± 5		μA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V	8			80		μA
ΔI <sub>CC</sub> <sup>§</sup>		One input at 3.4 V, Other inputs at GND or V <sub>CC</sub>	5.5 V	0.9			1		mA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V	4.5					pF
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V	12					pF

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

<sup>‡</sup> For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

<sup>§</sup> This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)**

		T <sub>A</sub> = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t <sub>w</sub>	Pulse duration, $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$ low	4		4		ns
t <sub>su</sub>	Setup time	Data after $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}\uparrow$		2.5		ns
		Data before $\overline{\text{CEAB}}$ or $\overline{\text{CEBA}}\uparrow$		3		
t <sub>h</sub>	Hold time	Data after $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}\uparrow$		2		ns
		Data after $\overline{\text{CEAB}}$ or $\overline{\text{CEBA}}\uparrow$		1.5		

**74ACT11543**  
**OCTAL REGISTERED TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

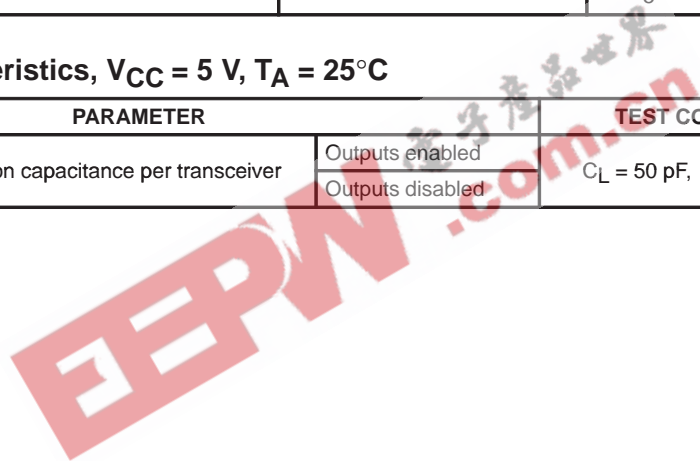
SCAS136 – D3608, JULY 1990 – REVISED APRIL 1993

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t <sub>PLH</sub>	A or B	B or A	3.5	6.2	9.1	3.5	10.2	ns
t <sub>PHL</sub>			3.2	6.5	10.8	3.2	12.1	
t <sub>PLH</sub>	LEBA or LEAB	A or B	3	6.1	10.1	3	11.2	ns
t <sub>PHL</sub>			3.7	7.2	11.7	3.7	13.2	
t <sub>PZH</sub>	$\overline{\text{CEBA}}$ or $\overline{\text{CEAB}}$	A or B	3.5	6.7	11.1	3.5	12.2	ns
t <sub>PZL</sub>			3.2	8.4	13.4	3.2	16	
t <sub>PHZ</sub>	$\overline{\text{CEBA}}$ or $\overline{\text{CEAB}}$	A or B	4.8	7.3	10.1	4.8	11	ns
t <sub>PLZ</sub>			5.1	7.5	10.3	5.1	11.1	
t <sub>PZH</sub>	$\overline{\text{GBA}}$ or $\overline{\text{GAB}}$	A or B	3.3	6.4	10.5	3.3	11.5	ns
t <sub>PZL</sub>			3	8	12.8	3	15.3	
t <sub>PHZ</sub>	$\overline{\text{GBA}}$ or $\overline{\text{GAB}}$	A or B	4.6	6.9	9.6	4.6	10.4	ns
t <sub>PLZ</sub>			5	7.1	9.8	5	10.5	

operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

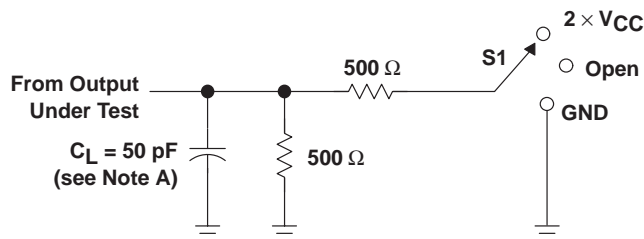
PARAMETER		TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per transceiver	C <sub>L</sub> = 50 pF, f = 1 MHz	47	pF
			13	



# 74ACT11543 OCTAL REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

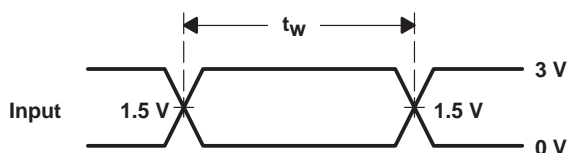
SCAS136 – D3608, JULY 1990 – REVISED APRIL 1993

## PARAMETER MEASUREMENT INFORMATION

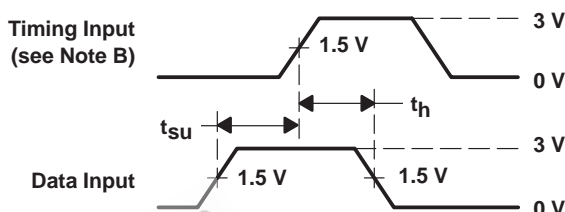


LOAD CIRCUIT

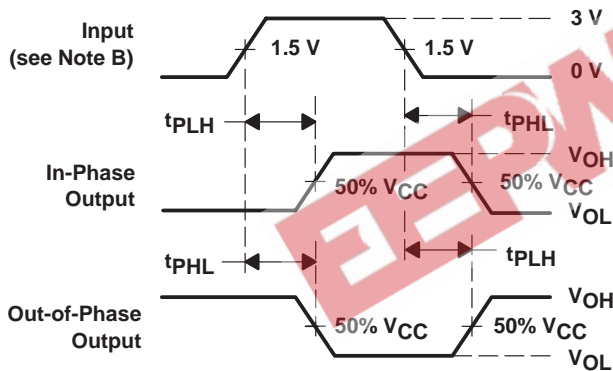
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



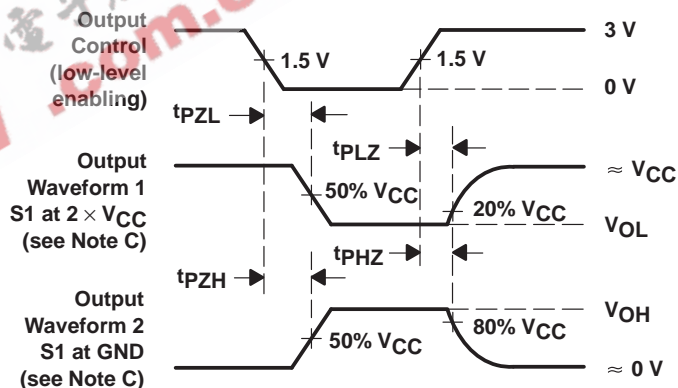
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ .  
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

EEPW 电子产品世界  
.com.cn

## IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.