

DATA SHEET

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74ALVT16260

12-bit to 24-bit multiplexed D-type latches
(3-State)

Product specification
IC23 Data Handbook

1998 Jan 30

2.5V/3.3V 12-bit to 24-bit multiplexed D-type latches (3-State)

74ALVT16260

FEATURES

- ESD protection exceeds 2000V per Mil-Std-883C, Method 3015; exceeds 200V using machine model
- Latch-up protection exceeds 500mA per JEDEC Standard JESD-17.
- Distributed V_{CC} and GND pin configuration minimizes high-speed switching noise.
- Output capability ($-32\text{mA } I_{OH}$, $64\text{mA } I_{OL}$).
- Bus hold inputs eliminate the need for external pull-up resistors.
- 5V I/O compatible
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up Reset

DESCRIPTION

The 74ALVT16260 is a 12-bit to 24-bit multiplexed D-type latch used in applications where two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing of address and data information in microprocessor or bus-interface applications. This device is also useful in memory-interleaving applications.

Three 12-bit I/O ports (A1–A12, 1B1–1B12, and 2B1–2B12) are available for address and/or data transfer. The output enable ($\overline{OE1B}$, $\overline{OE2B}$, and $\overline{OE A}$) inputs control the bus transceiver functions. The $\overline{OE1B}$ and $\overline{OE2B}$ control signals also allow bank control in the A to B direction.

Address and/or data information can be stored using the internal storage latches. The latch enable (LE1B, LE2B, LEA1B, and LEA2B) inputs are used to control data storage. When the latch enable input is high, the latch is transparent. When the latch enable input goes low, the data present at the inputs is latched and remains latched until the latch enable input is returned high.

To ensure the high-impedance state during power-up or power-down, \overline{OE} should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current sinking capability of the driver.

The 74ALVT16260 is available in a 56-pin Shrink Small Outline Package (SSOP) and 56-pin Thin Shrink Small Outline Package (TSSOP).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH}	Propagation delay	$C_L = 50 \text{ pF}$	3.5	2.8	ns
t_{PHL}	nAx to nBx nBx to nAx		3.3	2.6	
C_{IN}	Input capacitance	$V_I = 0 \text{ V or } V_{CC}$	4	4	pF
C_{OUT}	Output capacitance	$V_{IO} = 0 \text{ V or } 5.0 \text{ V}$	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	100	80	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	$-40^{\circ}\text{C to } +85^{\circ}\text{C}$	74ALVT16260 DL	AV16260 DL	SOT371-1
56-Pin Plastic TSSOP Type II	$-40^{\circ}\text{C to } +85^{\circ}\text{C}$	74ALVT16260 DGG	AV16260 DGG	SOT364-1

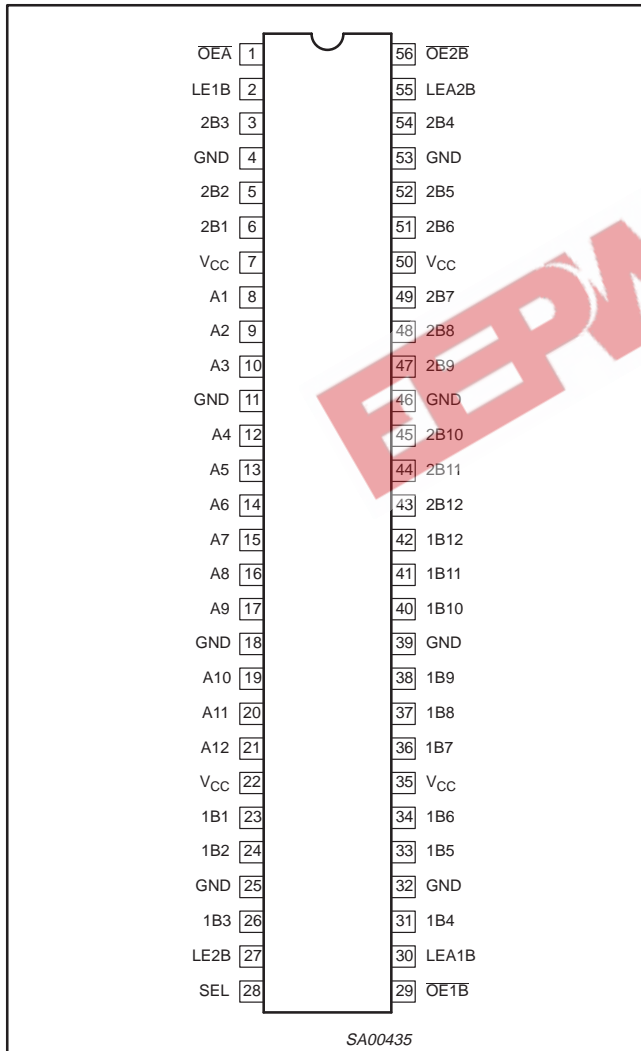
2.5V/3.3V 12-bit to 24-bit multiplexed D-type latches (3-State)

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PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21	A _n	Data inputs/outputs (A)
23, 24, 26, 31, 33, 34, 36, 37, 38, 40, 41, 42	1B _n	Data inputs/outputs (B1)
6, 5, 3, 54, 52, 51, 49, 48, 47, 45, 44, 43	2B _n	Data inputs/outputs (B2)
1, 29, 56	$\overline{OE}A$, $\overline{OE}1B$, $\overline{OE}2B$	Output enable input (active low)
2, 27, 30, 55	LE1B, LE2B, LEA1B, LEA2B	Latch enable inputs
28	SEL	B1/B2 input select input
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V _{CC}	Positive supply voltage

PIN CONFIGURATION



FUNCTION TABLES

B to A ($\overline{OE}B = H$)

INPUTS						OUTPUT
1B	2B	SEL	LE1B	LE2B	$\overline{OE}A$	A
H	X	H	H	X	L	H
L	X	H	H	X	L	L
X	X	H	L	X	L	A0
X	H	L	X	H	L	H
X	L	L	X	H	L	L
X	X	L	X	L	L	A0
X	X	X	X	X	H	Z

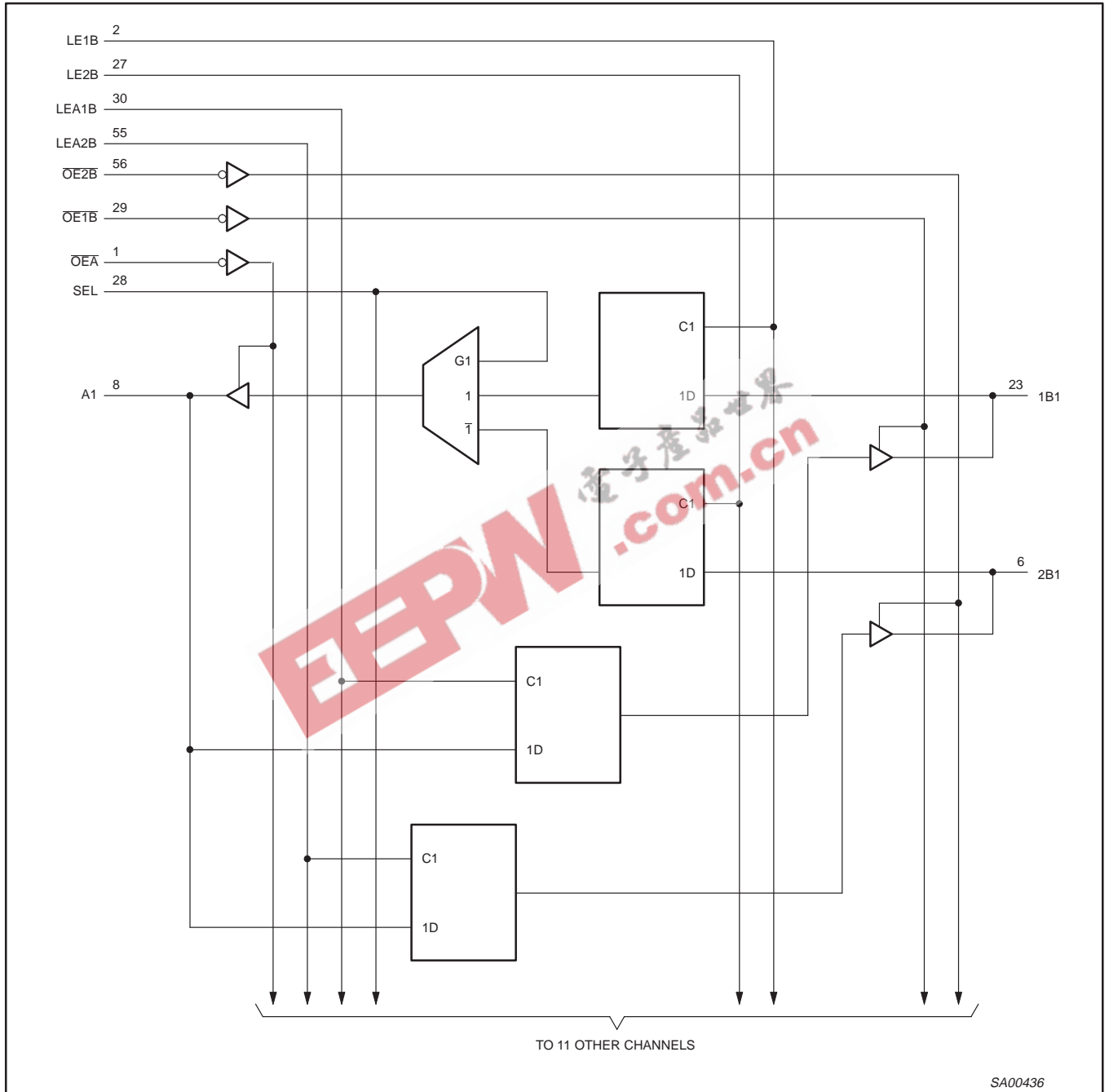
A to B ($\overline{OE}A = H$)

INPUTS					OUTPUT	
A	LEA1B	LEA2B	$\overline{OE}1B$	$\overline{OE}2B$	1B	2B
H	H	H	L	L	H	H
L	H	H	L	L	L	L
H	H	L	L	L	H	2B0
L	H	L	L	L	L	2B0
H	L	H	L	L	1B0	H
L	L	H	L	L	1B0	L
X	L	L	L	L	1B0	2B0
X	X	X	H	H	Z	Z
X	X	X	L	H	Active	Z
X	X	X	H	L	Z	Active
X	X	X	L	L	Active	Active

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LOGIC DIAGRAM (POSITIVE LOGIC)



2.5V/3.3V 12-bit to 24-bit multiplexed D-type latches (3-State)

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ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage ³		-0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage ³	Output in Off or High state	-0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		-8		-32	mA
I_{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle $\leq 50\%$; $f \geq 1$ kHz		24		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	-40	+85	°C

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DC ELECTRICAL CHARACTERISTICS (3.3V ± 0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 3.0V; I _{IK} = -18mA		-0.85	-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 3.0 to 3.6V; I _{OH} = -100µA	V _{CC} -0.2	V _{CC}		V
		V _{CC} = 3.0V; I _{OH} = -32mA	2.0	2.3		
V _{OL}	Low-level output voltage	V _{CC} = 3.0V; I _{OL} = 100µA		0.07	0.2	V
		V _{CC} = 3.0V; I _{OL} = 16mA		0.25	0.4	
		V _{CC} = 3.0V; I _{OL} = 32mA		0.3	0.5	
		V _{CC} = 3.0V; I _{OL} = 64mA		0.4	0.55	
V _{RST}	Power-up output low voltage ⁶	V _{CC} = 3.6V; I _O = 1mA; V _I = V _{CC} or GND			0.55	V
I _I	Input leakage current	V _{CC} = 3.6V; V _I = V _{CC} or GND	Control pins	0.1	±1	µA
		V _{CC} = 0 or 3.6V; V _I = 5.5V		0.1	10	
		V _{CC} = 3.6V; V _I = V _{CC}	Data pins ⁴	0.1	1	
		V _{CC} = 3.6V; V _I = 0V		0.1	-5	
I _{OFF}	Off current	V _{CC} = 0V; V _I or V _O = 0 to 4.5V		0.1	±100	µA
I _{HOLD}	Bus Hold current Data inputs ⁷	V _{CC} = 3V; V _I = 0.8V	75	130		µA
		V _{CC} = 3V; V _I = 2.0V	-75	-140		
		V _{CC} = 0V to 3.6V; V _{CC} = 3.6V	±500			
I _{EX}	Current into an output in the High state when V _O > V _{CC}	V _O = 5.5V; V _{CC} = 3.0V		10	125	µA
I _{PU/PD}	Power up/down 3-State output current ³	V _{CC} ≤ 1.2V; V _O = 0.5V to V _{CC} ; V _I = GND or V _{CC} OE/OE = Don't care		1	±100	µA
I _{OZH}	3-State output High current	V _{CC} = 3.6V; V _O = 3.0V; V _I = V _{IL} or V _{IH}		0.5	5	µA
I _{OZL}	3-State output Low current	V _{CC} = 3.6V; V _O = 0.5V; V _I = V _{IL} or V _{IH}		0.5	-5	µA
I _{CCH}	Quiescent supply current	V _{CC} = 3.6V; Outputs High, V _I = GND or V _{CC} , I _O = 0		0.04	0.1	mA
I _{CCL}		V _{CC} = 3.6V; Outputs Low, V _I = GND or V _{CC} , I _O = 0		3.7	6	
I _{CCZ}		V _{CC} = 3.6V; Outputs Disabled; V _I = GND or V _{CC} , I _O = 0 ⁵		0.04	0.1	
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 3V to 3.6V; One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND		0.04	0.4	mA

NOTES:

- All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
- This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
- This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.2V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
- Unused pins at V_{CC} or GND.
- I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

2.5V/3.3V 12-bit to 24-bit multiplexed D-type latches (3-State)

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AC ELECTRICAL CHARACTERISTICS (3.3V ± 0.3V RANGE)

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$

SYMBOL	PARAMETER		$T_{\text{amb}} = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{\text{CC}} = +3.3\text{V} \pm 0.3\text{V}$			UNIT
	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	
t_{PLH}	A or B	B or A	1	2.8	4.8	ns
t_{PHL}			1	2.6	4.6	ns
t_{PLH}	$\overline{\text{LE}}$	A or B	1.1	2.9	4.6	ns
t_{PHL}			1.1	3.1	4.7	ns
t_{PLH}	SEL (B1)	A	1.3	2.3	3.4	ns
	SEL (B2)	A	1.1	2.4	3.8	ns
t_{PHL}	SEL (B1)	A	1.5	2.4	3.6	ns
	SEL (B2)	A	1.6	2.4	3.6	ns
t_{PZH}	$\overline{\text{OE}}$	A or B	1	2.3	4.2	ns
t_{PZL}			1.6	2.3	4.0	ns
t_{PHZ}	$\overline{\text{OE}}$	A or B	2.2	4.4	6.0	ns
t_{PLZ}			1.3	3.1	5.0	ns

AC SETUP CHARACTERISTICS (3.3V ± 0.3V RANGE)

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$

SYMBOL	PARAMETER	$T_{\text{amb}} = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{\text{CC}} = +3.3\text{V} \pm 0.3\text{V}$		UNIT
		MIN	MAX	
t_w	Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high	3.3		ns
t_{su}	Setup time, data before LE1B, LE2B, LEA1B, or LEA2B↓	1		ns
t_h	Hold time, data after LE1B, LE2B, LEA1B, or LEA2B↓	1		ns

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DC ELECTRICAL CHARACTERISTICS (2.5V ± 0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 2.3V; I _{IK} = -18mA		-0.85	-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 2.3 to 3.6V; I _{OH} = -100µA	V _{CC} -0.2	V _{CC}		V
		V _{CC} = 2.3V; I _{OH} = -8mA	1.8	2.1		
V _{OL}	Low-level output voltage	V _{CC} = 2.3V; I _{OL} = 100µA		0.07	0.2	
		V _{CC} = 2.3V; I _{OL} = 24mA		0.3	0.5	
V _{RST}	Power-up output low voltage ⁷	V _{CC} = 2.7V; I _O = 1mA; V _I = V _{CC} or GND			0.55	V
I _I	Input leakage current	V _{CC} = 2.7V; V _I = V _{CC} or GND	Control pins	0.1	±1	µA
		V _{CC} = 0 or 2.7V; V _I = 5.5V		0.1	10	
		V _{CC} = 2.7V; V _I = V _{CC}	Data pins ⁴	0.1	1	
		V _{CC} = 2.7V; V _I = 0		0.1	-5	
I _{OFF}	Off current	V _{CC} = 0V; V _I or V _O = 0 to 4.5V		0.1	±100	µA
I _{HOLD}	Bus Hold current Data inputs ⁶	V _{CC} = 2.3V; V _I = 0.7V		90		µA
		V _{CC} = 2.3V; V _I = 1.7V		-10		
I _{EX}	Current into an output in the High state when V _O > V _{CC}	V _O = 5.5V; V _{CC} = 2.3V		10	125	µA
I _{PU/PD}	Power up/down 3-State output current ³	V _{CC} ≤ 1.2V; V _O = 0.5V to V _{CC} ; V _I = GND or V _{CC} ; OE/OE = Don't care		1	100	µA
I _{OZH}	3-State output High current	V _{CC} = 2.7V; V _O = 2.3V; V _I = V _{IL} or V _{IH}		0.5	5	µA
I _{OZL}	3-State output Low current	V _{CC} = 2.7V; V _O = 0.5V; V _I = V _{IL} or V _{IH}		0.5	-5	µA
I _{CCH}	Quiescent supply current	V _{CC} = 2.7V; Outputs High, V _I = GND or V _{CC} , I _O = 0		0.04	0.1	mA
I _{CCL}		V _{CC} = 2.7V; Outputs Low, V _I = GND or V _{CC} , I _O = 0		2.7	4.5	
I _{CCZ}		V _{CC} = 2.7V; Outputs Disabled; V _I = GND or V _{CC} , I _O = 0 ⁵		0.04	0.1	
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 2.3V to 2.7V; One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND		0.04	0.4	mA

NOTES:

- All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
- This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
- This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
- Unused pins at V_{CC} or GND.
- I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
- Not guaranteed.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

2.5V/3.3V 12-bit to 24-bit multiplexed D-type latches (3-State)

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AC ELECTRICAL CHARACTERISTICS (2.5V ± 0.2V RANGE)

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$

SYMBOL	PARAMETER		$T_{\text{amb}} = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{\text{CC}} = +2.5\text{V} \pm 0.2\text{V}$			UNIT
	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	
t_{PLH}	A or B	B or A	1	3.5	5.3	ns
t_{PHL}			1	3.3	5.4	ns
t_{PLH}	$\overline{\text{LE}}$	A or B	1.1	3.9	6.0	ns
t_{PHL}			1.1	4.2	6.2	ns
t_{PLH}	SEL (B1)	A	1.3	2.9	4.5	ns
	SEL (B2)	A	1.1	3.3	4.8	ns
t_{PHL}	SEL (B1)	A	1.5	3.0	4.5	ns
	SEL (B2)	A	1.6	3.2	4.6	ns
t_{PZH}	$\overline{\text{OE}}$	A or B	1	3.1	5.0	ns
t_{PZL}			1.6	2.0	3.0	ns
t_{PHZ}	$\overline{\text{OE}}$	A or B	2.2	4.0	6.6	ns
t_{PLZ}			1.3	2.0	3.4	ns

AC SETUP CHARACTERISTICS (2.5V ± 0.2V RANGE)

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$

SYMBOL	PARAMETER	$T_{\text{amb}} = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{\text{CC}} = +2.5\text{V} \pm 0.2\text{V}$		UNIT
		MIN	MAX	
t_w	Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high	3.3		ns
t_{su}	Setup time, data before LE1B, LE2B, LEA1B, or LEA2B↓	1		ns
t_h	Hold time, data after LE1B, LE2B, LEA1B, or LEA2B↓	1		ns

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AC WAVEFORMS

$V_M = 1.5V$ for all waveforms

The outputs are measured one at a time with one transition per measurement.

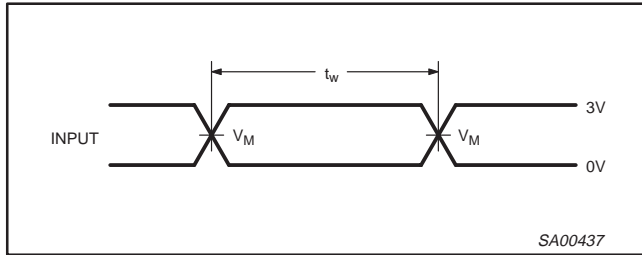


Figure 1. Pulse duration

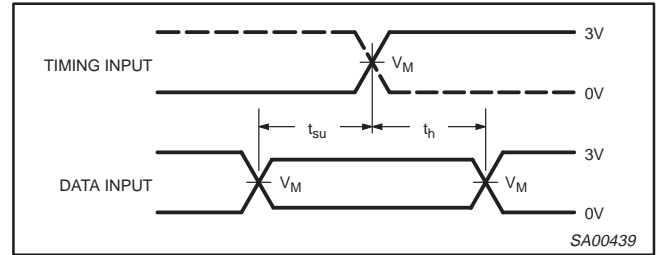
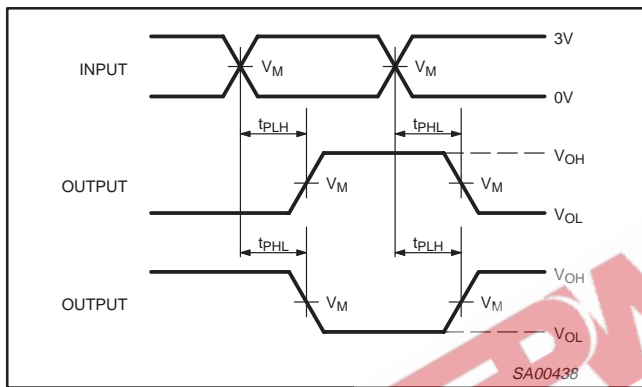
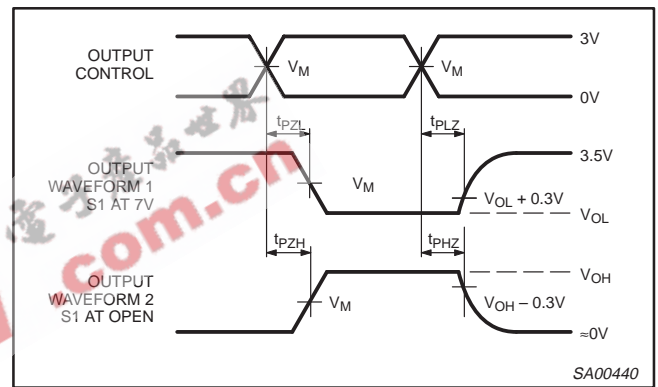


Figure 3. Setup and hold times



All input pulses are supplied by generators having the following characteristics: $PRR \leq 10MHz$, $Z_O = 50\Omega$, $t_r \leq 2.5ns$, $t_f \leq 2.5ns$.

Figure 2. Propagation delay times; inverting and non-inverting outputs



Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 4. Enable and disable times; low- and high-level enabling

TEST LOAD CIRCUIT

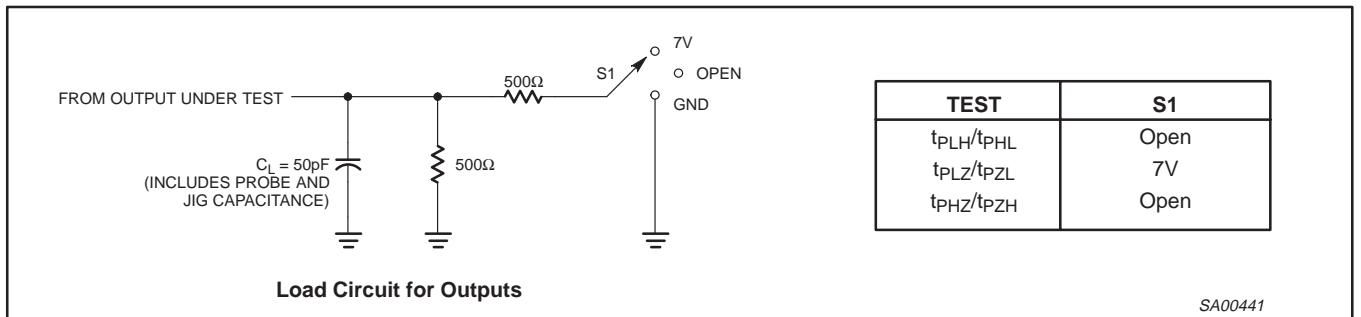


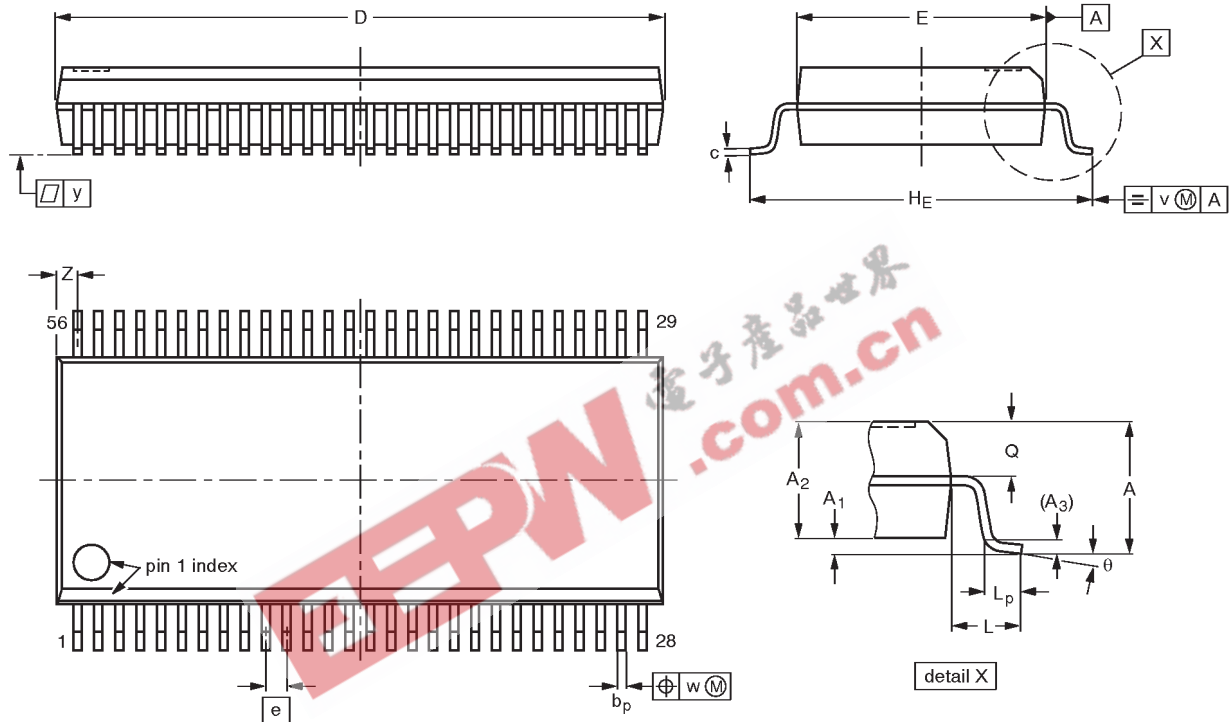
Figure 5. Test load circuit

12-bit to 24-bit multiplexed D-type latches (3-State)

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SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

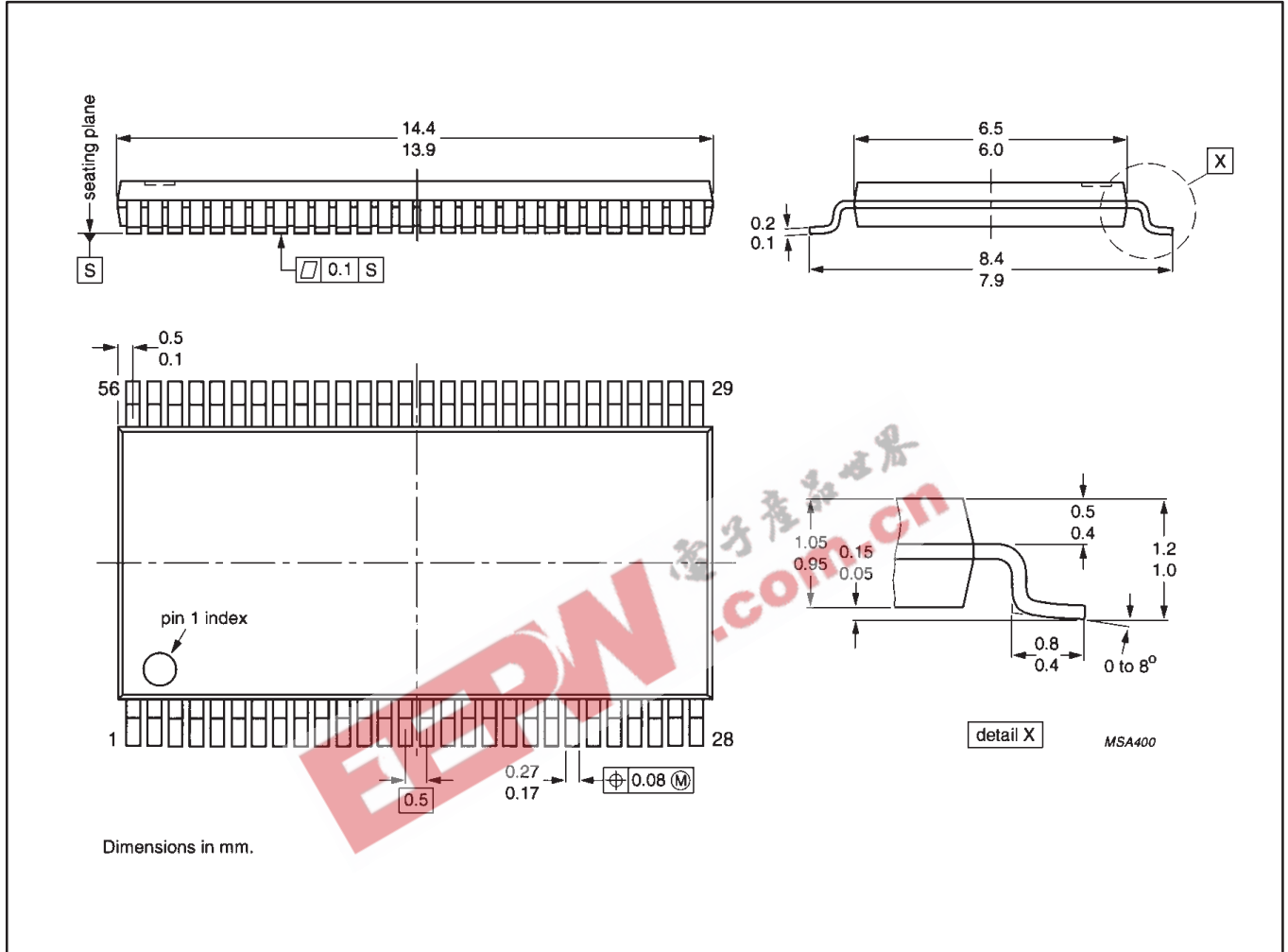
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118AB				93-11-02 95-02-04

12-bit to 24-bit multiplexed D-type latches (3-State)

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TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



12-bit to 24-bit multiplexed D-type latches (3-State)

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NOTES

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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