FAIRCHILD SEMICONDUCTOR™

March 1990
Revised September 2000

# 74ACTQ821
# Quiet Series™ 10-Bit D-Type Flip-Flop with 3-STATE Outputs

## General Description

The ACTQ821 is a 10-bit D-type flip-flop with non-inverting 3-STATE outputs arranged in a broadside pinout. The ACTQ821 utilizes Fairchild's Quiet Series™ technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

## Features

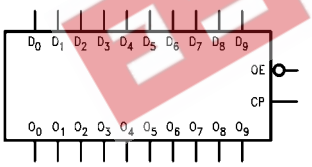
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Non-inverting 3-STATE outputs for bus interfacing
- 4 kV minimum ESD immunity
- Outputs source/sink 24 mA

## Ordering Code:

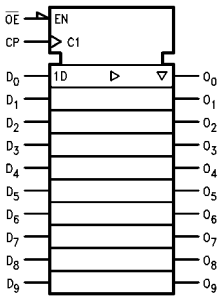
| Order Number | Package Number | Package Description |
|---|---|---|
| 74ACTQ821SC | M24B | 24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide |
| 74ACTQ821SPC | N24C | 24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

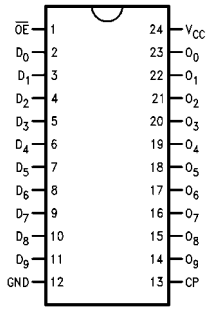
## Logic Symbols




IEEE/IEC




## Connection Diagram




## Pin Descriptions

| Pin Names | Description |
|---|---|
| $D_0$–$D_9$ | Data Inputs |
| $O_0$–$O_9$ | Data Outputs |
| $\overline{OE}$ | Output Enable Input |
| CP | Clock Input |

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## Functional Description

The ACTQ821 consists of ten-bit D-type edge-triggered flip-flops. The buffered Clock (CP) and buffered Output Enable ($\overline{OE}$) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With $\overline{OE}$ LOW the contents of the flip-flops are available at the outputs. When $\overline{OE}$ is HIGH the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

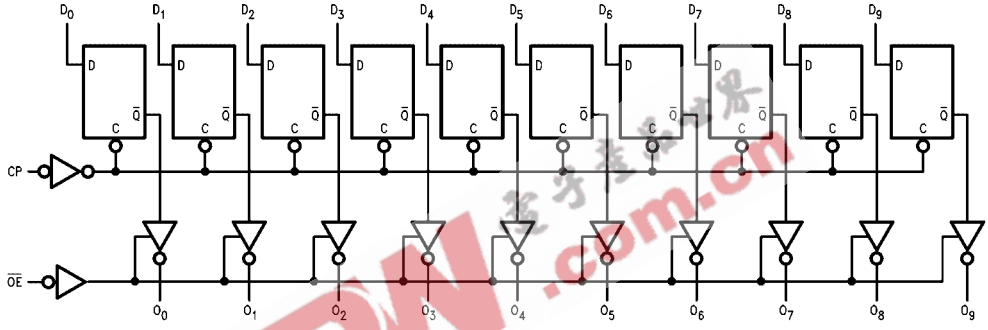
The ACTQ821 is functionally and pin compatible with the AM29821.

## Function Table

| Inputs | | | Internal | Outputs | Function |
|---|---|---|---|---|---|
| $\overline{OE}$ | CP | D | Q | O | |
| H | ⌐ | L | L | Z | High Z |
| H | ⌐ | H | H | Z | High Z |
| L | ⌐ | L | L | L | Load |
| L | ⌐ | H | H | H | Load |

H = HIGH Voltage Level
L = LOW Voltage Level
Z = HIGH Impedance
⌐ = LOW-to-HIGH Clock Transition

## Logic Diagram




Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings(Note 1)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | − 0.5V to + 7.0V |
| DC Input Diode Current ($I_{IK}$) | |
| $V_I$ = − 0.5V | − 20 mA |
| $V_I$ = $V_{CC}$ + 0.5V | + 20 mA |
| DC Input Voltage ($V_I$) | − 0.5V to $V_{CC}$ + 0.5V |
| DC Output Diode Current ($I_{OK}$) | |
| $V_O$ = − 0.5V | − 20 mA |
| $V_O$ = $V_{CC}$ + 0.5V | + 20 mA |
| DC Output Voltage ($V_O$) | − 0.5V to $V_{CC}$ + 0.5V |
| DC Output Source or Sink Current ($I_O$) | ± 50 mA |
| DC $V_{CC}$ or Ground Current per Output Pin ($I_{CC}$ or $I_{GND}$) | ± 50 mA |
| Storage Temperature ($T_{STG}$) | − 65°C to + 150°C |
| DC Latch-Up Source or Sink Current | ± 300 mA |
| Junction Temperature ($T_J$) | |
| PDIP | 140°C |

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | 4.5V to 5.5V |
| Input Voltage ($V_I$) | 0V to $V_{CC}$ |
| Output Voltage ($V_O$) | 0V to $V_{CC}$ |
| Operating Temperature ($T_A$) | − 40°C to + 85°C |
| Minimum Input Edge Rate ΔV/Δt | |
| Minimum Input Edge Rate ΔV/Δt | 125 mV/ns |
| $V_{IN}$ from 0.8V to 2.0V | |
| $V_{CC}$ @ 4.5V, 5.5V | |

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

## DC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ | $T_A$ = + 25°C | $T_A$ = − 40°C to + 85°C | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | (V) | Typ | Guaranteed Limits | | | |
| $V_{IH}$ | Minimum HIGH Level Input Voltage | 4.5 | 1.5 | 2.0 | 2.0 | V | $V_{OUT}$ = 0.1V or $V_{CC}$ − 0.1V |
| | | 5.5 | 1.5 | 2.0 | 2.0 | | |
| $V_{IL}$ | Maximum LOW Level Input Voltage | 4.5 | 1.5 | 0.8 | 0.8 | V | $V_{OUT}$ = 0.1V or $V_{CC}$ − 0.1V |
| | | 5.5 | 1.5 | 0.8 | 0.8 | | |
| $V_{OH}$ | Minimum HIGH Level Output Voltage | 4.5 | 4.49 | 4.4 | 4.4 | V | $I_{OUT}$ = − 50 μA |
| | | 5.5 | 5.49 | 5.4 | 5.4 | | |
| | | 4.5 | | 3.86 | 3.76 | V | $V_{IN}$ = $V_{IL}$ or $V_{IH}$<br>$I_{OH}$ = − 24 mA |
| | | 5.5 | | 4.86 | 4.76 | | $I_{OH}$ = − 24 mA (Note 2) |
| $V_{OL}$ | Maximum LOW Level Output Voltage | 4.5 | 0.001 | 0.1 | 0.1 | V | $I_{OUT}$ = 50 μA |
| | | 5.5 | 0.001 | 0.1 | 0.1 | | |
| | | 4.5 | | 0.36 | 0.44 | V | $V_{IN}$ = $V_{IL}$ or $V_{IH}$<br>$I_{OL}$ = 24 mA |
| | | 5.5 | | 0.36 | 0.44 | | $I_{OL}$ = 24 mA (Note 2) |
| $I_{IN}$ | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | μA | $V_I$ = $V_{CC}$, GND |
| $I_{OZ}$ | Maximum 3-STATE Leakage Current | 5.5 | | ±0.5 | ±5.0 | μA | $V_I$ = $V_{IL}$, $V_{IH}$<br>$V_O$ = $V_{CC}$, GND |
| $I_{CCT}$ | Maximum $I_{CC}$/Input | 5.5 | 0.6 | | 1.5 | mA | $V_I$ = $V_{CC}$ − 2.1V |
| $I_{OLD}$ | Minimum Dynamic | 5.5 | | | 75 | mA | $V_{OLD}$ = 1.65V Max |
| $I_{OHD}$ | Output Current (Note 3) | 5.5 | | | −75 | mA | $V_{OHD}$ = 3.85V Min |
| $I_{CC}$ | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 80.0 | μA | $V_{IN}$ = $V_{CC}$ or GND |
| $V_{OLP}$ | Quiet Output Maximum Dynamic $V_{OL}$ | 5.0 | 1.1 | 1.5 | | V | Figure 1, Figure 2 (Note 4)(Note 5) |
| $V_{OLV}$ | Quiet Output Minimum Dynamic $V_{OL}$ | 5.0 | − 0.6 | − 1.2 | | V | Figure 1, Figure 2 (Note 4)(Note 5) |
| $V_{IHD}$ | Minimum HIGH Level Dynamic Input Voltage | 5.0 | 1.9 | 2.2 | | V | (Note 4)(Note 6) |
| $V_{ILD}$ | Maximum LOW Level Dynamic Input Voltage | 5.0 | 1.2 | 0.8 | | V | (Note 4)(Note 6) |

## DC Electrical Characteristics (Continued)

**Note 2:** All outputs loaded; thresholds on input associated with output under test.

**Note 3:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 4:** DIP package.

**Note 5:** Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.

**Note 6:** Maximum number of data inputs (n) switching. (n–1) inputs switching 0V to 3V. Input-under-test switching: 3V to threshold ($V_{ILD}$), 0V to threshold ($V_{IHD}$), f = 1 MHz.

## AC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ (V) (Note 7) | $T_A = +25°C$, $C_L = 50$ pF | | | $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | 5.0 | 120 | | | 110 | | MHz |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay CP to $O_n$ | 5.0 | 3.0 | 6.5 | 9.5 | 2.5 | 10.5 | ns |
| $t_{PZH}$ $t_{PZL}$ | Output Enable Time $\overline{OE}$ to $O_n$ | 5.0 | 3.0 | 7.5 | 10.5 | 2.5 | 11.5 | ns |
| $t_{PHZ}$ $t_{PLZ}$ | Output Disable Time $\overline{OE}$ to $O_n$ | 5.0 | 1.0 | 6.5 | 8.5 | 1.0 | 9.0 | ns |
| $t_{OSLH}$ $t_{OSHL}$ | Output to Output Skew CP to $O_n$ (Note 8) | 5.0 | | 0.5 | 1.0 | | 1.0 | ns |

**Note 7:** Voltage Range 5.0 is 5.0V ± 0.5V

**Note 8:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same packaged device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ($t_{OSHL}$) or LOW-to-HIGH ($t_{OSLH}$). Parameter guaranteed by design. Not tested.

## AC Operating Requirements

| Symbol | Parameter | $V_{CC}$ (V) (Note 9) | $T_A = +25°C$, $C_L = 50$ pF | | $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | Units |
|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Minimum | | |
| $t_S$ | Setup Time, HIGH or LOW $D_n$ to CP | 5.0 | | 3.0 | 3.0 | ns |
| $t_H$ | Hold Time, HIGH or LOW $D_n$ to CP | 5.0 | | 1.5 | 1.5 | ns |
| $t_H$ | CP Pulse Width HIGH or LOW | 5.0 | | 4.5 | 5.5 | ns |

**Note 9:** Voltage Range 5.0 is 5.0V ± 0.5V

## Capacitance

| Symbol | Parameter | Typ | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4.5 | pF | $V_{CC}$ = OPEN |
| $C_{PD}$ | Power Dissipation Capacitance | 55.0 | pF | $V_{CC}$ = 5.0V |

## FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

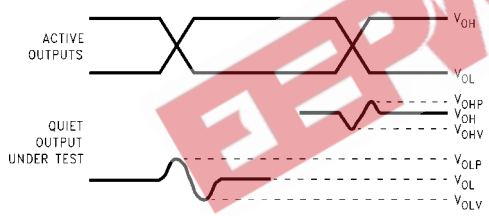
Hewlett Packard Model 8180A Word Generator

PC-163A Test Fixture

Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the HFS generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. It is important to deskew the HFS generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set the HFS generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and effect the results of the measurement.
5. Set the HFS generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with an oscilloscope.




**Note 10:** $V_{OHV}$ and $V_{OLP}$ are measured with respect to ground reference.

**Note 11:** Input pulses have the following characteristics: f = 1 MHz, $t_r$ = 3 ns, $t_f$ = 3 ns, skew < 150 ps.

**FIGURE 1. Quiet Output Noise Voltage Waveforms**

$V_{OLP}/V_{OLV}$ and $V_{OHP}/V_{OHV}$:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure $V_{OLP}$ and $V_{OLV}$ on the quiet output during the worst case transition for active and enable. Measure $V_{OHP}$ and $V_{OHV}$ on the quiet output during the worst case active and enable transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

$V_{ILD}$ and $V_{IHD}$:

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, $V_{IL}$, until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds $V_{IL}$ limits, or on output HIGH levels that exceed $V_{IH}$ limits. The input LOW voltage level at which oscillation occurs is defined as $V_{ILD}$.
- Next decrease the input HIGH voltage level $V_{IH}$ until the output begins to oscillate or steps out a min of 2ns. Oscillation is defined as noise on the output LOW level that exceeds $V_{IL}$ limits, or on output HIGH levels that exceed $V_{IH}$ limits. The input HIGH voltage level at which oscillation occurs is defined as $V_{IHD}$.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

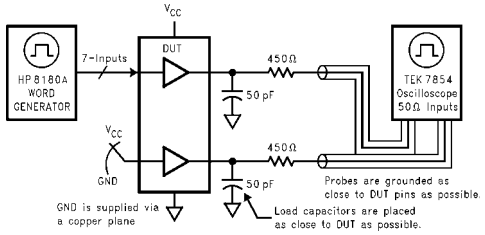
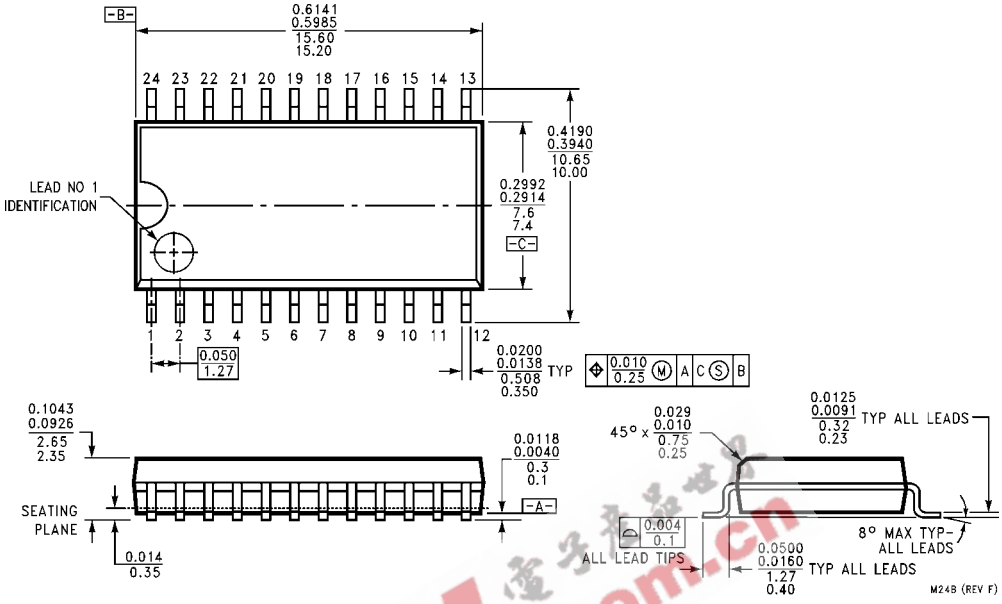


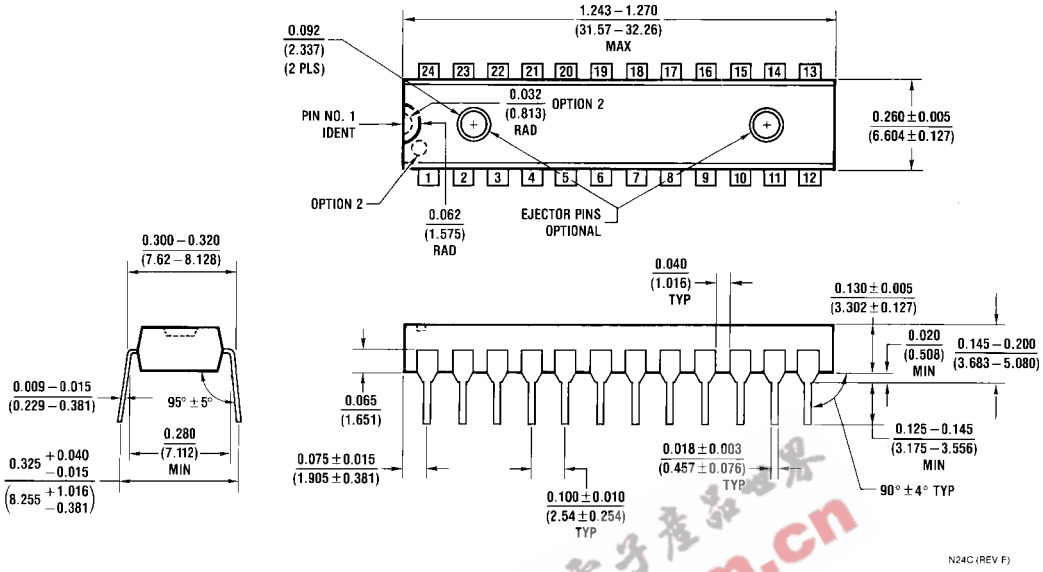

**FIGURE 2. Simultaneous Switching Test Circuit**

## Physical Dimensions inches (millimeters) unless otherwise noted




**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide**
**Package Number M24B**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide**
**Package Number N24C**



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