

# DATA SHEET

## 74LVC821A

10-bit D-type flip-flop with 5-volt tolerant inputs/outputs; positive-edge trigger (3-State)

Product specification

1998 Sep 25

# 10-bit D-type flip-flop with 5-volt tolerant inputs/outputs; positive-edge trigger (3-State)

## 74LVC821A

### FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Supply voltage range of 2.7V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- 10-bit positive edge-triggered register
- Independent register and 3-State buffer operation
- Flow-through pin-out architecture

### DESCRIPTION

The 74LVC821A is a high performance, low-power, low-voltage Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5.0V devices. In 3-state operation, outputs can handle 5V. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC821A is a 10-bit D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-State outputs for bus-oriented applications. A clock (CP) and an output enable ( $\overline{OE}$ ) input are common to all flip-flops. The ten flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition. When  $\overline{OE}$  is LOW, the contents of the ten flip-flops is available at the outputs.

When  $\overline{OE}$  is HIGH, the outputs go to the high impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

### QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25^{\circ}\text{C}$ ;  $t_r = t_f \leq 2.5$  ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	Propagation delay CP to $Q_n$	$C_L = 50$ pF; $V_{CC} = 3.3$ V	5.4	ns
$f_{max}$	Maximum clock frequency		150	MHz
$C_I$	Input capacitance		5.0	pF
$C_{PD}$	Power dissipation capacitance per flip-flop	Notes 1 and 2	26	pF

#### NOTES:

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ )  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacity in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.
2. The condition is  $V_I = \text{GND to } V_{CC}$

### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDERING CODE	PKG. DWG. #
24-Pin Plastic SO	-40°C to +85°C	74LVC821A D	SOT137-1
24-Pin Plastic SSOP Type II	-40°C to +85°C	74LVC821A DB	SOT340-1
24-Pin Plastic TSSOP Type I	-40°C to +85°C	74LVC821A PW	SOT355-1

# 10-bit D-type flip-flop with 5-volt tolerant inputs/outputs; positive-edge trigger (3-State)

74LVC821A

## PIN DESCRIPTION

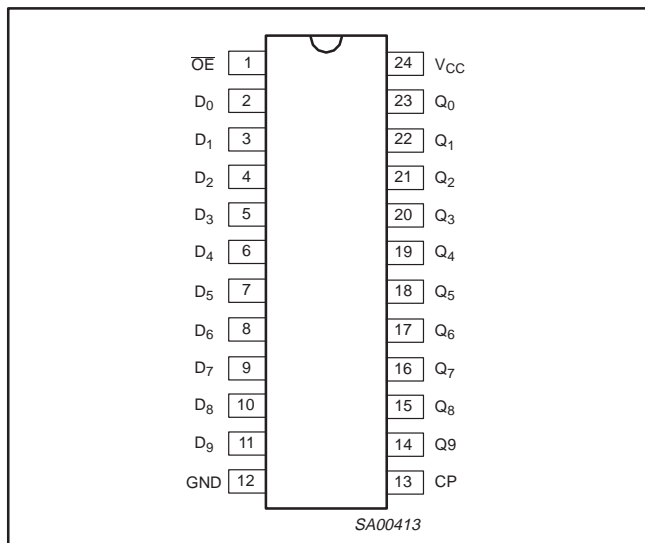
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	Output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	D <sub>0</sub> to D <sub>9</sub>	Data inputs
23, 22, 21, 20, 19, 18, 17, 16, 15, 14	Q <sub>0</sub> to Q <sub>9</sub>	3-State flip-flop outputs
12	GND	Ground (0 V)
13	CP	Clock input (LOW-to-HIGH, edge-triggered)
24	V <sub>CC</sub>	Positive supply voltage

## FUNCTION TABLE

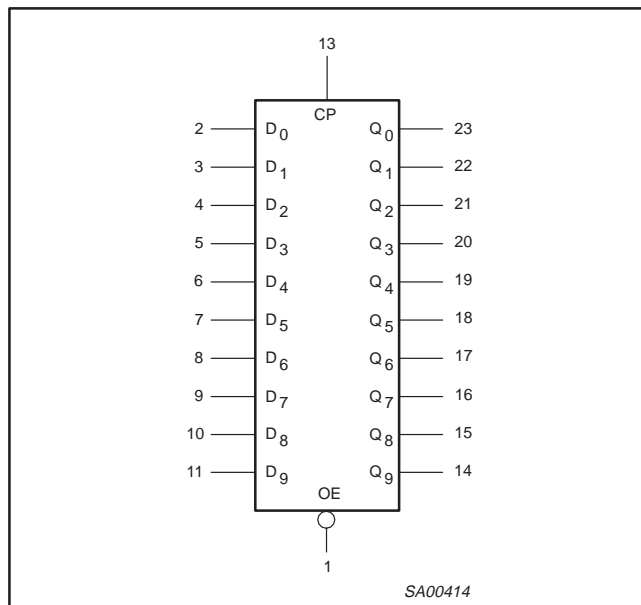
OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS Q <sub>0</sub> to Q <sub>9</sub>
	$\overline{OE}$	CP	D <sub>n</sub>		
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z
Hold	L	H or L	X	NC	NC

H = HIGH voltage level  
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition  
 L = LOW voltage level  
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition  
 Z = high impedance OFF-state  
 ↑ = LOW-to-HIGH clock transition  
 NC= no change

## PIN CONFIGURATION



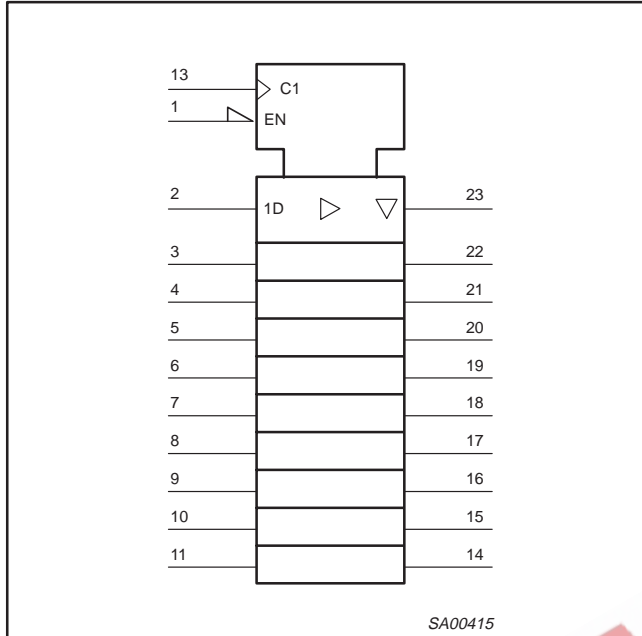
## LOGIC SYMBOL



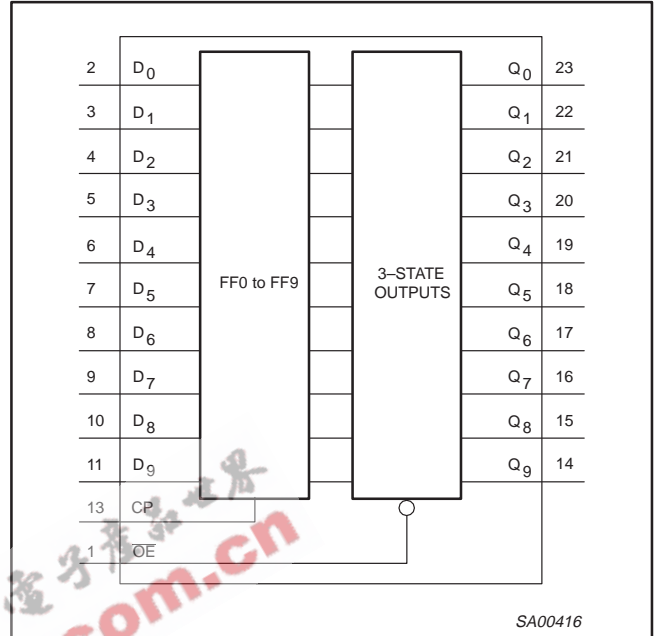
10-bit D-type flip-flop with 5-volt tolerant inputs/outputs; positive-edge trigger (3-State)

74LVC821A

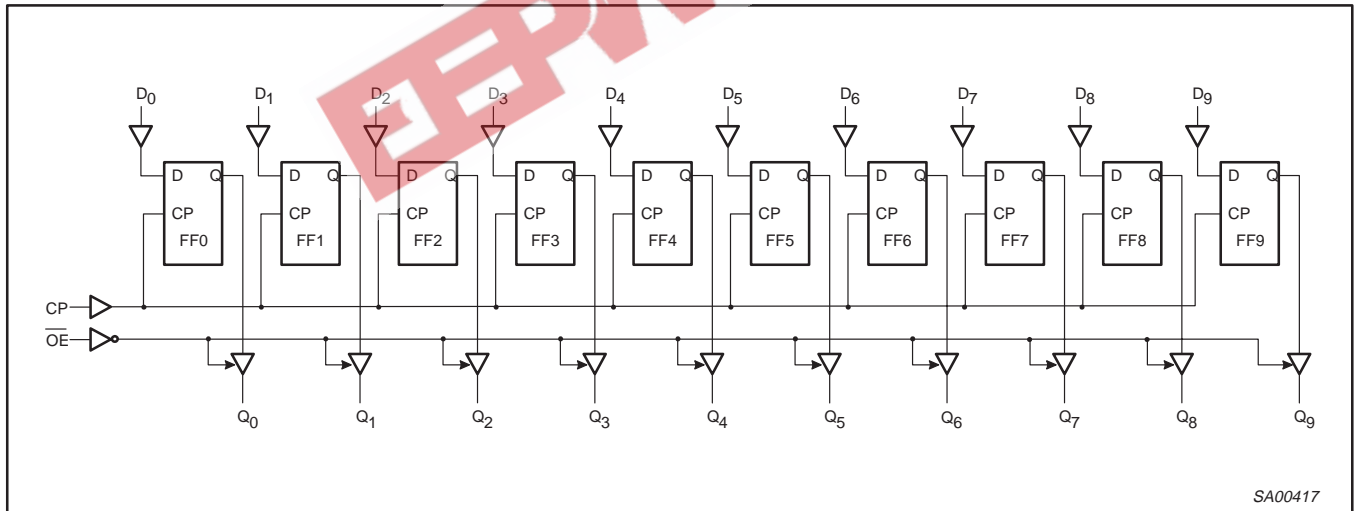
LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



# 10-bit D-type flip-flop with 5-volt tolerant inputs/outputs; positive-edge trigger (3-State)

74LVC821A

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
$V_{CC}$	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
$V_I$	DC Input voltage range		0	5.5	V
$V_O$	DC output voltage range; output HIGH or LOW state		0	$V_{CC}$	V
	DC output voltage range; output 3-State		0	5.5	
$T_{amb}$	Operating ambient temperature range in free-air		-40	+85	°C
$t_r, t_f$	Input rise and fall times	$V_{CC} = 1.2$ to $2.7V$ $V_{CC} = 2.7$ to $3.6V$	0 0	20 10	ns/V

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

In accordance with the Absolute Maximum Rating System (IEC 134)  
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +6.5	V
$I_{IK}$	DC input diode current	$V_I < 0$	-50	mA
$V_I$	DC input voltage	Note 2	-0.5 to +6.5	V
$I_{OK}$	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	± 50	mA
$V_O$	DC output voltage; output HIGH or LOW state	Note 2	-0.5 to $V_{CC} + 0.5$	V
	DC output voltage; output 3-State	Note 2	-0.5 to 6.5	
$I_O$	DC output source or sink current	$V_O = 0$ to $V_{CC}$	± 50	mA
$I_{GND}, I_{CC}$	DC $V_{CC}$ or GND current		± 100	mA
$T_{stg}$	Storage temperature range		-65 to +150	°C
$P_{TOT}$	Power dissipation per package			
	- plastic mini-pack (SO) - plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	500 500	mW

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

# 10-bit D-type flip-flop with 5-volt tolerant inputs/outputs; positive-edge trigger (3-State)

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## DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
V <sub>IH</sub>	HIGH level Input voltage	V <sub>CC</sub> = 1.2V	V <sub>CC</sub>			V
		V <sub>CC</sub> = 2.7 to 3.6V	2.0			
V <sub>IL</sub>	LOW level Input voltage	V <sub>CC</sub> = 1.2V			GND	V
		V <sub>CC</sub> = 2.7 to 3.6V			0.8	
V <sub>OH</sub>	HIGH level output voltage	V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA	V <sub>CC</sub> - 0.5			V
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -100μA	V <sub>CC</sub> - 0.2	V <sub>CC</sub>		
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -18mA	V <sub>CC</sub> - 0.6			
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -24mA	V <sub>CC</sub> - 0.8			
V <sub>OL</sub>	LOW level output voltage	V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA			0.40	V
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100μA			0.20	
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 24mA			0.55	
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = 5.5V or GND		±0.1	±5	μA
I <sub>OZ</sub>	3-State output OFF-state current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5V or GND		0.1	±5	μA
I <sub>off</sub>	Power off leakage supply	V <sub>CC</sub> = 0.0V; V <sub>I</sub> or V <sub>O</sub> = 5.5V		0.1	±10	μA
I <sub>CC</sub>	Quiescent supply current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0		0.1	10	μA
ΔI <sub>CC</sub>	Additional quiescent supply current per input pin	V <sub>CC</sub> = 2.7V to 3.6V; V <sub>I</sub> = V <sub>CC</sub> - 0.6V; I <sub>O</sub> = 0		5	500	μA

### NOTES:

- All typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.
- The specified overdrive current at the data input forces the data input to the opposite logic input state.

## AC CHARACTERISTICS

GND = 0V; t<sub>r</sub> = t<sub>f</sub> ≤ 2.5ns; C<sub>L</sub> = 50pF; R<sub>L</sub> = 500Ω; T<sub>amb</sub> = -40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			V <sub>CC</sub> = 3.3V ±0.3V			V <sub>CC</sub> = 2.7V		
			MIN	TYP <sup>1</sup>	MAX	MIN	MAX	
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation delay CP to Q <sub>n</sub>	Figures 1, 4	1.5	5.4	7.3	1.5	8.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	3-State output enable time OE to Q <sub>n</sub>	Figures 2, 4	1.5	5.5	7.6	1.5	8.8	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	3-State output disable time OE to Q <sub>n</sub>	Figures 2, 4	1.5	3.8	6.2	1.5	6.8	ns
t <sub>w</sub>	Clock pulse width HIGH or LOW	Figure 1	3.3	1.7	–	3.3	–	ns
t <sub>SU</sub>	Setup time D <sub>n</sub> to CP	Figure 3	1.9	0.6	–	0.9	–	ns
t <sub>H</sub>	Hold time D <sub>n</sub> to CP	Figure 3	1.5	0	–	1.5	–	ns
f <sub>max</sub>	Maximum clock pulse frequency	Figure 1	150	200	–	150	–	MHz

### NOTE:

- Unless otherwise stated, all typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.

# 10-bit D-type flip-flop with 5-volt tolerant inputs/outputs; positive-edge trigger (3-State)

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## AC WAVEFORMS

$V_M = 1.5V$  at  $V_{CC} \geq 2.7V$ ;  $V_M = 0.5 V_{CC}$  at  $V_{CC} < 2.7V$ .  
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.  
 $V_X = V_{OL} + 0.3V$  at  $V_{CC} \geq 2.7V$ ;  $V_X = V_{OL} + 0.1 V_{CC}$  at  $V_{CC} < 2.7V$   
 $V_Y = V_{OH} - 0.3V$  at  $V_{CC} \geq 2.7V$ ;  $V_Y = V_{OH} - 0.1 V_{CC}$  at  $V_{CC} < 2.7V$

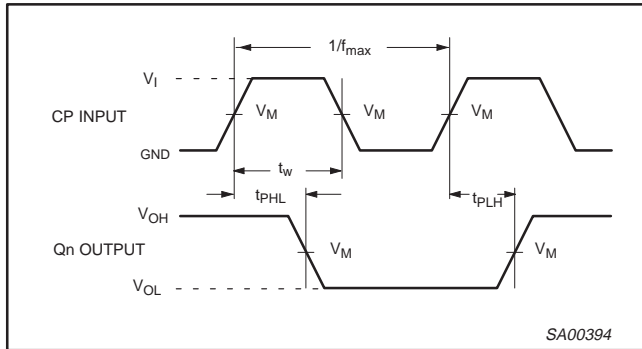


Figure 1. Clock (CP) to output ( $Q_n$ ) propagation delays, the clock pulse width and the maximum clock pulse frequency.

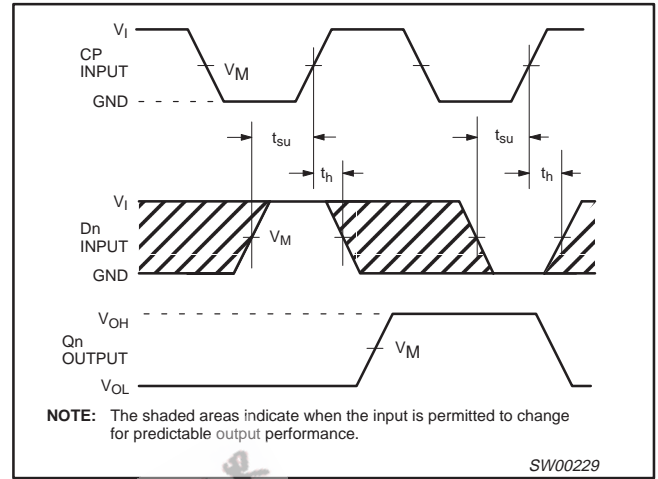


Figure 3. Data setup and hold times for the  $D_n$  input to the CP input.

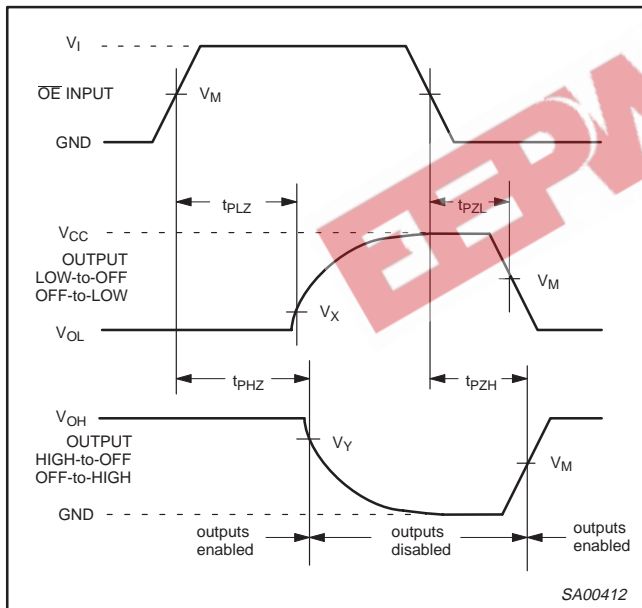


Figure 2. 3-State enable and disable times.

## TEST CIRCUIT

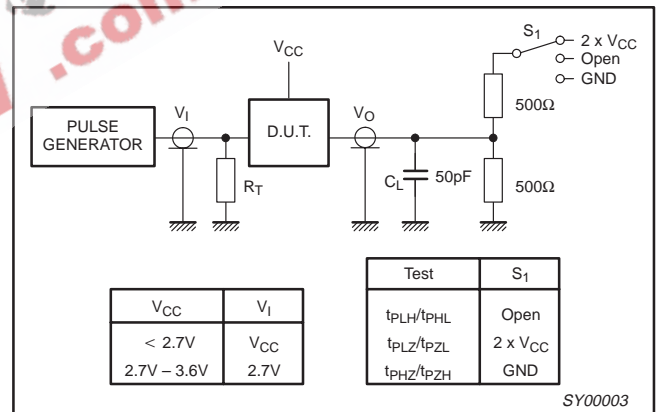


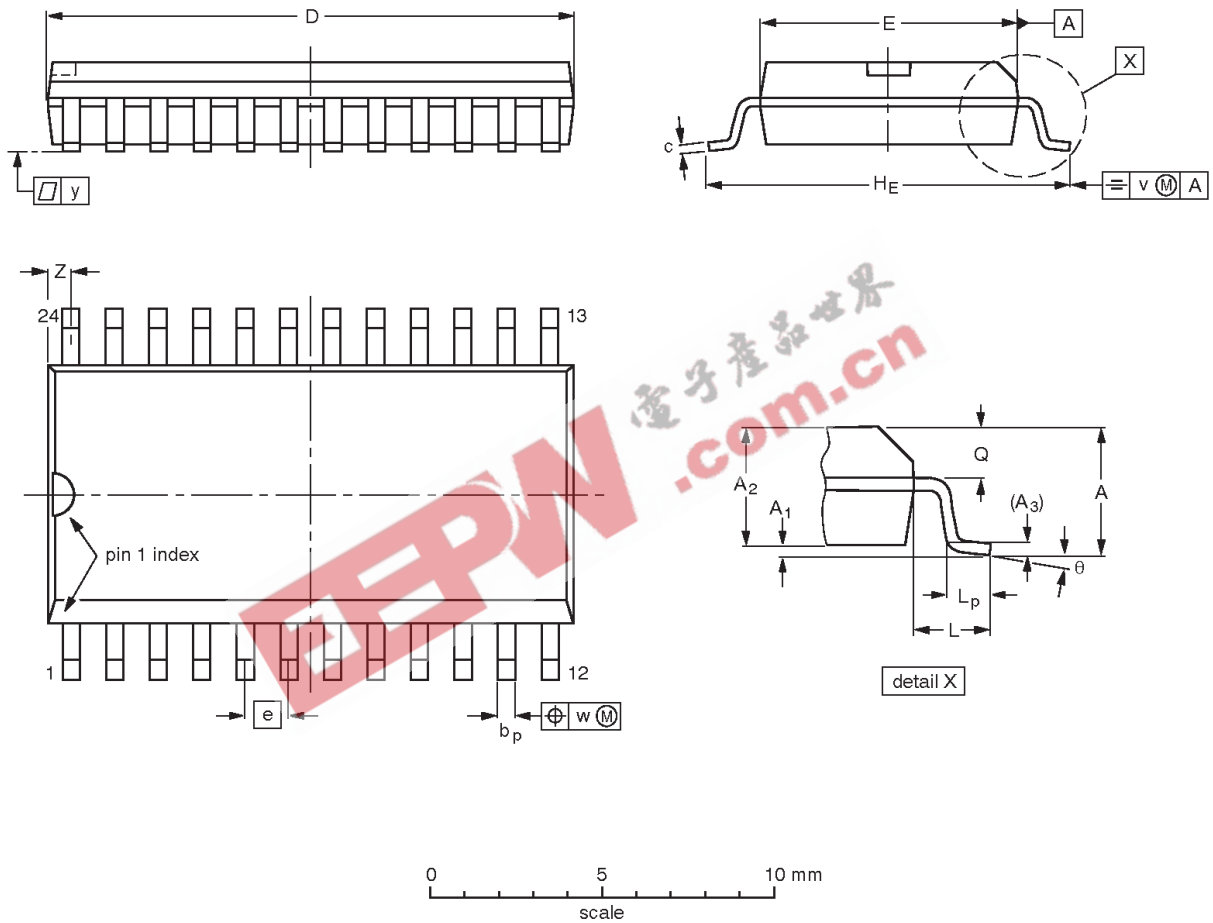
Figure 4. Load circuitry for switching times.

10-bit D-type flip-flop with 5-volt tolerant inputs/outputs; positive-edge trigger (3-State)

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SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				95-01-24 97-05-22

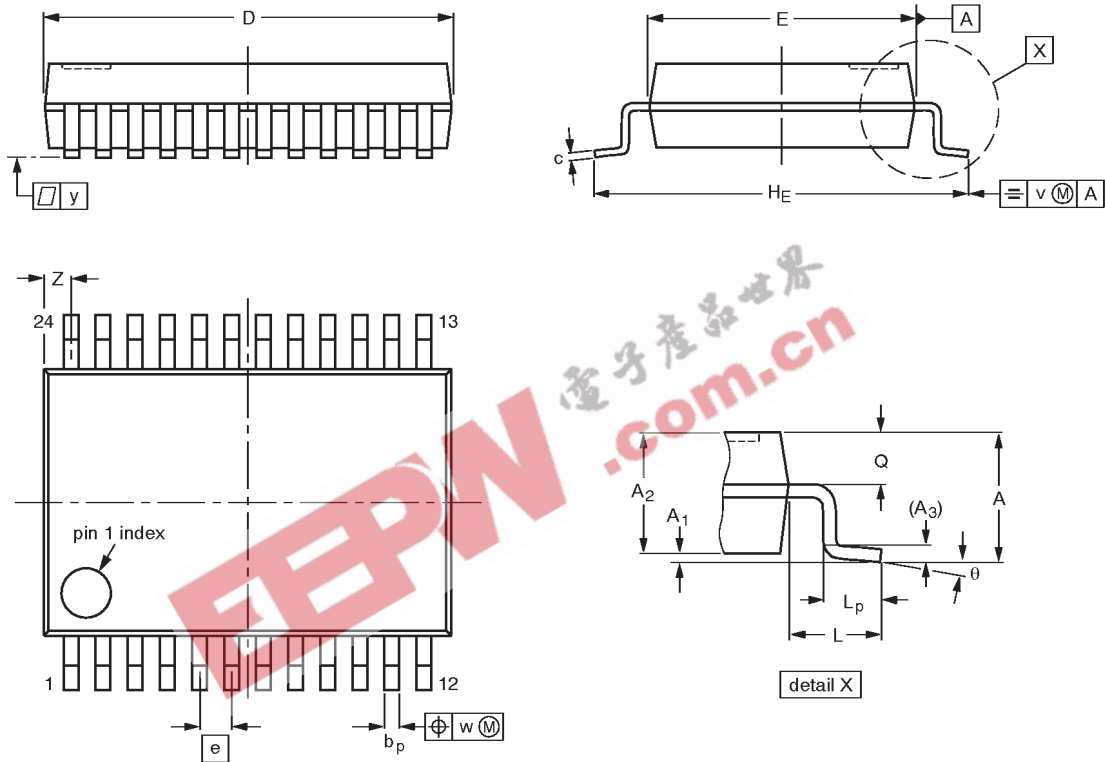


10-bit D-type flip-flop with 5-volt tolerant inputs/outputs; positive-edge trigger (3-State)

74LVC821A

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

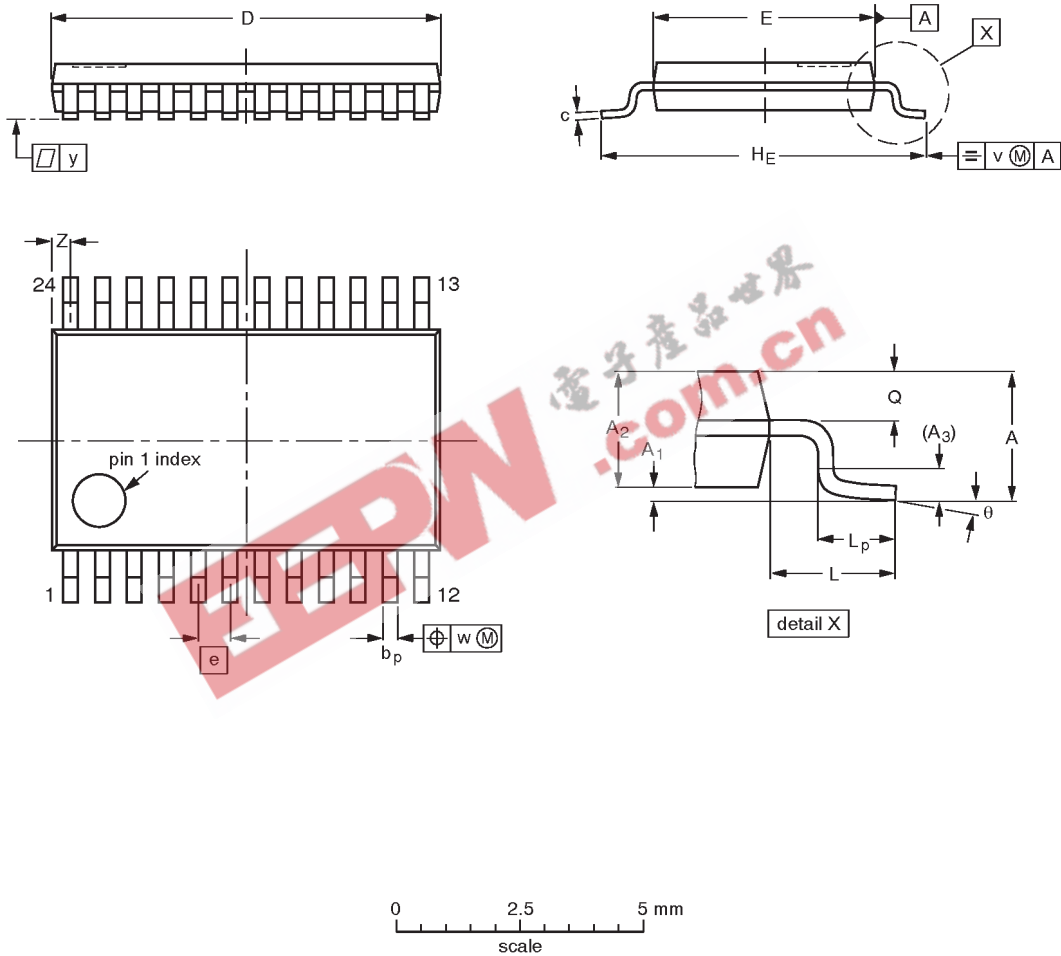
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				93-09-08 95-02-04

10-bit D-type flip-flop with 5-volt tolerant inputs/outputs; positive-edge trigger (3-State)

74LVC821A

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1



**DIMENSIONS** (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				93-06-16 95-02-04

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10-bit D-type flip-flop with 5-volt tolerant  
inputs/outputs; positive-edge trigger (3-State)

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NOTES



# 10-bit D-type flip-flop with 5-volt tolerant inputs/outputs; positive-edge trigger (3-State)

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

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print code

Date of release: 08-98

Document order number:

9397-750-04584

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