FAIRCHILD
SEMICONDUCTOR™

January 1990
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74ACQ657 • 74ACTQ657
Quiet Series™ Octal Bidirectional Transceiver with 8-Bit Parity Generator/Checker and 3-STATE Outputs

General Description

The ACQ/ACTQ657 contains eight non-inverting buffers with 3-STATE outputs and an 8-bit parity generator/checker. Intended for bus oriented applications, the device combines the 245 and the 280 functions in one package.

The ACQ/ACTQ utilizes Fairchild Quiet Series™ technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series features GTO™ output control and undershoot corrector in addition to a split ground bus or superior performance.

Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Combines the 245 and the 280 functions in one package
- 300 mil 24-pin slim dual-in-line package
- Outputs source/sink 24 mA
- ACTQ has TTL-compatible inputs

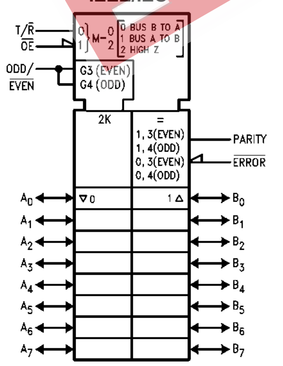
Ordering Code:

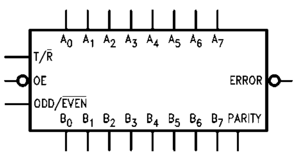
Order Number	Package Number	Package Description
74ACQ657SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
74ACTQ657SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74ACTQ657SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code

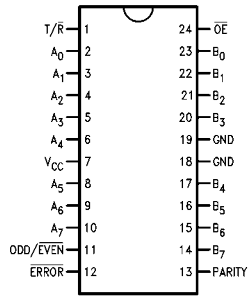
Logic Symbols

IEEE/IEC





Connection Diagram



Pin Descriptions

Pin Names	Description
A_0–A_7	Data Inputs/3-STATE Outputs
B_0–B_7	Data Inputs/3-STATE Outputs
T/$\overline{R}$	Transmit/Receive Input
$\overline{OE}$	Enable Input
PARITY	Parity Input/3-STATE Output
ODD/$\overline{EVEN}$	ODD/$\overline{EVEN}$ Parity Input
$\overline{ERROR}$	Error 3-STATE Output

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Functional Description

The Transmit/Receive (T/$\overline{R}$) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active HIGH) enables data from the A-Port to the B-Port; Receive (active LOW) enables data from the B-Port to the A-Port.

The Output Enable ($\overline{OE}$) input disables the parity and $\overline{ERROR}$ outputs and both the A and B Ports by placing them in a HIGH-Z condition when the Output Enable input is HIGH.

When transmitting (T/$\overline{R}$ HIGH), the parity generator detects whether an even or odd number of bits on the A-Port are HIGH and compares these with the condition of the parity select (ODD/$\overline{EVEN}$). If the Parity Select is HIGH and an even number of A inputs are HIGH, the Parity output is HIGH.

In receiving mode (T/$\overline{R}$ LOW), the parity select and number of HIGH inputs on port B are compared to the condition of the Parity input. If an even number of bits on the B-Port are HIGH, the parity select is HIGH, and the PARITY input is HIGH, then $\overline{ERROR}$ will be HIGH to indicate no error. If an odd number of bits on the B-Port are HIGH, the parity select is HIGH, and the PARITY input is HIGH, the $\overline{ERROR}$ will be LOW indicating an error.

Function Table

Number of Inputs That	Inputs			Input/ Output	Outputs	
Are High	$\overline{OE}$	T/$\overline{R}$	ODD/$\overline{EVEN}$	Parity	$\overline{ERROR}$	Outputs Mode
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Immaterial	H	X	X	Z	Z	Z

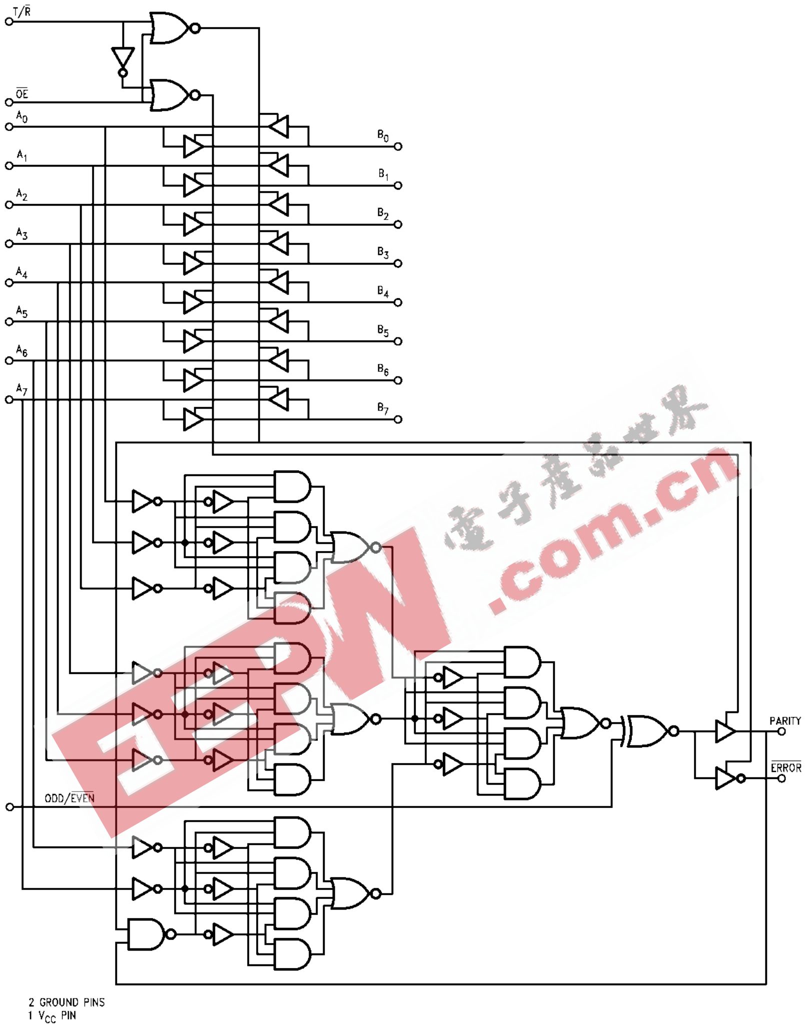
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Function Table

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High-Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Functional Block Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 MA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source	
or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-up Source	
Sink Current	±300 mA
Junction Temperature (T_J)	
PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
ACQ	2.0V to 6.0V
ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ΔV/Δt	
ACQ Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ΔV/Δt	
ACTQ Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for ACQ

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Typ		$T_A = -40°C$ to $+85°C$	Units	Conditions
				Guaranteed Limits			
V_{IH}	Minimum HIGH Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	2.1 3.15 3.85	2.1 3.15 3.85	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{IL}	Maximum LOW Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	0.9 1.35 1.65	0.9 1.35 1.65	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{OH}	Minimum HIGH Level Voltage Output	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	V	$I_{OUT} = -50$ µA
		3.0 4.5 5.5		2.56 3.86 4.85	2.46 3.76 4.76	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -12$ mA $I_{OH} = -24$mA $I_{OH} = -24$ mA (Note 2)
V_{OL}	Maximum LOW Level Output Voltage	3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V	$I_{OUT} = 50$ µA
		3.0 4.5 5.5		0.36 0.36 0.36	0.44 0.44 0.44	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 12$ mA $I_{OL} = 24$ mA $I_{OL} = 24$ mA (Note 2)
I_{IN} (Note 4)	Maximum Input Leakage Current ($T/\overline{R}$, $\overline{OE}$, $ODD/\overline{EVEN}$ Inputs)	5.5		±0.1	±1.0	µA	$V_I = V_{CC}$, GND
I_{OLD}	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}	Output Current (Note 3)	5.5			−75	mA	$V_{OHD} = 3.85V$ Min
I_{CC} (Note 4)	Maximum Quiescent Supply Current	5.5		8.0	80.0	µA	$V_{IN} = V_{CC}$ or GND
I_{OZT}	Maximum I/O Leakage Current (A_n, B_n Inputs)	5.5		±0.6	±6.0	µA	V_I (OE) = V_{IL}, V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5		V	Figures 1, 2 (Note 5)(Note 6)

DC Electrical Characteristics for ACQ (Continued)

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$		$T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2		V	Figures 1, 2 (Note 5)(Note 6)
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	5.0	3.1	3.5		V	(Note 5)(Note 7)
V_{ILD}	Maximum LOW Level Dynamic Input Voltage	5.0	1.9	1.5		V	(Note 5)(Note 7)

Note 2: Maximum of 8 outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

Note 5: DIP package.

Note 6: Max number of outputs defined as (n). Data Inputs are driven 0V to 5V. One output @ GND.

Note 7: Max number of Data Inputs (n) switching. (n–1) Inputs switching 0V to 5V (ACQ).Input-under-test switching: 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}) f = 1 MHz.

DC Electrical Characteristics for ACTQ

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$		$T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum HIGH Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{IL}	Maximum LOW Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{OH}	Minimum HIGH Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	$I_{OUT} = -50$ µA
		4.5 5.5		3.86 4.86	3.76 4.76	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -24mA$ $I_{OH} = -24$ mA (Note 8)
V_{OL}	Maximum LOW Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	$I_{OUT} = 50$ µA
		4.5 5.5		0.36 0.36	0.44 0.44	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 24$ mA $I_{OL} = 24$ mA (Note 8)
I_{IN}	Maximum Input Leakage Current ($T/\overline{R}$, $\overline{OE}$, $ODD/\overline{EVEN}$ Inputs)	5.5		±0.1	±1.0	µA	$V_I = V_{CC}$, GND
I_{OZT}	Maximum I/O Leakage Current (A_n, B_n Inputs)	5.5 5.5		±0.6	±6.0	µA	$V_I = V_{IL}$, V_{IH} $V_O = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}	Output Current (Note 9)	5.5			−75	mA	$V_{OHD} = 3.85V$ Min
I_{CC} (Note 4)	Maximum Quiescent Supply Current	5.5		8.0	80.0	µA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5		V	Figures 1, 2 (Note 10)(Note 11)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2		V	Figures 1, 2 (Note 10)(Note 11)
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	5.0	1.9	2.2		V	(Note 10)(Note 12)
V_{ILD}	Maximum LOW Level Dynamic Input Voltage	5.0	1.2	0.8		V	(Note 10)(Note 12)

Note 8: All outputs loaded; thresholds on input associated with output under test.

Note 9: Maximum test duration 2.0 ms, one output loaded at a time.

Note 10: DIP package.

Note 11: Max number of outputs defined as (n). n–1 Data Inputs are driven 0V to 3V; one output @ GND.

Note 12: Max number of Data Inputs (n) switching. (n–1) Inputs switching 0V to 3V (ACQ). Input-under-test switching; 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}) f =1 MHz.

AC Electrical Characteristics for ACQ

Symbol	Parameter	V_{CC} (V) (Note 13)	$T_A = 25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	3.3	2.5	8.0	11.5	2.5	12.0	ns
t_{PHL}	A_n to B_n, B_n to A_n	5.0	1.5	5.0	7.5	1.5	8.0	
t_{PLH}	Propagation Delay	3.3	3.0	11.5	16.5	3.0	17.0	ns
t_{PHL}	A_n to Parity	5.0	2.0	7.0	10.5	2.0	11.0	
t_{PLH}	Propagation Delay	3.3	3.0	10.0	15.0	3.0	15.5	ns
t_{PHL}	ODD/$\overline{EVEN}$ to PARITY	5.0	2.5	6.5	10.0	2.5	10.5	
t_{PLH}	Propagation Delay	3.3	3.0	10.0	15.0	3.0	15.5	ns
t_{PHL}	ODD/$\overline{EVEN}$ to $\overline{ERROR}$	5.0	2.5	6.5	10.0	2.5	10.5	
t_{PLH}	Propagation Delay	3.3	3.5	11.5	16.0	3.5	16.5	ns
t_{PHL}	B_n to $\overline{ERROR}$	5.0	2.5	7.0	10.5	2.5	11.0	
t_{PLH}	Propagation Delay	3.3	3.0	9.0	13.5	3.0	14.0	ns
t_{PHL}	PARITY to $\overline{ERROR}$	5.0	2.0	6.0	9.0	2.0	9.5	
t_{PZH}	Output Enable Time	3.3	2.5	9.0	13.5	2.5	14.0	ns
t_{PZL}	$\overline{OE}$ to A_n/B_n	5.0	2.0	6.0	9.0	2.0	9.5	
t_{PHZ}	Output Disable Time	3.3	1.0	8.5	13.0	1.0	13.5	ns
t_{PLZ}	$\overline{OE}$ to A_n/B_n	5.0	1.0	5.5	8.5	1.0	9.0	
t_{PZH}	Output Enable Time	3.3	2.5	9.0	13.5	2.5	14.0	ns
t_{PZL}	$\overline{OE}$ to $\overline{ERROR}$ (Note 15)	5.0	2.0	6.0	9.0	2.0	9.5	
t_{PHZ}	Output Disable Time	3.3	1.0	8.5	13.0	1.0	13.5	ns
t_{PLZ}	$\overline{OE}$ to $\overline{ERROR}$	5.0	1.0	5.5	8.5	1.0	9.0	
t_{PZH}	Output Enable Time	3.3	2.5	9.0	13.5	2.5	14.0	ns
t_{PZL}	$\overline{OE}$ to PARITY	5.0	2.0	6.0	9.0	2.0	9.5	
t_{PHZ}	Output Disable Time	3.3	1.0	8.5	13.0	1.0	13.5	ns
t_{PLZ}	$\overline{OE}$ to PARITY	5.0	1.0	5.5	8.5	1.0	9.0	
t_{OSHL}	Output to Output Skew (Note 14)	3.3		1.0	1.5		1.5	ns
t_{OSLH}	A_n, B_n to B_n, A_n	5.0		0.5	1.0		1.0	

Note 13: Voltage Range 3.3 is 3.3V ± 0.3V

Voltage Range 5.0 is 5.0V ± 0.5V

Note 14: Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same packaged device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design. Not tested.

Note 15: These delay times reflect the 3-STATE recovery time only and not the signal time through the buffers or the parity check circuitry. To assure VALID information at the $\overline{ERROR}$ pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to PARITY), and to the $\overline{ERROR}$ output after the $\overline{ERROR}$ pin has been enabled (Output Enable times). VALID data at the $\overline{ERROR}$ pin ≥ (A to PARITY) +(Output Enable Time).

AC Electrical Characteristics for ACTQ

Symbol	Parameter	V_{CC} (V) (Note 16)	$T_A = 25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay A_n to B_n, B_n to A_n	5.0	1.5	5.0	8.0	1.5	8.5	ns
t_{PLH}, t_{PHL}	Propagation Delay A_n to Parity	5.0	2.5	7.5	11.0	2.5	11.5	ns
t_{PLH}, t_{PHL}	Propagation Delay ODD/$\overline{EVEN}$ to PARITY	5.0	2.5	6.5	10.5	2.5	11.0	ns
t_{PLH}, t_{PHL}	Propagation Delay ODD/$\overline{EVEN}$ to $\overline{ERROR}$	5.0	2.5	6.5	10.5	2.5	11.0	ns
t_{PLH}, t_{PHL}	Propagation Delay B_n to $\overline{ERROR}$	5.0	3.0	7.5	11.0	3.0	11.5	ns
t_{PLH}, t_{PHL}	Propagation Delay PARITY to $\overline{ERROR}$	5.0	2.0	6.0	9.5	2.0	10.0	ns
t_{PZH}, t_{PZL}	Output Enable Time $\overline{OE}$ to A_n/B_n	5.0	2.0	6.0	9.5	2.0	10.0	ns
t_{PHZ}, t_{PLZ}	Output Disable Time $\overline{OE}$ to A_n/B_n	5.0	1.0	5.0	9.0	1.0	9.5	ns
t_{PZH}, t_{PZL}	Output Enable Time $\overline{OE}$ to $\overline{ERROR}$ (Note 18)	5.0	2.0	6.0	9.5	2.0	10.0	ns
t_{PHZ}, t_{PLZ}	Output Disable Time $\overline{OE}$ to $\overline{ERROR}$	5.0	1.0	6.0	9.0	1.0	9.5	ns
t_{PZH}, t_{PZL}	Output Enable Time $\overline{OE}$ to PARITY	5.0	2.0	6.0	9.5	2.0	10.0	ns
t_{PHZ}, t_{PLZ}	Output Disable Time $\overline{OE}$ to PARITY	5.0	1.0	5.0	9.0	1.0	9.5	ns
t_{OSHL}, t_{OSLH}	Output to Output Skew A_n, B_n to B_n, A_n (Note 17)	5.0		0.5	1.0		1.0	ns

Note 16: Voltage Range 5.0 is 5.0V ±0.5V

Note 17: Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same packaged device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design. Not tested.

Note 18: These delay times reflect the 3-STATE recovery time only and not the signal time through the buffers or the parity check circuitry. To assure VALID information at the $\overline{ERROR}$ pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to PARITY), and to the $\overline{ERROR}$ output after the $\overline{ERROR}$ pin has been enabled (Output Enable times). VALID data at the $\overline{ERROR}$ pin ≥ (A to PARITY) + (Output Enable Time).

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	160.0	pF	$V_{CC} = 5.0$

FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

Hewlett Packard Model 8180A Word Generator

PC-163A Test Fixture

Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the HFS generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. It is important to deskew the HFS generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set the HFS generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and effect the results of the measurement.
5. Set the HFS generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with an oscilloscope.

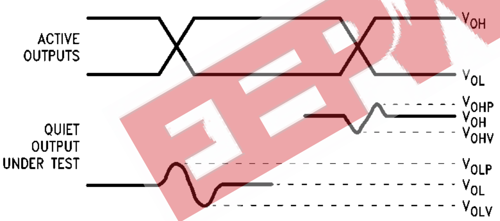


FIGURE 1. Quiet Output Noise Voltage Waveforms

Note 19: V_{OHV} and V_{OLP} are measured with respect to ground reference.

Note 20: Input pulses have the following characteristics: f = 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 150 ps.

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV}:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV} on the quiet output during the worst case transition for active and enable. Measure V_{OHP} and V_{OHV} on the quiet output during the worst case transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD}:

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL}, until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD}.
- Next decrease the input HIGH voltage level, V_{IH}, until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD}.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

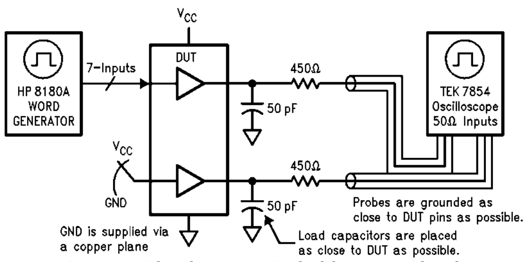
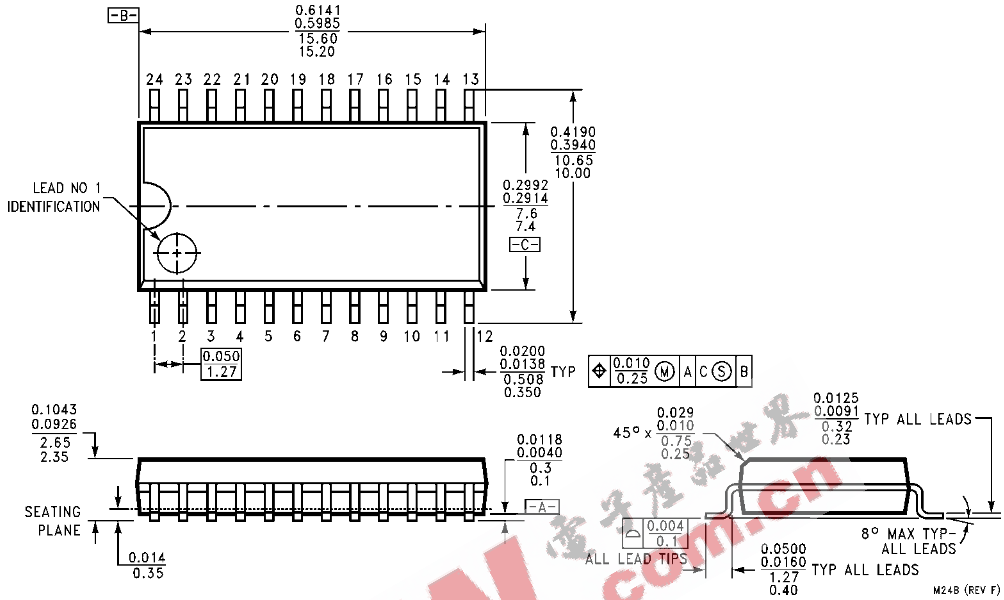


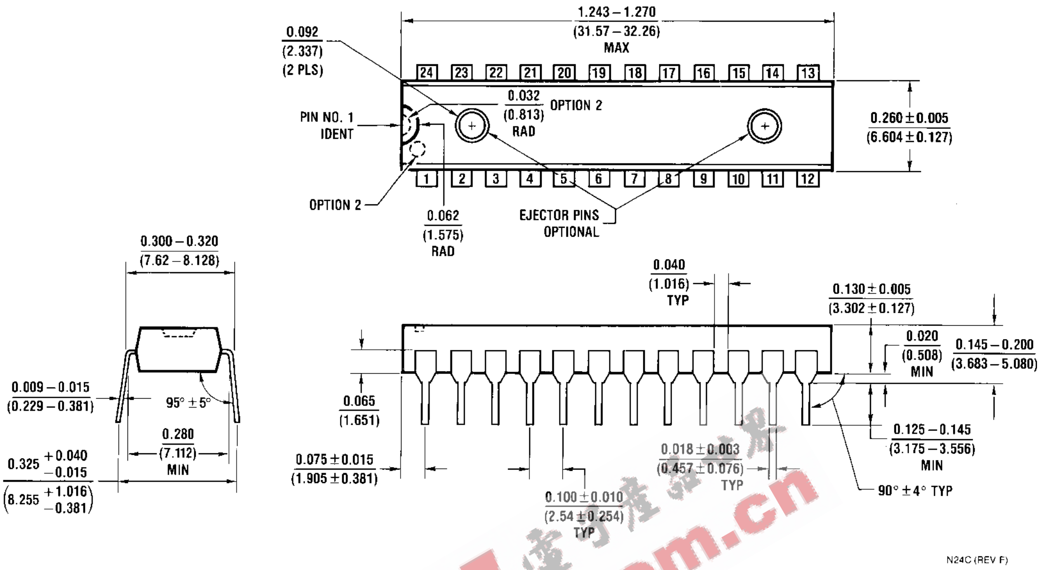
FIGURE 2. Simultaneous Switching Test Circuit

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N24C

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