

DATA SHEET

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74LVC244A/74LVCH244A

Octal buffer/line driver with 5-volt tolerant inputs/outputs (3-State)title

Product specification
Supersedes data of 1996 Sep 06
IC24 Data Handbook

1998 May 20

Octal buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

74LVC244A 74LVCH244A

FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Supply voltage range of 2.7V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- High impedance when $V_{CC} = 0V$
- Bushold on all data inputs (74LVCH244A only)

DESCRIPTION

The 74LVC244A/74LVCH244A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. These features allow the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC244A/74LVCH244A is an octal non-inverting buffer/line driver with 3-State outputs. The 3-State outputs are controlled by the output enable inputs $\overline{1OE}$ and $\overline{2OE}$. A HIGH on \overline{nOE} causes the outputs to assume a high impedance OFF-state. Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times.

The '244' is functionally identical to the '240', but the '240' has non-inverting outputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	$C_L = 50pF$ $V_{CC} = 3.3V$	3.5	ns
C_I	Input capacitance		4.4	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1 and 2	22.6	pF

NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is $V_I = GND$ to V_{CC} .

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic Shrink Small Outline (SO)	-40°C to +85°C	74LVC244A D	74LVC244A D	SOT163-1
20-Pin Plastic Shrink Small Outline (SSOP) Type II	-40°C to +85°C	74LVC244A DB	74LVC244A DB	SOT339-1
20-Pin Plastic Thin Shrink Small Outline (TSSOP) Type I	-40°C to +85°C	74LVC244A PW	7LVC244APW DH	SOT360-1
20-Pin Plastic Shrink Small Outline (SO)	-40°C to +85°C	74LVCH244A D	74LVCH244A D	SOT163-1
20-Pin Plastic Shrink Small Outline (SSOP) Type II	-40°C to +85°C	74LVCH244A DB	74LVCH244A DB	SOT339-1
20-Pin Plastic Thin Shrink Small Outline (TSSOP) Type I	-40°C to +85°C	74LVCH244A PW	LVCH244APW DH	SOT360-1

Octal buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

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PIN DESCRIPTION

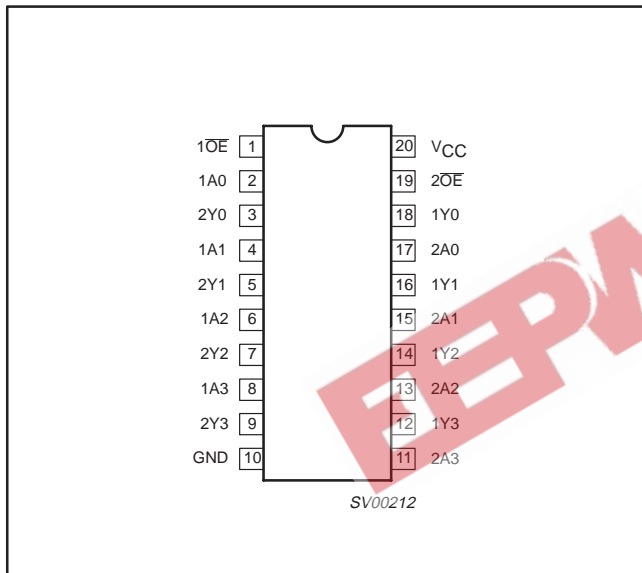
PIN NUMBER	SYMBOL	FUNCTION
1	1 \overline{OE}	Output enable input (active LOW)
2, 4, 6, 8	1A ₀ to 1A ₃	Data inputs
3, 5, 7, 9	2Y ₀ to 2Y ₃	Bus outputs
10	GND	Ground (0V)
17, 15, 13, 11	2A ₀ to 2A ₃	Bus inputs
18, 16, 14, 12	1Y ₀ to 1Y ₃	Bus outputs
19	2 \overline{OE}	Output enable input (active-LOW)
20	V _{CC}	Positive supply voltage

FUNCTION TABLE

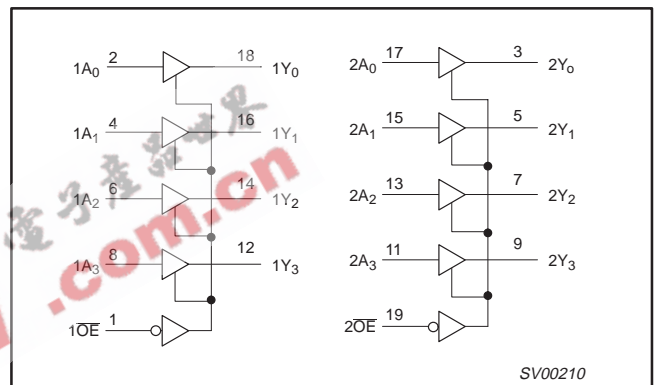
INPUTS		OUTPUT
n \overline{OE}	nA _n	nY _n
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance OFF-state

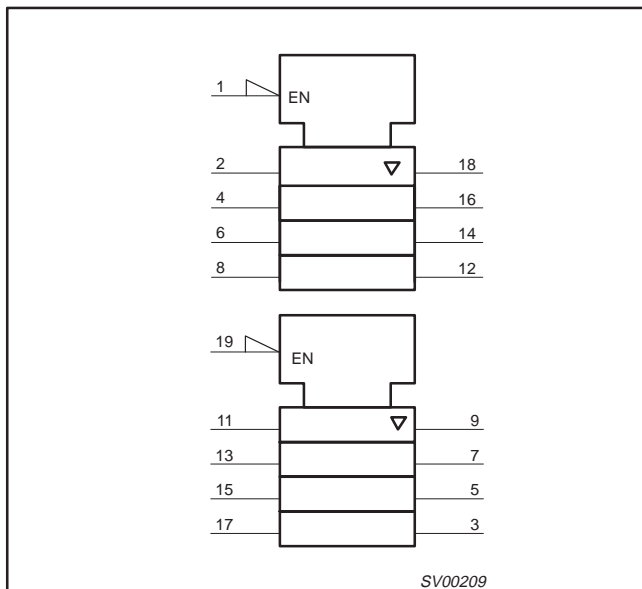
PIN CONFIGURATION



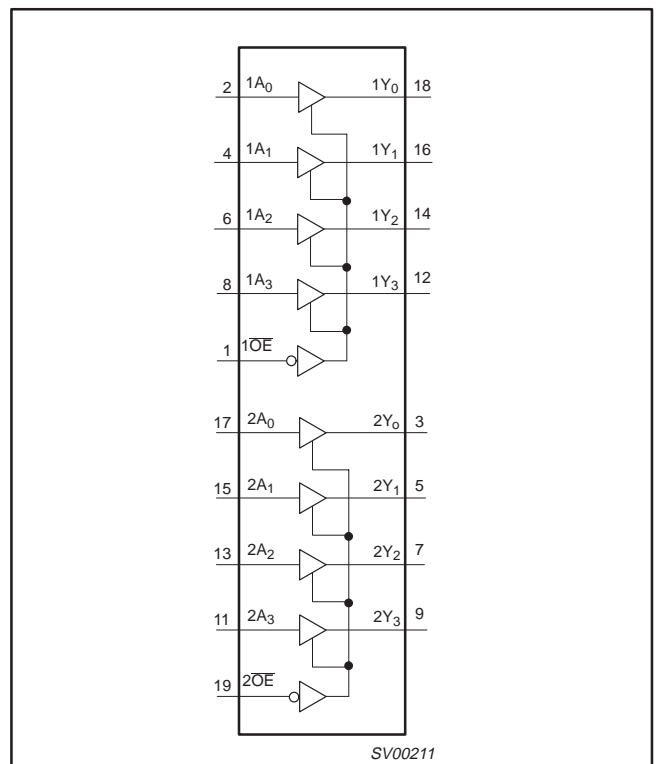
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



Octal buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

74LVC244A 74LVCH244A

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC Input voltage range		0	5.5	V
V_O	DC Output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range; output 3-State		0	5.5	
T_{amb}	Operating ambient temperature range in free-air		-40	+85	°C
t_r, t_f	Input rise and fall times	$V_{CC} = 1.2$ to $2.7V$ $V_{CC} = 2.7$ to $3.6V$	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS¹

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage	Note 2	-0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	± 50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	-0.5 to $V_{CC} + 0.5$	V
	DC output voltage; output 3-State	Note 2	-0.5 to 6.5	
I_O	DC output source or sink current	$V_O = 0$ to V_{CC}	± 50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		± 100	mA
T_{stg}	Storage temperature range		-65 to +150	°C
P_{TOT}	Power dissipation per package			
	- plastic mini-pack (SO) - plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	500 500	mW

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Octal buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V _{IH}	HIGH level Input voltage	V _{CC} = 1.2V	V _{CC}			V
		V _{CC} = 2.7 to 3.6V	2.0			
V _{IL}	LOW level Input voltage	V _{CC} = 1.2V			GND	V
		V _{CC} = 2.7 to 3.6V			0.8	
V _{OH}	HIGH level output voltage	V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = -12mA	V _{CC} - 0.5			V
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -100μA	V _{CC} - 0.2	V _{CC}		
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -18mA	V _{CC} - 0.6			
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -24mA	V _{CC} - 0.8			
V _{OL}	LOW level output voltage	V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 12mA			0.40	V
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 100μA		GND	0.20	
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 24mA			0.55	
I _I	Input leakage current	V _{CC} = 3.6V; V _I = 5.5V or GND		±0.1	±5	μA
I _{OZ}	3-State output OFF-state current	V _{CC} = 3.6V; V _I = V _{IH} or V _{IL} ; V _O = 5.5V or GND		0.1	±5	μA
I _{off}	Power off leakage supply	V _{CC} = 0.0V; V _I or V _O = 5.5V		0.1	±10	μA
I _{CC}	Quiescent supply current	V _{CC} = 3.6V; V _I = V _{CC} or GND; I _O = 0		0.1	10	μA
ΔI _{CC}	Additional quiescent supply current per input pin	V _{CC} = 2.7V to 3.6V; V _I = V _{CC} - 0.6V; I _O = 0		5	500	μA
I _{BHL}	Bushold LOW sustaining current ^{2, 3, 4}	V _{CC} = 3.0V; V _I = 0.8V	75	-	-	μA
I _{BHH}	Bushold HIGH sustaining current ^{2, 3, 4}	V _{CC} = 3.0V; V _I = 2.0V	-75	-	-	μA
I _{BHLO}	Bushold LOW overdrive current ^{2, 3, 5}	V _{CC} = 3.6V	500	-	-	μA
I _{BHHO}	Bushold HIGH overdrive current ^{2, 3, 5}	V _{CC} = 3.6V	-500	-	-	μA

NOTES:

- All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
- Valid for data inputs of bushold parts (LVCH-A) only.
- For data inputs only, control inputs do not have a bushold circuit
- The specified sustaining current at the data inputs do not have a bushold circuit.
- The specified overdrive current at the data input forces the data input to the opposite logic input state.
- For bushold parts, the bushold circuit is switched off when V_I exceeds V_{CC} allowing 5.5V on the input terminal.

Octal buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

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AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$			$V_{CC} = 2.7\text{V}$		$V_{CC} = 1.2\text{V}$	
			MIN	TYP ¹	MAX	MIN	MAX	TYP	
t_{PHL} t_{PLH}	Propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	1, 3	1.5	3.5	5.9	1.5	6.9	16.0	ns
t_{PZH} t_{PZL}	3-State output enable time $1OE$ to $1Y_n$; $2OE$ to $2Y_n$	2, 3	1.5	4.3	7.6	1.5	8.6	19.0	ns
t_{PHZ} t_{PLZ}	3-State output disable time $1OE$ to $1Y_n$; $2OE$ to $2Y_n$	2, 3	1.5	3.7	5.8	1.5	6.8	17.0	ns

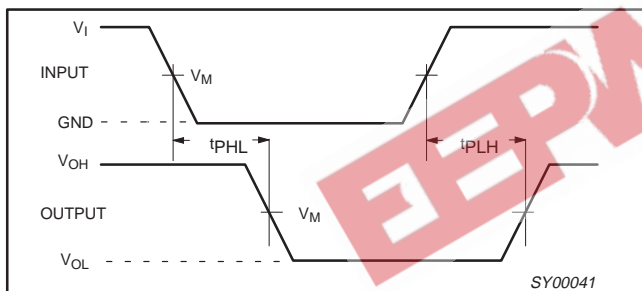
NOTE:

1. Unless otherwise stated, all typical values are at $V_{CC} = 3.3\text{V}$ and $T_{\text{amb}} = 25^\circ\text{C}$.

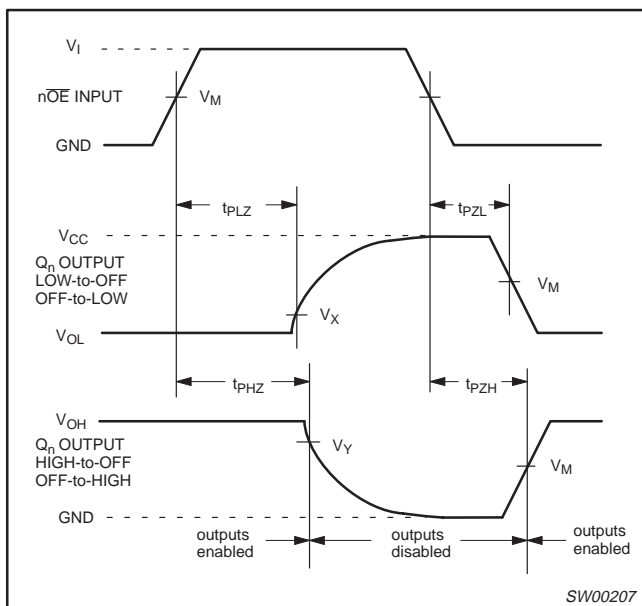
AC WAVEFORMS

$V_M = 1.5\text{V}$ at $V_{CC} \geq 2.7\text{V}$; $V_M = 0.5 V_{CC}$ at $V_{CC} < 2.7\text{V}$
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

$V_X = V_{OL} + 0.3\text{V}$ at $V_{CC} \geq 2.7\text{V}$; $V_X = V_{OL} + 0.1 V_{CC}$ at $V_{CC} < 2.7\text{V}$
 $V_Y = V_{OH} - 0.3\text{V}$ at $V_{CC} \geq 2.7\text{V}$; $V_Y = V_{OH} - 0.1 V_{CC}$ at $V_{CC} < 2.7\text{V}$

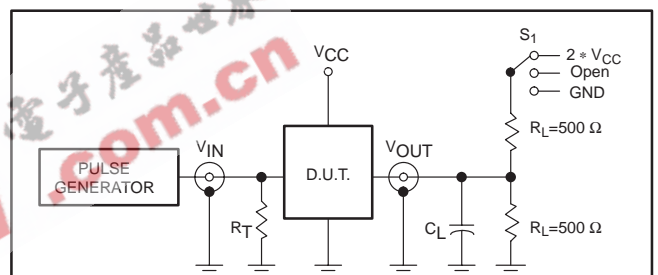


Waveform 1. Input (D_n) to output (Q_n) propagation delays.



Waveform 2. 3-State enable and disable times.

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
$t_{\text{PLH}}/t_{\text{PHL}}$	Open
$t_{\text{PLZ}}/t_{\text{PZL}}$	$2 * V_{CC}$
$t_{\text{PHZ}}/t_{\text{PZH}}$	GND

V_{CC}	V_{IN}
$< 2.7\text{V}$	V_{CC}
$2.7 - 3.6\text{V}$	2.7V

DEFINITIONS

R_L = Load resistor
 C_L = Load capacitance includes jig and probe capacitance
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00047

Waveform 3. Load circuitry for switching times.

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

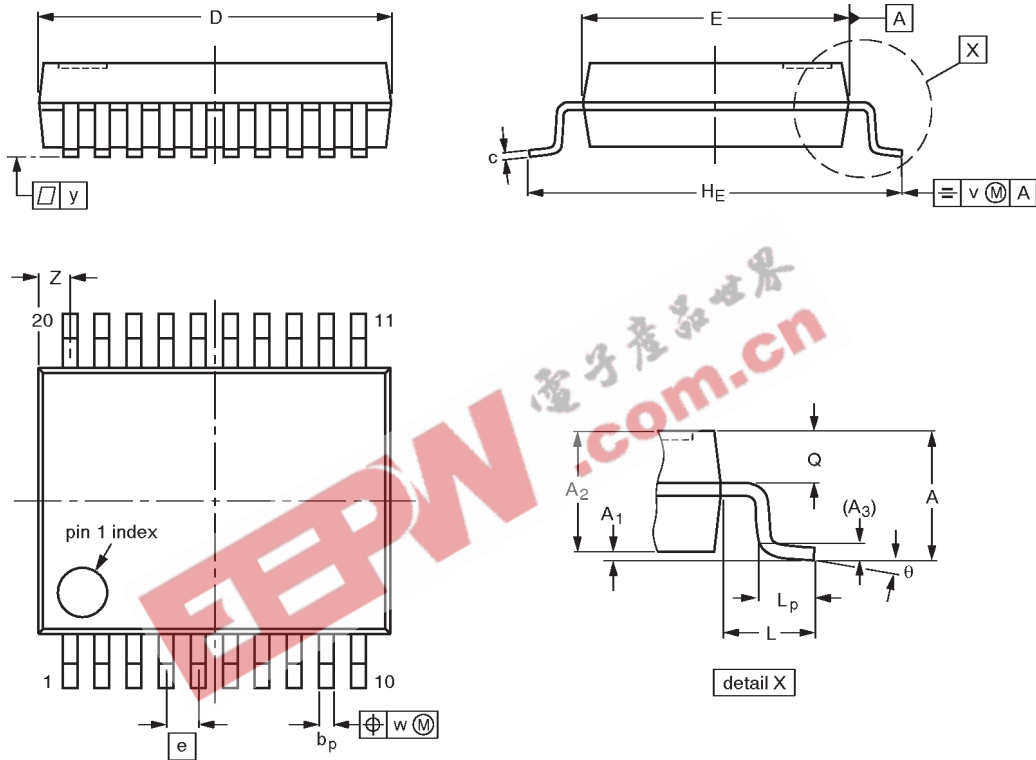
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				92-11-17 95-01-24

Octal buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

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SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

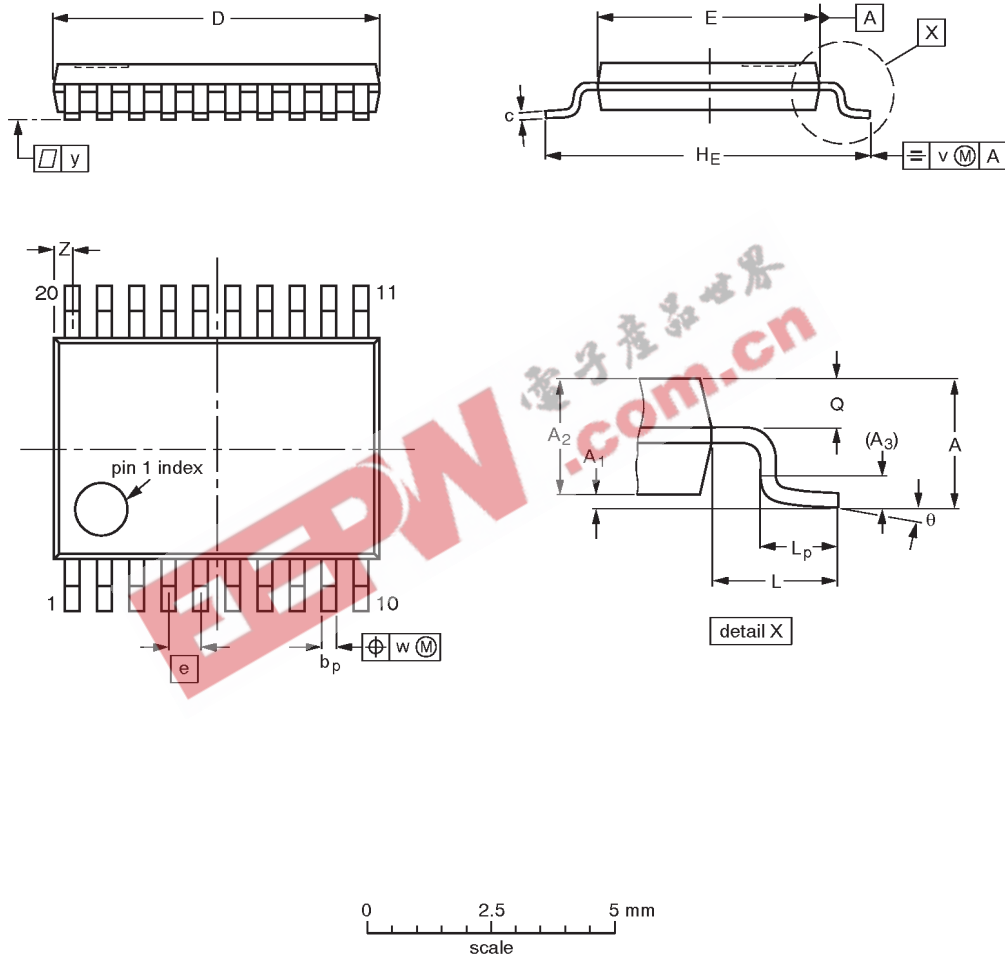
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				93-09-08 95-02-04

Octal buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				93-06-16 95-02-04

Octal buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

74LVC244A
74LVCH244A

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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