DATA SHEET

74HC1G125; 74HCT1G125
Bus buffer/line drivers; 3-state

Product specification
Supersedes data of 2002 May 17

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Bus buffer/line drivers; 3-state 74HC1G125; 74HCT1G125

FEATURES

- Wide supply voltage range from 2.0 to 6.0 V
- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- Very small 5 pins package
- Output capability: bus driver.

DESCRIPTION

The 74HC1G/HCT1G125 is a high-speed Si-gate CMOS device.

The 74HC1G/HCT1G125 provides one non-inverting buffer/line driver with 3-state output. The 3-state output is controlled by the output enable input pin ($\overline{OE}$). A HIGH at pin $\overline{OE}$ causes the output as assume a high-impedance OFF-state.

The bus driver output currents are equal compared to the 74HC/HCT125.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 6.0$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC1G	HCT1G	
t_{PHL}/t_{PLH}	propagation delay A to Y	C_L = 15 pF; V_{CC} = 5 V	9	10	ns
C_I	input capacitance		1.5	1.5	pF
C_{PD}	power dissipation capacitance	notes 1 and 2	30	27	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. For HC1G the condition is V_I = GND to V_{CC}.
   For HCT1G the condition is V_I = GND to V_{CC} − 1.5 V.

FUNCTION TABLE

See note 1.

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	L	L
L	H	H
H	X	Z

Note

1. H = HIGH voltage level;
   L = LOW voltage level;
   X = don't care;
   Z = high-impedance OFF-state.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74HC1G125GW	–40 to +125 °C	5	SC-88A	plastic	SOT353	HM
74HCT1G125GW	–40 to +125 °C	5	SC-88A	plastic	SOT353	TM
74HC1G125GV	–40 to +125 °C	5	SC-74A	plastic	SOT753	H25
74HCT1G125GV	–40 to +125 °C	5	SC-74A	plastic	SOT753	T25

PINNING

PIN	SYMBOL	DESCRIPTION
1	$\overline{OE}$	output enable input
2	A	data input A
3	GND	ground (0 V)
4	Y	data output Y
5	V_{CC}	supply voltage

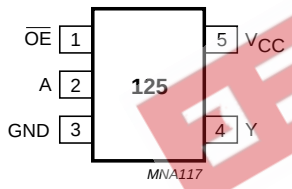


Fig.1 Pin configuration.

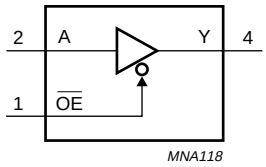


Fig.2 Logic symbol.

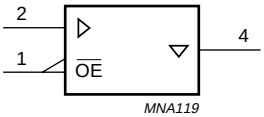


Fig.3 IEC logic symbol.

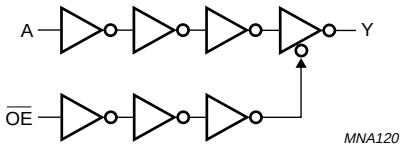


Fig.4 Logic diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC1G125			74HCT1G125			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	–	V_{CC}	0	–	V_{CC}	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+125	–40	+25	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 2.0 V	–	–	1000	–	–	–	ns
		V_{CC} = 4.5 V	–	–	500	–	–	500	ns
		V_{CC} = 6.0 V	–	–	400	–	–	–	ns

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+7.0	V
I_{IK}	input diode current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V; note 1	–	±20	mA
I_{OK}	output diode current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V; note 1	–	±20	mA
I_O	output source or sink current	-0.5 V $< V_O < V_{CC} + 0.5$ V; note 1	–	±12.5	mA
I_{CC}	V_{CC} or GND current	note 1	–	±25	mA
T_{stg}	storage temperature		–65	+150	°C
P_D	power dissipation per package	for temperature range from –40 to +125 °C; note 2	–	200	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 55 °C the value of P_D derates linearly with 2.5 mW/K.

DC CHARACTERISTICS

Family 74HC1G

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)					UNIT
		OTHER	V_{CC} (V)	–40 to +85			–40 to +125		
				MIN.	TYP.(1)	MAX.	MIN.	MAX.	
V_{IH}	HIGH-level input voltage		2.0	1.5	1.2	–	1.5	–	V
			4.5	3.15	2.4	–	3.15	–	V
			6.0	4.2	3.2	–	4.2	–	V
V_{IL}	LOW-level input voltage		2.0	–	0.8	0.5	–	0.5	V
			4.5	–	2.1	1.35	–	1.35	V
			6.0	–	2.8	1.8	–	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = -20$ µA	2.0	1.9	2.0	–	1.9	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -20$ µA	4.5	4.4	4.5	–	4.4	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -20$ µA	6.0	5.9	6.0	–	5.9	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -2.0$ mA	4.5	4.13	4.32	–	3.7	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -2.6$ mA	6.0	5.63	5.81	–	5.2	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = 20$ µA	2.0	–	0	0.1	–	0.1	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 20$ µA	4.5	–	0	0.1	–	0.1	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 20$ µA	6.0	–	0	0.1	–	0.1	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 2.0$ mA	4.5	–	0.15	0.33	–	0.4	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 2.6$ mA	6.0	–	0.16	0.33	–	0.4	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND	6.0	–	–	1.0	–	1.0	µA
I_{OZ}	3-state output current OFF-state	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND	6.0	–	–	5	–	10	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$	6.0	–	–	10	–	20	µA

Note

1. All typical values are measured at T_{amb} = 25 °C.

Family 74HCT1G

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)					UNIT
		OTHER	V_{CC} (V)	–40 to +85			–40 to +125		
				MIN.	TYP.(1)	MAX.	MIN.	MAX.	
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	1.6	–	2.0	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	1.2	0.8	–	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = –20$ µA	4.5	4.4	4.5	–	4.4	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = –2.0$ mA	4.5	4.13	4.32	–	3.7	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = 20$ µA	4.5	–	0	0.1	–	0.1	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 2.0$ mA	4.5	–	0.15	0.33	–	0.4	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND	5.5	–	–	1.0	–	1.0	µA
I_{OZ}	3-state output current OFF-state	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND	5.5	–	–	5	–	10	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$	5.5	–	–	10	–	20	µA
ΔI_{CC}	additional supply current per input	$V_I = V_{CC} – 2.1$ V; $I_O = 0$	4.5 to 5.5	–	–	500	–	850	µA

Note

1. All typical values are measured at $T_{amb} = 25$ °C.

AC CHARACTERISTICS

Type 74HC1G125

GND = 0 V; $t_r = t_f \leq 6.0$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)					UNIT
		WAVEFORMS	V_{CC} (V)	–40 to +85			–40 to +125		
				MIN.	TYP.(1)	MAX.	MIN.	MAX.	
t_{PHL}/t_{PLH}	propagation delay A to Y	see Figs 5 and 7	2.0	–	24	125	–	150	ns
			4.5	–	10	25	–	30	ns
			6.0	–	8	21	–	26	ns
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Y	see Figs 6 and 7	2.0	–	19	155	–	190	ns
			4.5	–	9	31	–	38	ns
			6.0	–	7	26	–	32	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Y	see Figs 6 and 7	2.0	–	18	155	–	190	ns
			4.5	–	12	31	–	38	ns
			6.0	–	11	26	–	32	ns

Note

1. All typical values are measured at $T_{amb} = 25$ °C.

Type 74HCT1G125

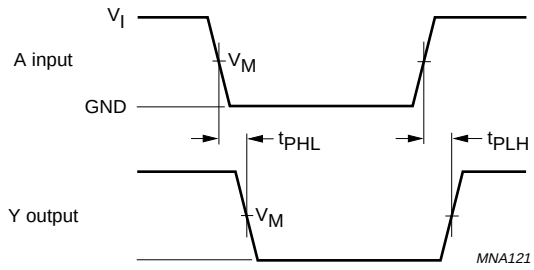
GND = 0 V; $t_r = t_f \leq 6.0$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)					UNIT
		WAVEFORMS	V_{CC} (V)	–40 to +85			–40 to +125		
				MIN.	TYP.(1)	MAX.	MIN.	MAX.	
t_{PHL}/t_{PLH}	propagation delay A to Y	see Figs 5 and 7	4.5	–	11	30	–	36	ns
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Y	see Figs 6 and 7	4.5	–	10	35	–	42	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Y	see Figs 6 and 7	4.5	–	11	31	–	38	ns

Note

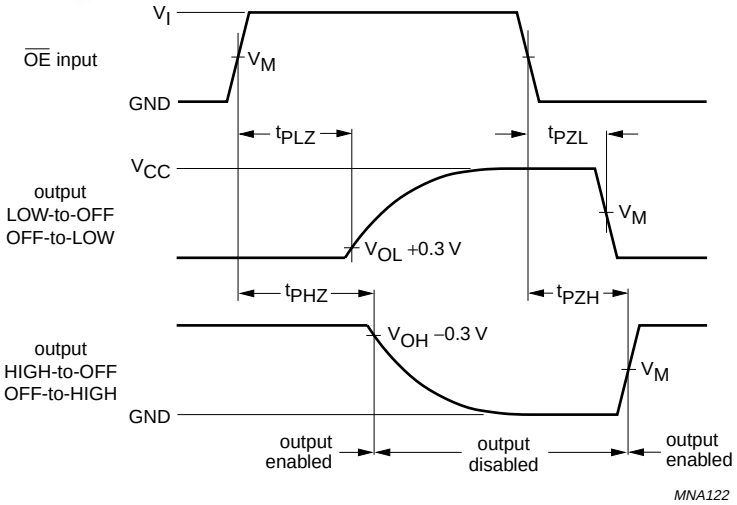
1. All typical values are measured at $T_{amb} = 25$ °C.

AC WAVEFORMS



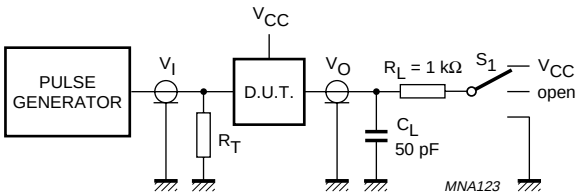
For HC1G: V_M = 50%; V_I = GND to V_{CC}.
For HCT1G: V_M = 1.3 V; V_I = GND to 3.0 V.

Fig.5 The input (A) to output (Y) propagation delays.



For HC1G: V_M = 50%; V_I = GND to V_{CC}.
For HCT1G: V_M = 1.3 V; V_I = GND to 3.0 V.

Fig.6 The 3-state enable and disable times.



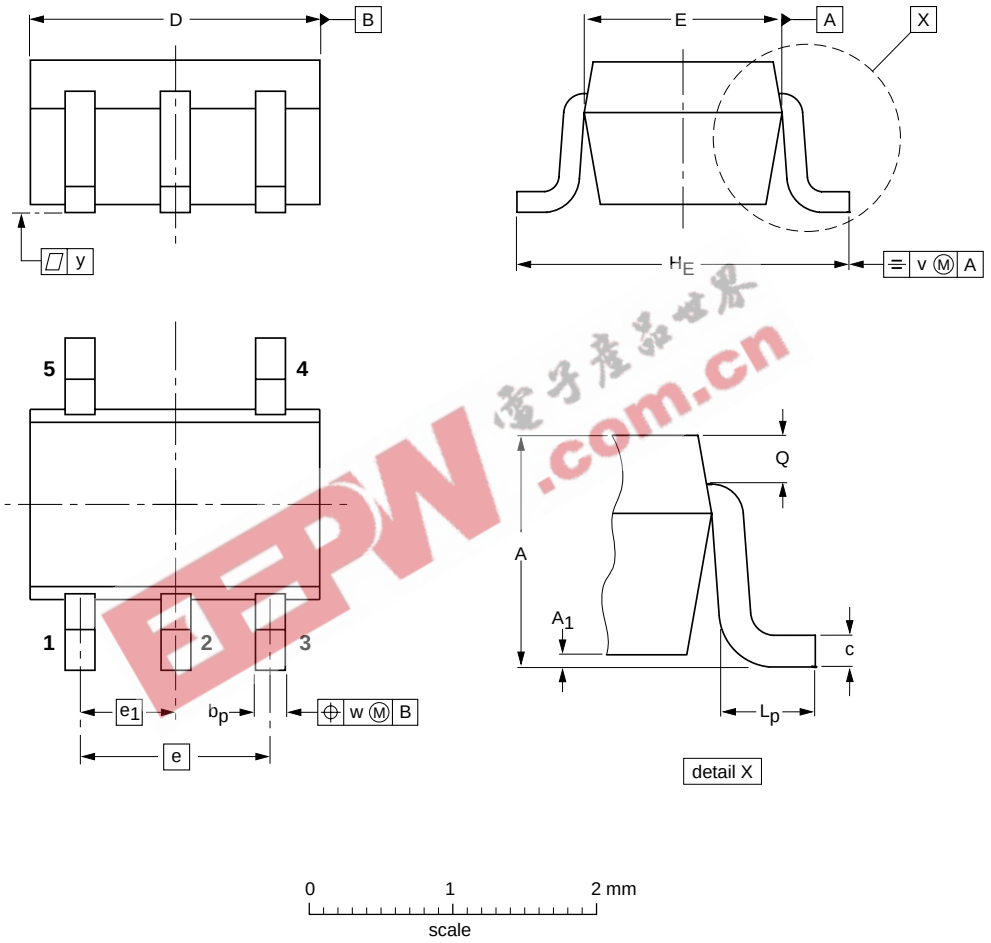
TEST	S_1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

Definitions for test circuit:
C_L = load capacitance including jig and probe capacitance (see “AC characteristics”).
R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.7 Load circuitry for switching times.

PACKAGE OUTLINES

Plastic surface mounted package; 5 leads **SOT353**

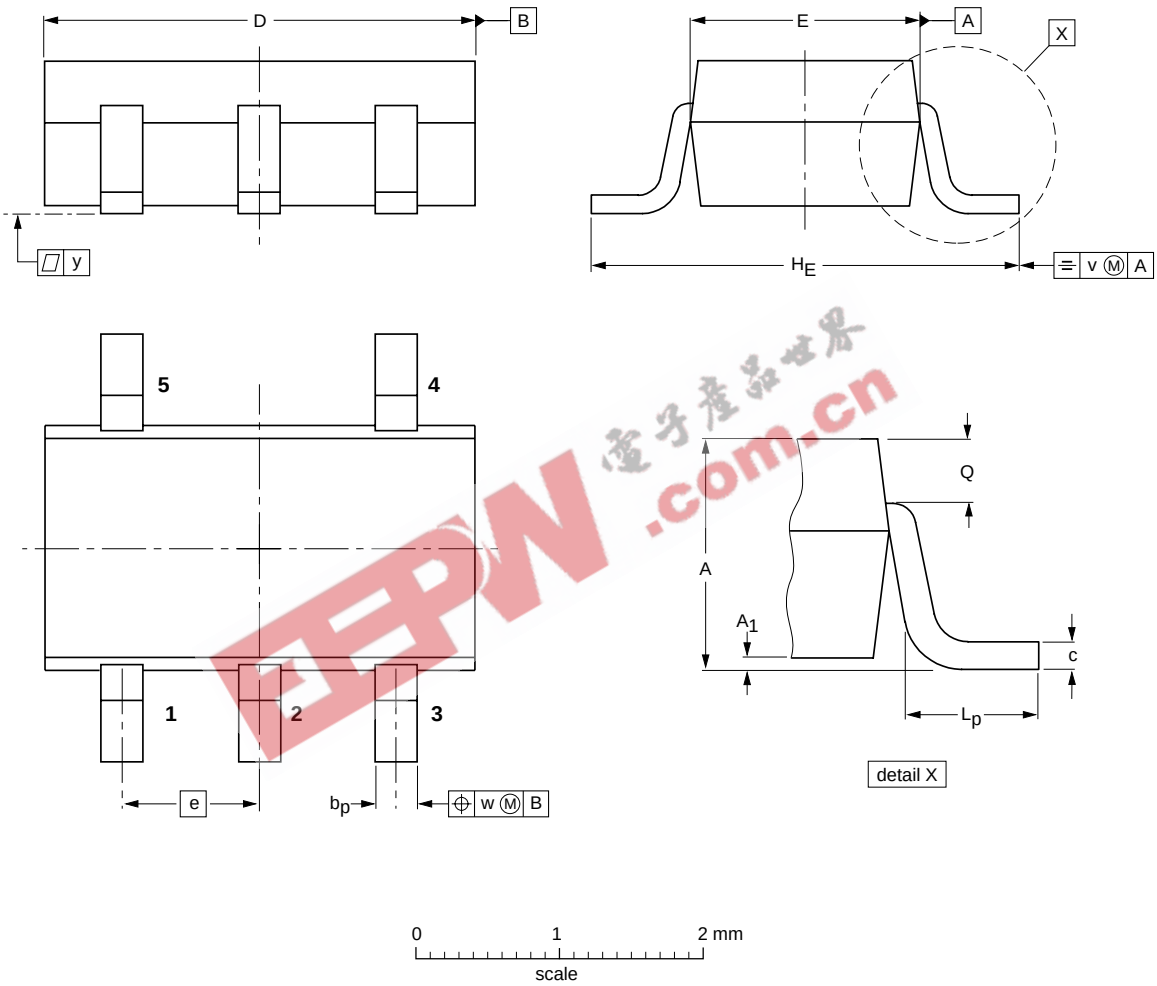


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E (2)	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT353			SC-88A			97-02-28

Plastic surface mounted package; 5 leads **SOT753**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.100 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT753			SC-74A			02-04-16

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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