

# DATA SHEET

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## 74LVC2G126

Dual bus buffer/line driver; 3-state

Product specification  
Supersedes data of 2003 Sep 01

2004 Sep 22

## Dual bus buffer/line driver; 3-state

## 74LVC2G126

## FEATURES

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V).
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- $\pm 24$  mA output drive ( $V_{CC} = 3.0$  V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from  $-40$  °C to  $+85$  °C and  $-40$  °C to  $+125$  °C.

## DESCRIPTION

The 74LVC2G126 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. These feature allows the use of these devices as translators in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74LVC2G126 provides a dual non-inverting buffer/line driver with 3-state output. The 3-state output is controlled by the output enable input (pin nOE). A LOW-level at pin nOE causes the output to assume a high-impedance OFF-state. Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25$  °C.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	propagation delay inputs nA to output nY	$V_{CC} = 1.8$ V; $C_L = 30$ pF; $R_L = 1$ k $\Omega$	3.9	ns
		$V_{CC} = 2.5$ V; $C_L = 30$ pF; $R_L = 500$ $\Omega$	2.6	ns
		$V_{CC} = 2.7$ V; $C_L = 50$ pF; $R_L = 500$ $\Omega$	2.8	ns
		$V_{CC} = 3.3$ V; $C_L = 50$ pF; $R_L = 500$ $\Omega$	2.4	ns
		$V_{CC} = 5.0$ V; $C_L = 50$ pF; $R_L = 500$ $\Omega$	1.9	ns
$C_I$	input capacitance		2	pF
$C_{PD}$	power dissipation capacitance per buffer	output enabled; notes 1 and 2	17	pF
		output disabled; notes 1 and 2	5	pF

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts;

$N$  = total load switching outputs;

$\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

2. The condition is  $V_I = \text{GND}$  to  $V_{CC}$ .

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## FUNCTION TABLE

See note 1.

INPUT		OUTPUT
nOE	nA	nY
H	L	L
H	H	H
L	X	Z

## Note

- H = HIGH voltage level;  
L = LOW voltage level;  
X = don't care;  
Z = high-impedance OFF-state.

## ORDERING INFORMATION

TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74LVC2G126DP	-40 °C to +125 °C	8	TSSOP8	plastic	SOT505-2	V126
74LVC2G126DC	-40 °C to +125 °C	8	VSSOP8	plastic	SOT765-1	V26
74LVC2G126GM	-40 °C to +125 °C	8	XSON8	plastic	SOT833-1	V26

## PINNING

PIN	SYMBOL	DESCRIPTION
1	1OE	output enable input
2	1A	data input
3	2Y	data output
4	GND	ground (0 V)
5	2A	data input
6	1Y	data output
7	2OE	output enable input
8	V <sub>CC</sub>	supply voltage

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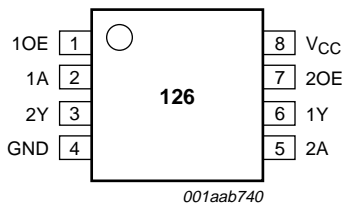
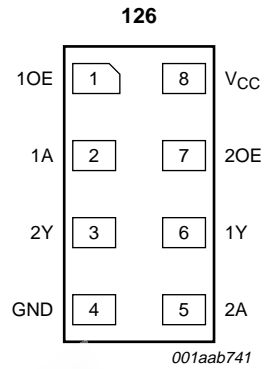


Fig.1 Pin configuration TSSOP8 and VSSOP8.



Transparent top view

Fig.2 Pin configuration XSON8.

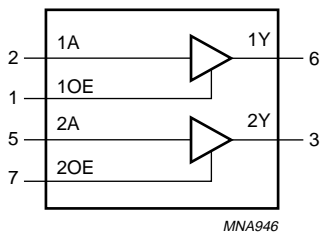


Fig.3 Logic symbol.

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		1.65	5.5	V
$V_I$	input voltage		0	5.5	V
$V_O$	output voltage	$V_{CC} = 1.65\text{ V to }5.5\text{ V}$ ; enable mode	0	$V_{CC}$	V
		$V_{CC} = 1.65\text{ V to }5.5\text{ V}$ ; disable mode	0	5.5	V
		$V_{CC} = 0\text{ V}$ ; Power-down mode	0	5.5	V
$T_{amb}$	operating ambient temperature		-40	+125	°C
$t_r, t_f$	input rise and fall times	$V_{CC} = 1.65\text{ V to }2.7\text{ V}$	0	20	ns/V
		$V_{CC} = 2.7\text{ V to }5.5\text{ V}$	0	10	ns/V

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input diode current	$V_I < 0\text{ V}$	-	-50	mA
$V_I$	input voltage	note 1	-0.5	+6.5	V
$I_{OK}$	output diode current	$V_O > V_{CC}$ or $V_O < 0\text{ V}$	-	±50	mA
$V_O$	output voltage	enable mode; notes 1 and 2	-0.5	$V_{CC} + 0.5$	V
		disable mode; notes 1 and 2	-0.5	+6.5	V
		Power-down mode; notes 1 and 2	-0.5	+6.5	V
$I_O$	output source or sink current	$V_O = 0\text{ V to }V_{CC}$	-	±50	mA
$I_{CC}, I_{GND}$	$V_{CC}$ or GND current		-	±100	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	power dissipation	$T_{amb} = -40\text{ °C to }+125\text{ °C}$	-	300	mW

## Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. When  $V_{CC} = 0\text{ V}$  (Power-down mode), the output voltage can be 5.5 V in normal operation.

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## DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
T <sub>amb</sub> = -40 °C to +85 °C; note 1							
V <sub>IH</sub>	HIGH-level input voltage		1.65 to 1.95	0.65 × V <sub>CC</sub>	–	–	V
			2.3 to 2.7	1.7	–	–	V
			2.7 to 3.6	2.0	–	–	V
			4.5 to 5.5	0.7 × V <sub>CC</sub>	–	–	V
V <sub>IL</sub>	LOW-level input voltage		1.65 to 1.95	–	–	0.35 × V <sub>CC</sub>	V
			2.3 to 2.7	–	–	0.7	V
			2.7 to 3.6	–	–	0.8	V
			4.5 to 5.5	–	–	0.3 × V <sub>CC</sub>	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 100 μA	1.65 to 5.5	–	–	0.1	V
		I <sub>O</sub> = 4 mA	1.65	–	–	0.45	V
		I <sub>O</sub> = 8 mA	2.3	–	–	0.3	V
		I <sub>O</sub> = 12 mA	2.7	–	–	0.4	V
		I <sub>O</sub> = 24 mA	3.0	–	–	0.55	V
		I <sub>O</sub> = 32 mA	4.5	–	–	0.55	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -100 μA	1.65 to 5.5	V <sub>CC</sub> - 0.1	–	–	V
		I <sub>O</sub> = -4 mA	1.65	1.2	–	–	V
		I <sub>O</sub> = -8 mA	2.3	1.9	–	–	V
		I <sub>O</sub> = -12 mA	2.7	2.2	–	–	V
		I <sub>O</sub> = -24 mA	3.0	2.3	–	–	V
		I <sub>O</sub> = -32 mA	4.5	3.8	–	–	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	5.5	–	±0.1	±5	μA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND	3.6	–	±0.1	±10	μA
I <sub>off</sub>	power OFF leakage current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0	–	±0.1	±10	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	5.5	–	0.1	10	μA
ΔI <sub>CC</sub>	additional quiescent supply current per pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	2.3 to 5.5	–	5	500	μA

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.65 to 1.95	0.65 × V <sub>CC</sub>	–	–	V
			2.3 to 2.7	1.7	–	–	V
			2.7 to 3.6	2.0	–	–	V
			4.5 to 5.5	0.7 × V <sub>CC</sub>	–	–	V
V <sub>IL</sub>	LOW-level input voltage		1.65 to 1.95	–	–	0.35 × V <sub>CC</sub>	V
			2.3 to 2.7	–	–	0.7	V
			2.7 to 3.6	–	–	0.8	V
			4.5 to 5.5	–	–	0.3 × V <sub>CC</sub>	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 100 μA	1.65 to 5.5	–	–	0.1	V
		I <sub>O</sub> = 4 mA	1.65	–	–	0.70	V
		I <sub>O</sub> = 8 mA	2.3	–	–	0.45	V
		I <sub>O</sub> = 12 mA	2.7	–	–	0.60	V
		I <sub>O</sub> = 24 mA	3.0	–	–	0.80	V
		I <sub>O</sub> = 32 mA	4.5	–	–	0.80	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -100 μA	1.65 to 5.5	V <sub>CC</sub> - 0.1	–	–	V
		I <sub>O</sub> = -4 mA	1.65	0.95	–	–	V
		I <sub>O</sub> = -8 mA	2.3	1.7	–	–	V
		I <sub>O</sub> = -12 mA	2.7	1.9	–	–	V
		I <sub>O</sub> = -24 mA	3.0	2.0	–	–	V
		I <sub>O</sub> = -32 mA	4.5	3.4	–	–	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	5.5	–	–	±20	μA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND	3.6	–	–	±20	μA
I <sub>off</sub>	power OFF leakage current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0	–	–	±20	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	5.5	–	–	40	μA
ΔI <sub>CC</sub>	additional quiescent supply current per pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	2.3 to 5.5	–	–	5000	μA

**Note**

1. All typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

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## AC CHARACTERISTICS

GND = 0 V.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 °C to +85 °C; note 1</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nA to nY	see Figs 4 and 6	1.65 to 1.95	1.0	3.9	9.8	ns
			2.3 to 2.7	0.5	2.6	4.9	ns
			2.7	1.0	2.8	4.7	ns
			3.0 to 3.6	0.5	2.4	4.3	ns
			4.5 to 5.5	0.5	1.9	3.2	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time nOE to nY	see Figs 5 and 6	1.65 to 1.95	1.0	4.1	10.0	ns
			2.3 to 2.7	1.0	2.6	5.0	ns
			2.7	1.0	2.8	4.7	ns
			3.0 to 3.6	1.0	2.4	4.1	ns
			4.5 to 5.5	0.5	1.8	3.1	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time nOE to nY	see Figs 5 and 6	1.65 to 1.95	1.0	3.3	12.6	ns
			2.3 to 2.7	0.5	1.9	5.7	ns
			2.7	1.5	3.0	4.8	ns
			3.0 to 3.6	1.0	2.5	4.4	ns
			4.5 to 5.5	0.5	1.8	3.3	ns
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nA to nY	see Figs 4 and 6	1.65 to 1.95	1.0	–	12.3	ns
			2.3 to 2.7	0.5	–	6.3	ns
			2.7	1.0	–	5.9	ns
			3.0 to 3.6	0.5	–	5.4	ns
			4.5 to 5.5	0.5	–	4.0	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time nOE to nY	see Figs 5 and 6	1.65 to 1.95	1.0	–	12.5	ns
			2.3 to 2.7	1.0	–	6.3	ns
			2.7	1.0	–	5.9	ns
			3.0 to 3.6	1.0	–	5.1	ns
			4.5 to 5.5	0.5	–	3.9	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time nOE to nY	see Figs 5 and 6	1.65 to 1.95	1.0	–	15.4	ns
			2.3 to 2.7	0.5	–	7.5	ns
			2.7	1.5	–	6.2	ns
			3.0 to 3.6	1.0	–	5.7	ns
			4.5 to 5.5	0.5	–	4.4	ns

## Note

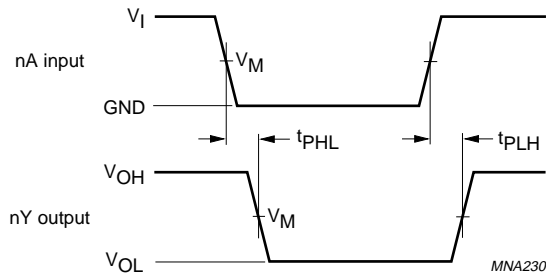
1. All typical values are measured at T<sub>amb</sub> = 25 °C.



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AC WAVEFORMS



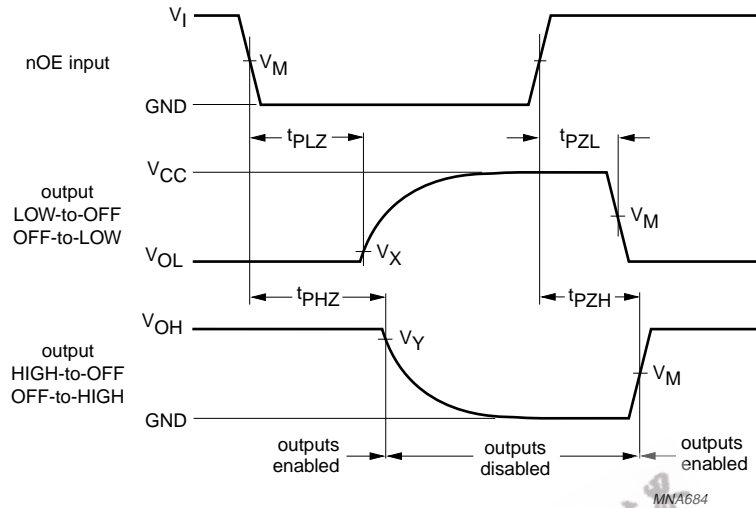
V <sub>CC</sub>	V <sub>M</sub>	INPUT	
		V <sub>I</sub>	t <sub>r</sub> = t <sub>f</sub>
1.65 V to 1.95 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	≤ 2.0 ns
2.3 V to 2.7 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 V to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 V to 5.5 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	≤ 2.5 ns

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

Fig.4 The input (nA) to output (nY) propagation delays and the output transition times.

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V <sub>CC</sub>	V <sub>M</sub>	INPUT	
		V <sub>I</sub>	t <sub>r</sub> = t <sub>f</sub>
1.65 V to 1.95 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	≤ 2.0 ns
2.3 V to 2.7 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 V to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 V to 5.5 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	≤ 2.5 ns

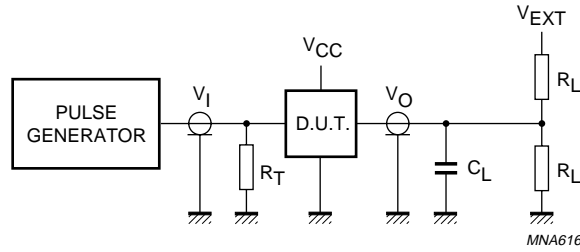
V<sub>X</sub> = V<sub>OL</sub> + 0.3 V at V<sub>CC</sub> ≥ 2.7 V;  
 V<sub>X</sub> = V<sub>OL</sub> + 0.15 V at V<sub>CC</sub> < 2.7 V;  
 V<sub>Y</sub> = V<sub>OH</sub> - 0.3 V at V<sub>CC</sub> ≥ 2.7 V;  
 V<sub>Y</sub> = V<sub>OH</sub> - 0.15 V at V<sub>CC</sub> < 2.7 V.

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

Fig.5 3-state enable and disable times.

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V <sub>CC</sub>	V <sub>I</sub>	C <sub>L</sub>	R <sub>L</sub>	V <sub>EXT</sub>		
				t <sub>PLH</sub> /t <sub>PHL</sub>	t <sub>PZH</sub> /t <sub>PHZ</sub>	t <sub>PZL</sub> /t <sub>PLZ</sub>
1.65 V to 1.95 V	V <sub>CC</sub>	30 pF	1 kΩ	open	GND	2 × V <sub>CC</sub>
2.3 V to 2.7 V	V <sub>CC</sub>	30 pF	500 Ω	open	GND	2 × V <sub>CC</sub>
2.7 V	2.7 V	50 pF	500 Ω	open	GND	6 V
3.0 V to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	6 V
4.5 V to 5.5 V	V <sub>CC</sub>	50 pF	500 Ω	open	GND	2 × V <sub>CC</sub>

Definitions for test circuit:

R<sub>L</sub> = Load resistor.

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

R<sub>T</sub> = Termination resistance should be equal to the output impedance Z<sub>o</sub> of the pulse generator.

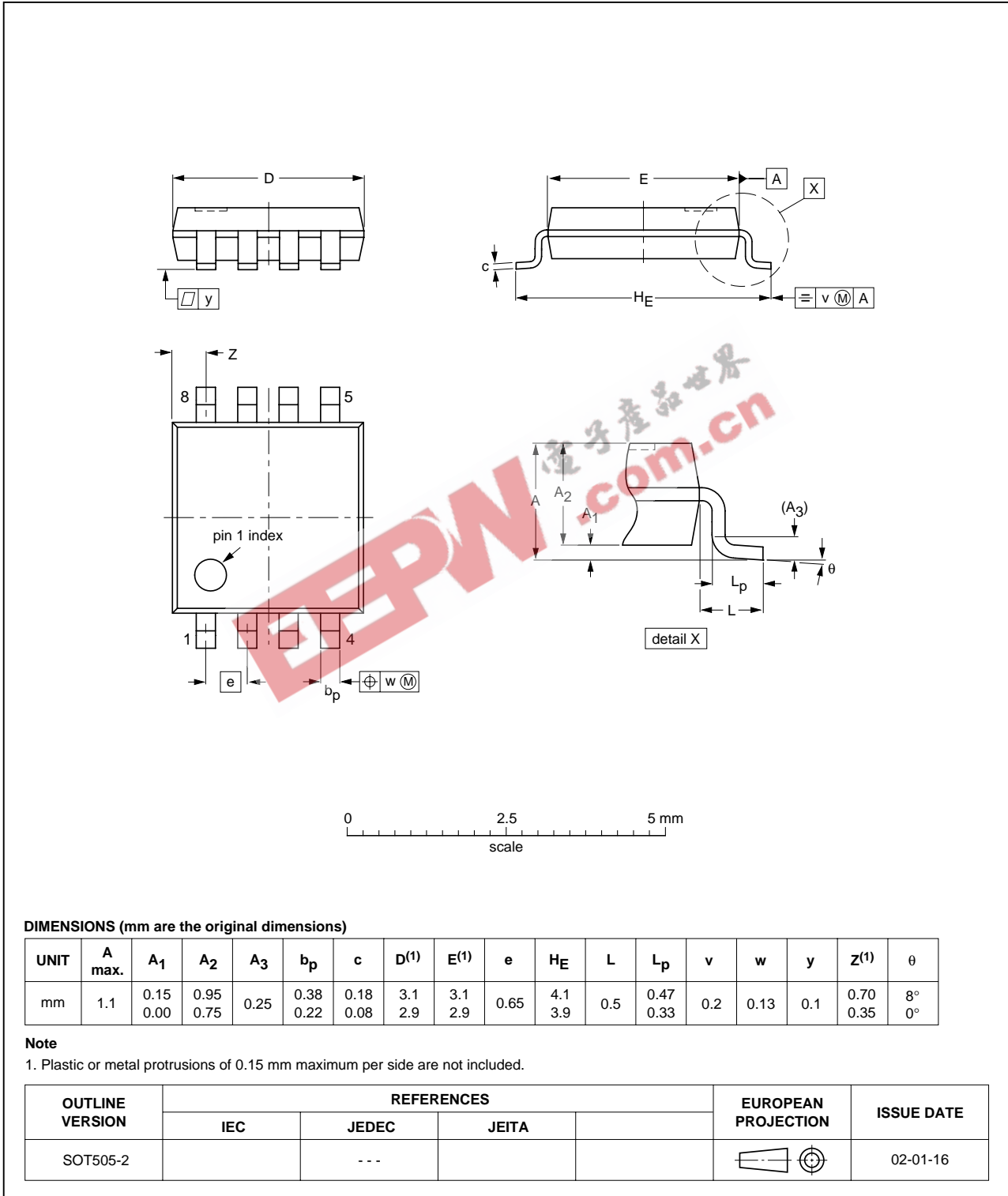
Fig.6 Load circuitry for switching times.

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PACKAGE OUTLINES

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

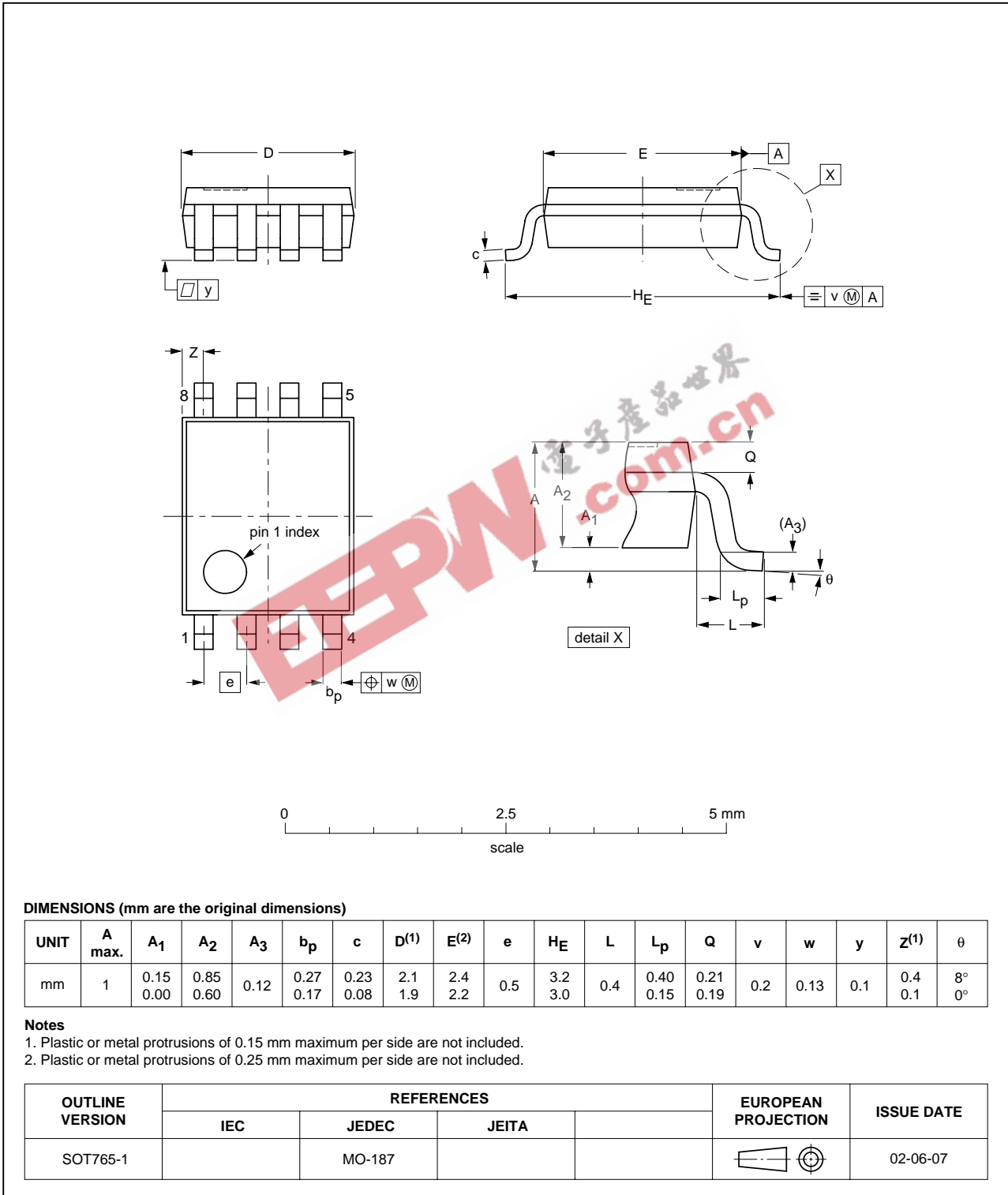


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VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

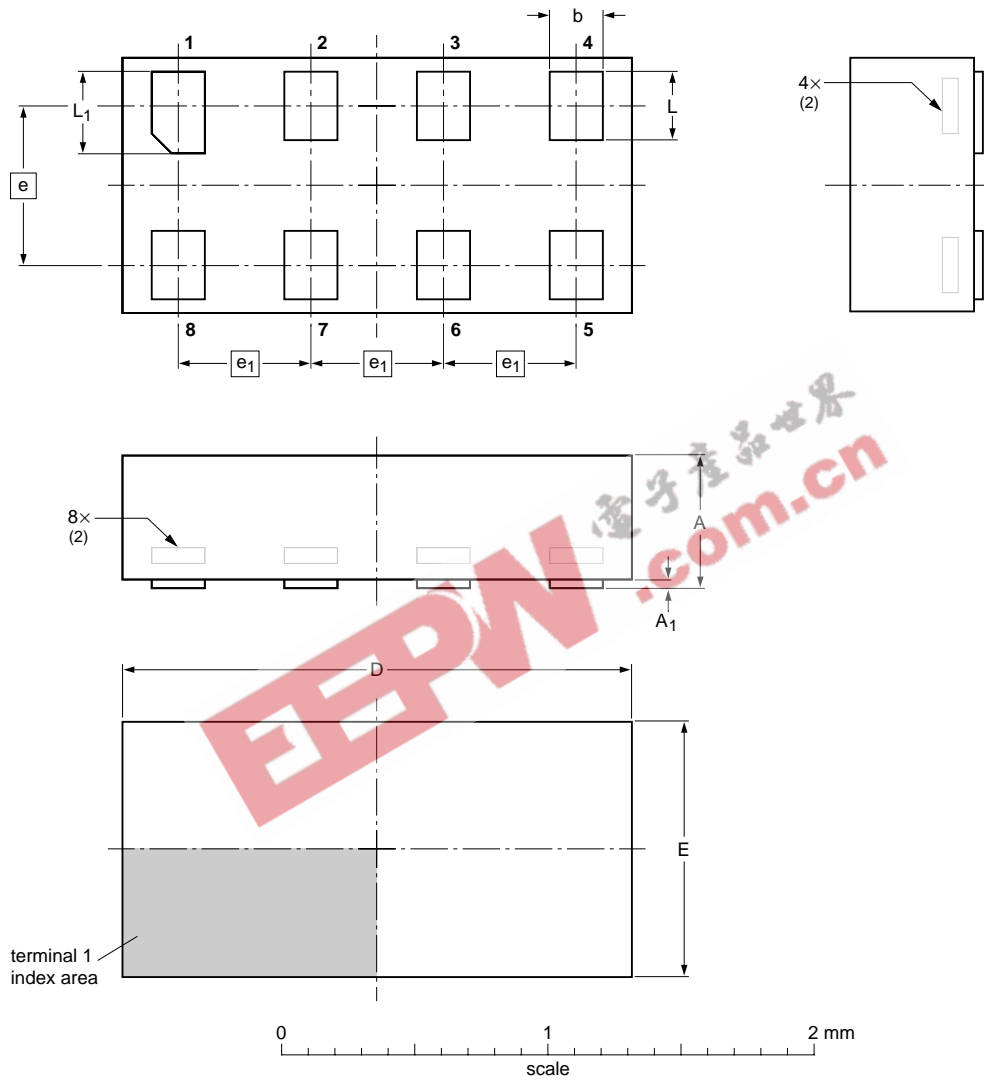


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XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 0.95 x 1.95 x 0.5 mm

SOT833-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A <sup>(1)</sup> max	A <sub>1</sub> max	b	D	E	e	e <sub>1</sub>	L	L <sub>1</sub>
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.0 0.9	0.6	0.5	0.35 0.27	0.40 0.32

**Notes**

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT833-1	---	MO-252	---		04-07-15 04-07-22

## Dual bus buffer/line driver; 3-state

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## DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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## **Contact information**

For additional information please visit <http://www.semiconductors.philips.com>. Fax: +31 40 27 24825  
For sales offices addresses send e-mail to: [sales.addresses@www.semiconductors.philips.com](mailto:sales.addresses@www.semiconductors.philips.com).

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