

DATA SHEET

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74ALS240A/74ALS240A-1 Octal inverter buffer (3-State)

Product specification
IC05 Data Handbook

1991 Feb 08

Octal inverter buffer (3-State)

74ALS240A/ 74ALS240A-1

FEATURES

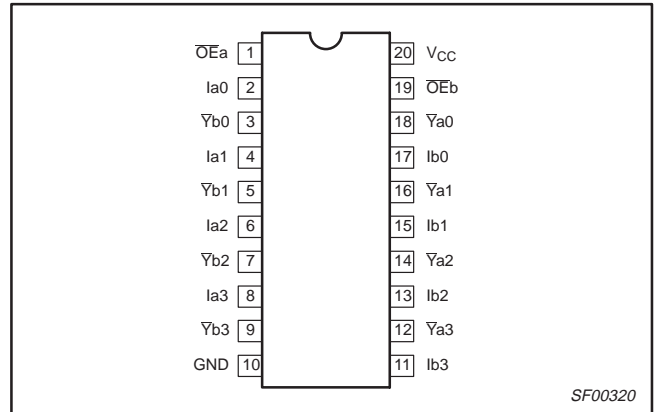
- Octal bus interface
- 3-State buffer outputs sink 24mA and source 15mA
- The -1 version sinks 48 mA

DESCRIPTION

The 74ALS240A is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The outputs are all capable of sinking 24mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two output enables, $\overline{OE}a$ and $\overline{OE}b$, each controlling four of the 3-State outputs.

The 74ALS240A-1 sinks 48 mA I_{OL} if the V_{CC} is limited to 5.0V $\pm 0.25V$.

PIN CONFIGURATION



SF00320

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS240A	4.5ns	15mA
74ALS240A-1	4.5ns	15mA

ORDERING INFORMATION

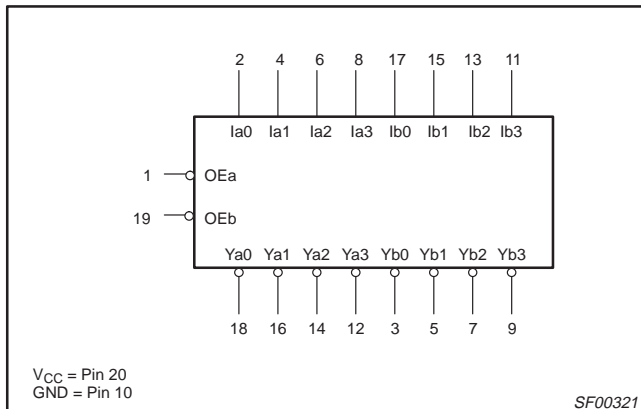
DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	
20-pin plastic DIP	74ALS240AN, 74ALS240A-1N	SOT146-1
20-pin plastic SOL	74ALS240AD, 74ALS240A-1D	SOT163-1
20-pin plastic SSOP Type II	74ALS240ADB, 74ALS240A-1DB	SOT339-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ian, Ibn	Data inputs	1.0/1.0	20 μ A/0.1mA
$\overline{OE}a$, $\overline{OE}b$	Output Enable inputs (active-Low)	1.0/1.0	20 μ A/0.1mA
$\overline{Y}an$, $\overline{Y}bn$	Data outputs	750/240	15mA/24mA
Yan, Ybn	Data outputs (-1 version)	750/480	15mA/48mA

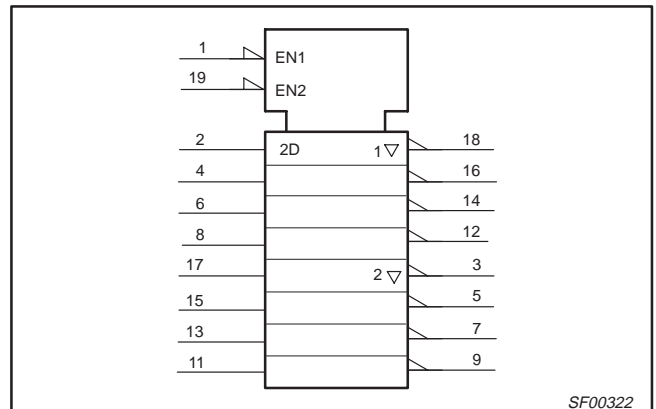
NOTE: One (1.0) ALS unit load is defined as: 20 μ A in the High state and 0.1mA in the Low state.

LOGIC SYMBOL



SF00321

IEC/IEEE SYMBOL

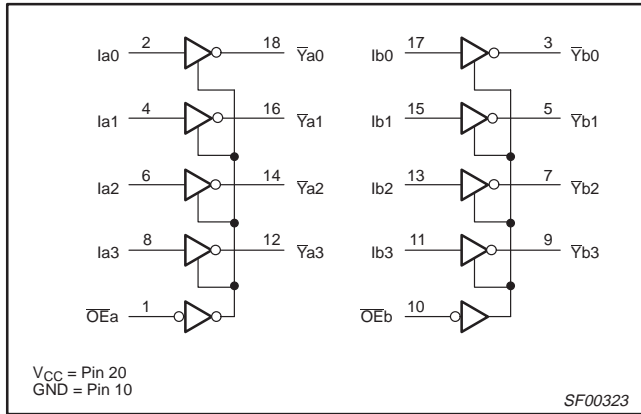


SF00322

Octal inverter buffer (3-State)

74ALS240A/
74ALS240A-1

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	
\overline{OEa}	Ia	\overline{OEb}	Ib	\overline{Ya}	\overline{Yb}
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	-0.5 to +7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +5	mA
V _{OUT}	Voltage applied to output in High output state	-0.5 to V _{CC}	V
I _{OUT}	Current applied to output in Low output state	All versions	48
		-1 version	96
T _{amb}	Operating free-air temperature range	0 to +70	°C
T _{stg}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			V
V _{IL}	Low-level input voltage			0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	High-level output current			-15	mA
I _{OL}	Low-level output current	All versions		24	mA
		-1 version		48 ¹	mA
T _{amb}	Operating free-air temperature range	0		+70	°C

NOTE:

1. The 48mA limit applies only under the condition of V_{CC} = 5.0V ±5%.

Octal inverter buffer (3-State)

74ALS240A/
74ALS240A-1**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹		LIMITS			UNIT
					MIN	TYP ²	MAX	
V _{OH}	High-level output voltage		V _{CC} ±10%, V _{IL} = MAX, V _{IH} = MIN	I _{OH} = -0.4mA	V _{CC} - 2			V
				I _{OH} = -3mA	2.4	3.2		V
			V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OH} = -15mA	2.0			
V _{OL}	Low-level output voltage	All versions	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OL} = 12mA		0.25	0.40	V
				I _{OL} = 24mA		0.35	0.50	V
		-1 version	V _{CC} = 4.75V, V _{IL} = MAX, V _{IH} = MIN	I _{OL} = 48mA		0.35	0.50	V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = I _{IK}			-0.73	-1.5	V
I _I	Input current at maximum input voltage		V _{CC} = MAX, V _I = 7.0V				0.1	mA
I _{IH}	High-level input current		V _{CC} = MAX, V _I = 2.7V				20	μA
I _{IL}	Low-level input current		V _{CC} = MAX, V _I = 0.4V				-0.1	mA
I _{OZH}	Off-state output current, High-level voltage applied		V _{CC} = MAX, V _I = 2.7V				20	μA
I _{OZL}	Off-state output current, Low-level voltage applied		V _{CC} = MAX, V _I = 0.4V				-20	μA
I _O	Output current ³		V _{CC} = MAX, V _O = 2.25V		-30		-112	mA
I _{CC}	Supply current (total)	I _{CCH}	V _{CC} = MAX			2.5	11	mA
		I _{CCL}				19.5	23	mA
		I _{CCZ}				23	30	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
- The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

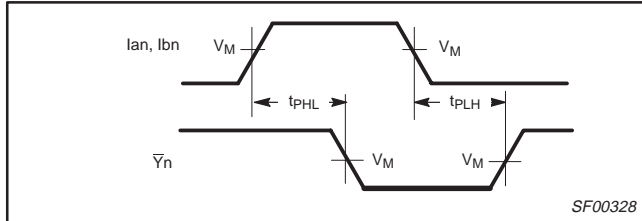
SYMBOL	PARAMETER		TEST CONDITION	LIMITS		UNIT
				T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
				MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay In to Yn		Waveform 1	2.0 2.0	9.0 9.0	ns
t _{PZH} t _{PZL}	Output Enable time to High or Low level		Waveform 2 Waveform 3	2.0 3.0	10.0 12.0	ns
t _{PHZ} t _{PLZ}	Output disable time from High or Low level		Waveform 2 Waveform 3	2.0 3.0	10.0 12.0	ns

Octal inverter buffer (3-State)

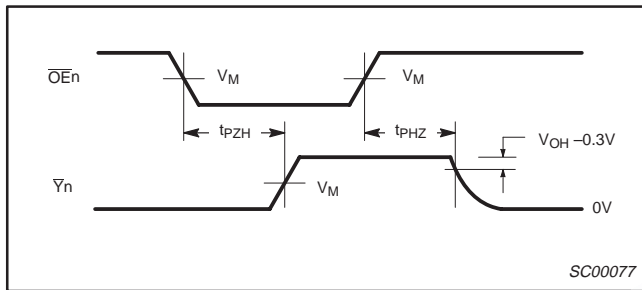
74ALS240A/
74ALS240A-1

AC WAVEFORMS

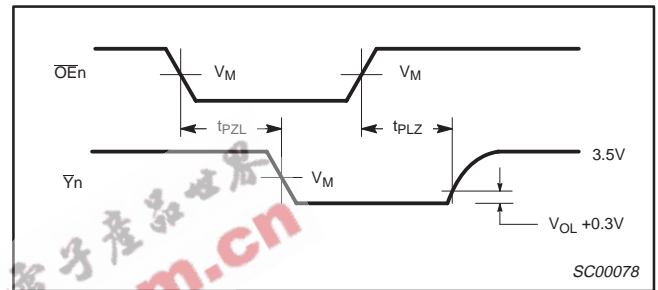
For all waveforms, $V_M = 1.3V$.



Waveform 1. Propagation Delay for Non-Inverting Output



Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS

Test Circuit for 3-State Outputs

SWITCH POSITION	
TEST	SWITCH
t_{pLZ} , t_{pZL}	closed
All other	open

DEFINITIONS:
 R_L = Load resistor; see AC electrical characteristics for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

INPUT PULSE REQUIREMENTS						
Family	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

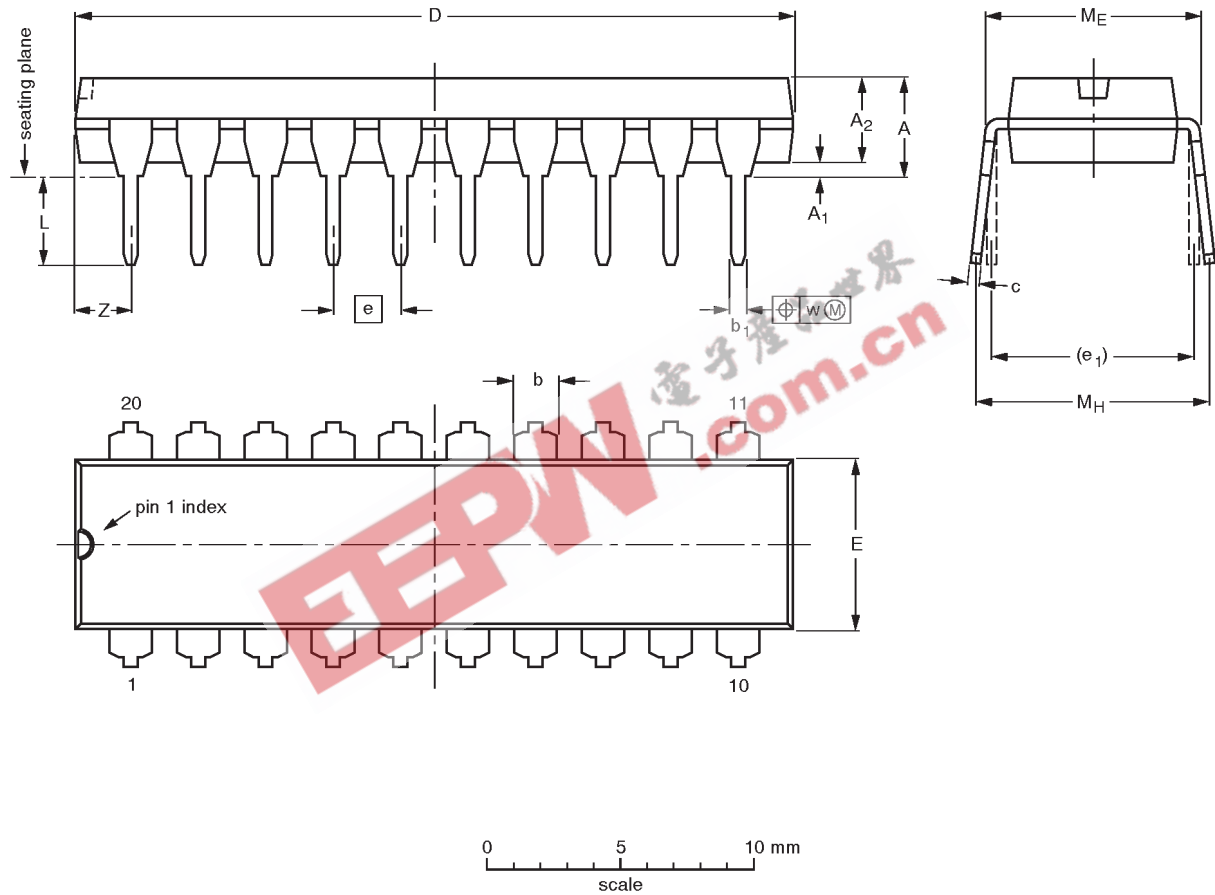
SC00072

Octal inverter buffer (3-State)

74ALS240A/74ALS240A-1

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

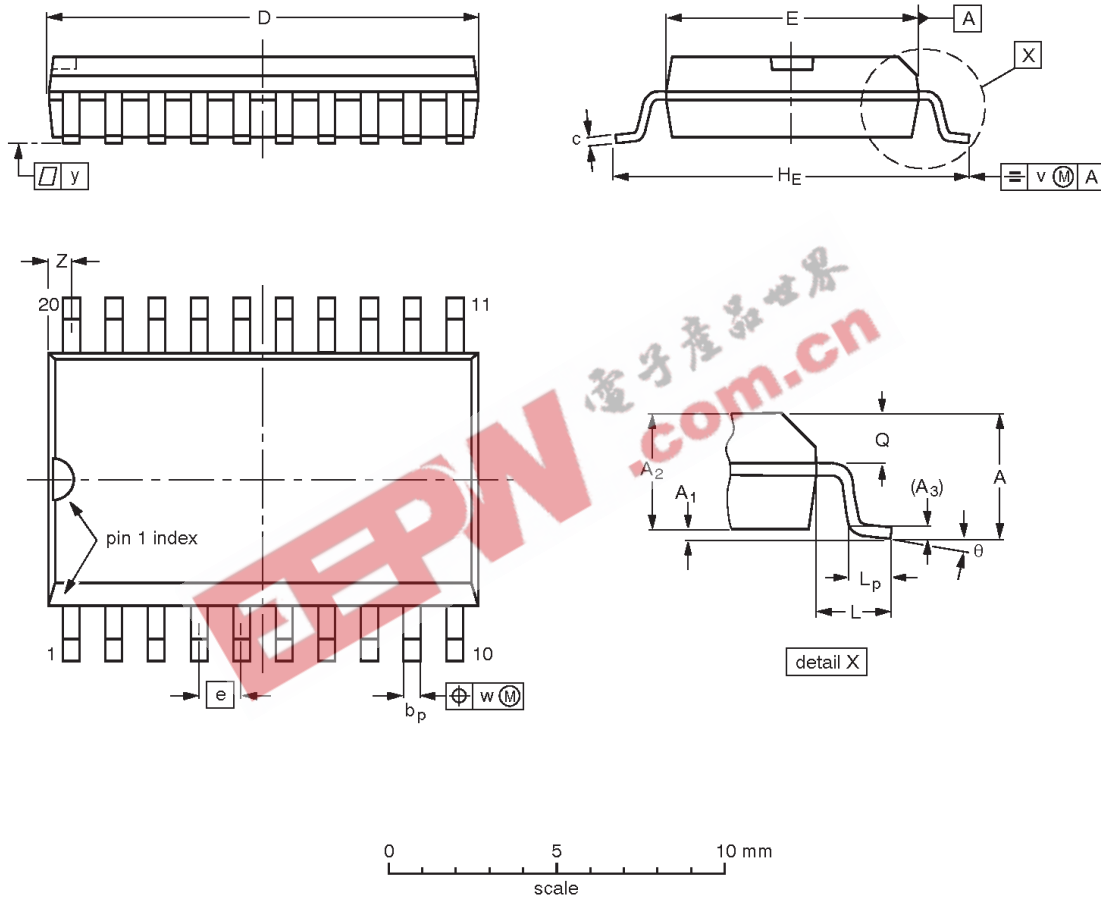
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

Octal inverter buffer (3-State)

74ALS240A/74ALS240A-1

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

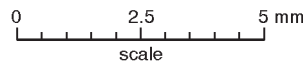
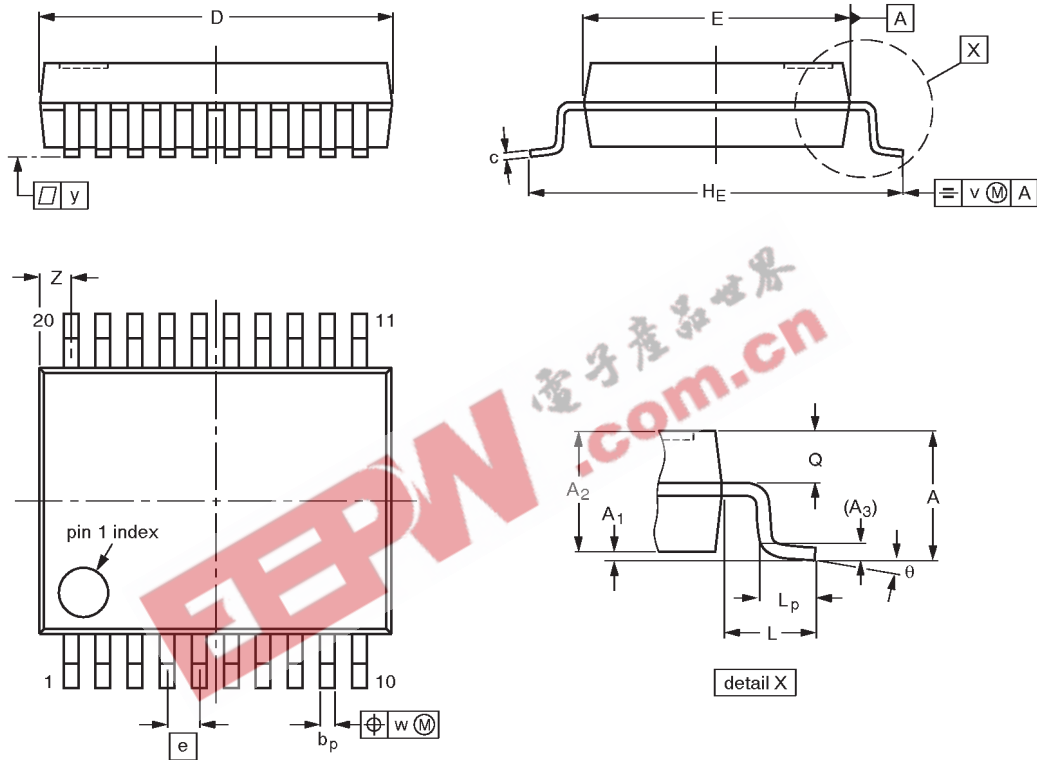
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				92-11-17 95-01-24

Octal inverter buffer (3-State)

74ALS240A/74ALS240A-1

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				93-09-08 95-02-04

Octal inverter buffer (3-State)

74ALS240A/74ALS240A-1

DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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