

April 1988 Revised August 1999

74F534

Octal D-Type Flip-Flop with 3-STATE Outputs

General Description

The 74F534 is a high speed, low-power octal D-type flipflop featuring separate D-type inputs for each flip-flop and 3-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable $(\overline{\text{OE}})$ are common to all flipflops. The 74F534 is the same as the 74F374 except that the outputs are inverted.

Features

- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- 3-STATE outputs for bus-oriented applications

3

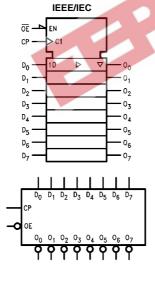
Ordering Code:

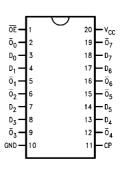
Order Number	Package Number	Package Description
74F534SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F534SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F534PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP) IEDEC MS-001_0 300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols

Connection Diagram





Unit Loading/Fan Out

Pin Names	December 1	U.L.	Input I _{IH} /I _{IL}		
	Description	HIGH/LOW	Output I _{OH} /I _{OL}		
D ₀ –D ₇	Data Inputs	1.0/1.0	20 μA/-0.6 mA		
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/-0.6 mA		
ŌE	3-STATE Output Enable Input (Active LOW)	1.0/1.0	20 μA/-0.6 mA		
$\overline{O}_0 - \overline{O}_7$	Complementary 3-STATE Outputs	150/40(33.3)	-3 mA/24 mA (20 mA)		

Function Table

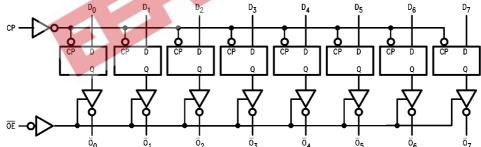
	Inputs		Output
СР	OE	D	ō
~	L	Н	L
~	L	L	Н
L	L	X	\overline{O}_0
X	Н	Χ	Z

H = HIGH Voltage Level

Functional Description

The 74F534 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH clock (CP) transition. With the Output Enable ($\overline{\text{OE}}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{\text{OE}}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{\text{OE}}$ input does not affect the state of the flip-flops.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

L = LOW Voltage Level Z = High Impedance

X = Immaterial Z = I $\sim = LOW-to-HIGH Clock Transition$

 $[\]overline{O}_0$ = Value stored from previous clock cycle

Absolute Maximum Ratings(Note 1)

$_{-65^{\circ}\text{C to}}$ to $_{+150^{\circ}\text{C}}$ Conditions

 $\begin{tabular}{lll} Storage Temperature & -65^{\circ}C to +150^{\circ}C \\ Ambient Temperature under Bias & -55^{\circ}C to +125^{\circ}C \\ \end{tabular}$

Voltage Applied to Output in HIGH State (with $V_{CC} = 0V$)

 $\begin{array}{ll} \text{Standard Output} & -0.5 \text{V to V}_{\text{CC}} \\ \text{3-STATE Output} & -0.5 \text{V to } +5.5 \text{V} \end{array}$

Current Applied to Output

in LOW State (Max) twice the rated I_{OL} (mA) ESD Last Passing Voltage (Min) 4000V

Free Air Ambient Temperature $0^{\circ}\text{C to } +70^{\circ}\text{C}$ Supply Voltage +4.5V to +5.5V

Recommended Operating

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

3

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

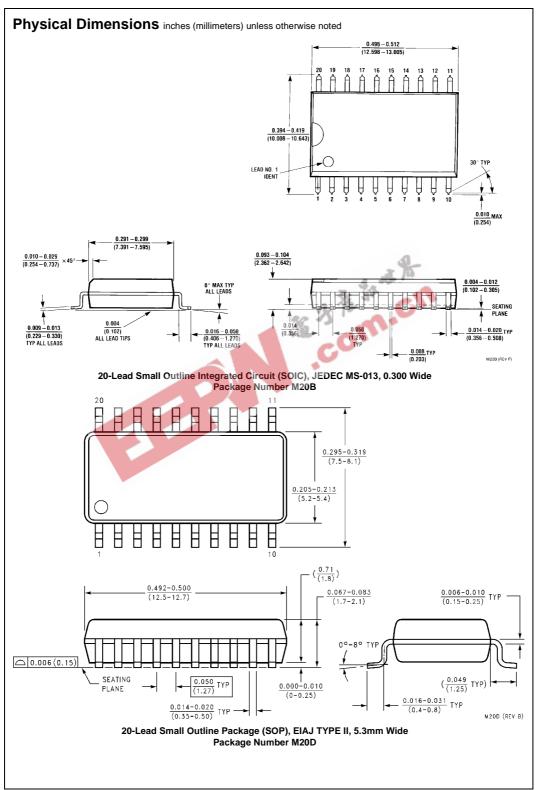
DC Electrical Characteristics

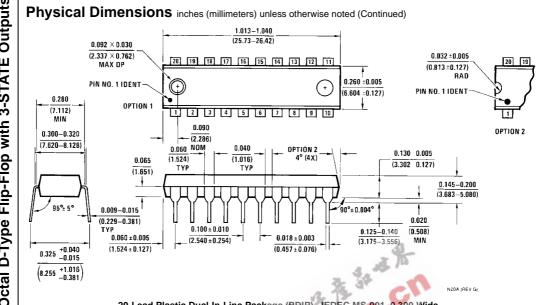
Symbol	Parameter		Min	Тур	Max	Units	V _{CC}	Conditions	
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal	
V _{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal	
V _{CD}	Input Clamp Diode Voltage				=1.2	V	Min	I _{IN} = -18 mA	
V _{OH}	Output HIGH	10% V _{CC}	2.5		137			I _{OH} = -1 mA	
	Voltage	10% V _{CC}	2.4		-	V	Min	$I_{OH} = -3 \text{ mA}$	
		5% V _{CC}	2.7			V	IVIIII	$I_{OH} = -1 \text{ mA}$	
		5% V _{CC}	2.7					$I_{OH} = -3 \text{ mA}$	
V _{OL}	Output LOW Voltage	10% V _{CC}			0.5	V	Min	I _{OL} = 24 mA	
I _{IH}	Input HIGH Current				5.0	μΑ	Max	$V_{IN} = 2.7V$	
I _{BVI}	Input HIGH Current		7.0	μА	Max	V _{IN} = 7.0V			
	Breakdown Test				7.0	μА	IVIAX	V _{IN} = 7.0V	
I _{CEX}	Output HIGH	ut HIGH 50 μA Max				Max	V _{OUT} = V _{CC}		
	Leakage Current				30	μΛ	IVIAX	VOUT - VCC	
V _{ID}	Input Leakage		4.75			V	0.0	$I_{ID} = 1.9 \mu A$	
	Test		4.75			V	0.0	All Other Pins Grounded	
I _{OD}	Output Leakage				3.75	μА	0.0	$V_{IOD} = 1.50 \mu A$	
	Circuit Current				3.73	μΛ	0.0	All Other Pins Grounded	
I _{IL}	Input LOW Current				-0.6	mA	Max	$V_{IN} = 0.5V$	
I _{OZH}	Output Leakage Current				50	μΑ	Max	V _{OUT} = 2.7V	
I _{OZL}	Output Leakage Current				-50	μΑ	Max	V _{OUT} = 0.5V	
Ios	Output Short-Circuit Cur	rent	-60		-150	mA	Max	V _{OUT} = 0V	
I _{ZZ}	Bus Drainage Test				500	μΑ	0.0V	V _{OUT} = 5.25V	
I _{CCZ}	Power Supply Current			55	86	mA	Max	V _O = HIGH Z	

Symbol	Parameter	$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$			$T_A = -55$ °C to +125°C $V_{CC} = +5.0V$		$T_A = 0$ °C to +70°C $V_{CC} = +5.0V$		Units
			$C_L = 50 \text{ pF}$		$C_L = 50 pF$		$C_L = 50 \text{ pF}$		01111
		Min	Тур	Max	Min	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	100			60		70		N
t _{PLH}	Propagation Delay	4.0	6.5	8.5	4.0	10.5	4.0	10.0	
t_{PHL}	CP to \overline{O}_n	4.0	6.5	8.5	4.0	11.0	4.0	10.0	ns
t _{PZH}	Output Enable Time	2.0	9.0	11.5	2.0	14.0	2.0	12.5	
t_{PZL}		2.0	5.8	7.5	2.0	10.0	2.0	8.5	1 .
t _{PHZ}	Output Disable Time	1.5	5.3	7.0	1.5	8.0	1.5	8.0	
t _{PLZ}		1.5	4.3	5.5	1.5	7.5	1.5	6.5	

AC Operating Requirements

		T _A =	= +25°C	$T_A = -55^{\circ}C$	to +125°C	T _A = 0°C	to +70°C	
Symbol	Symbol Parameter		$V_{CC} = +5.0V$		$V_{CC} = +5.0 \text{V}$		$V_{CC} = +5.0V$	
		Min	Max	Min	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	2.0		2.0	T In	2.0		
$t_S(L)$	D _n to CP	2.0		2.5		2.0		ns
t _H (H)	Hold Time, HIGH or LOW	2.0	./9	2.0		2.0		115
t _H (L)	D _n to CP	2.0	20 %	2.5		2.0		
t _W (H)	CP Pulse Width	7.0	100	7.0	100	7.0		ns
$t_W(L)$	HIGH or LOW	6.0	1 440	6.0		6.0		115





20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N20A

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