

# DATA SHEET

**74LVC162244A; 74LVCH162244A**  
16-bit buffer/line driver, 30  $\Omega$  series  
termination resistors; 5 V tolerant  
input/output; 3-state

Product specification  
Supersedes data of 1998 Feb 17

2003 Dec 12

# 16-bit buffer/line driver, 30 $\Omega$ series termination resistors; 5 V tolerant input/output; 3-state

## 74LVC162244A; 74LVCH162244A

### FEATURES

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 to 3.6 V
- CMOS low power consumption
- MULTIBYTE flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- Integrated 30  $\Omega$  termination resistors
- All data inputs have bushold (74LVCH162244A only)
- Complies with JEDEC standard no. 8-1A
- ESD protection:  
HBM EIA/JESD22-A114-A exceeds 2000 V  
MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from  $-40$  to  $+85$   $^{\circ}\text{C}$  and  $-40$  to  $+125$   $^{\circ}\text{C}$ .

### DESCRIPTION

The 74LVC(H)162244A is a high-performance, low power, low voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3 or 5 V devices. In 3-state operation, outputs can handle 5 V. These features allow the use of these devices as a mixed 3.3 and 5 V environment.

The 74LVC(H)162244A is a 16-bit non-inverting buffer/line driver with 3-state outputs. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer. The 3-state outputs are controlled by the output enable inputs  $1\text{OE}$ ,  $2\text{OE}$ ,  $3\text{OE}$  and  $4\text{OE}$ . A HIGH on  $n\text{OE}$  causes the outputs to assume a high-impedance OFF-state.

The 74LVCH162244A bushold data inputs eliminates the need for external termination resistors to hold unused inputs.

The 74LVC(H)162244A is designed with 30  $\Omega$  series termination resistors in both HIGH and LOW output stages to reduce line noise.

### QUICK REFERENCE DATA

GND = 0 V;  $T_{\text{amb}} = 25$   $^{\circ}\text{C}$ ;  $t_r = t_f \leq 2.5$  ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{\text{PHL}}/t_{\text{PLH}}$	propagation delay nAn to nYn	$C_L = 50$ pF; $V_{\text{CC}} = 3.3$ V	3.0	ns
$t_{\text{PZH}}/t_{\text{PZL}}$	3-state output enable time $n\text{OE}$ to nYn	$C_L = 50$ pF; $V_{\text{CC}} = 3.3$ V	3.5	ns
$t_{\text{PHZ}}/t_{\text{PLZ}}$	3-state output disable time $n\text{OE}$ to nYn	$C_L = 50$ pF; $V_{\text{CC}} = 3.3$ V	2.8	ns
$C_I$	input capacitance		5.0	pF
$C_{\text{PD}}$	power dissipation capacitance per gate	$V_{\text{CC}} = 3.3$ V; notes 1 and 2 outputs enabled outputs disabled	12 4.0	pF pF

### Notes

1.  $C_{\text{PD}}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{\text{PD}} \times V_{\text{CC}}^2 \times f_i \times N + \Sigma(C_L \times V_{\text{CC}}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{\text{CC}}$  = supply voltage in Volts;

$N$  = total load switching outputs;

$\Sigma(C_L \times V_{\text{CC}}^2 \times f_o)$  = sum of the outputs.

2. The condition is  $V_I = \text{GND to } V_{\text{CC}}$ .

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#### ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC162244ADL	-40 to +125 °C	48	SSOP48	plastic	SOT370-1
74LVCH162244ADL	-40 to +125 °C	48	SSOP48	plastic	SOT370-1
74LVC162244ADGG	-40 to +125 °C	48	TSSOP48	plastic	SOT362-1
74LVCH162244ADGG	-40 to +125 °C	48	TSSOP48	plastic	SOT362-1

#### FUNCTION TABLE

See note 1.

INPUT		OUTPUT
nOE	nAn	nYn
L	L	L
L	H	H
H	X	Z

#### Note

1. H = HIGH voltage level;  
L = LOW voltage level;  
X = don't care;  
Z = high-impedance OFF-state.

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PINNING

PIN	SYMBOL	DESCRIPTION
1	1OE	output enable input (active LOW)
2	1Y0	data output
3	1Y1	data output
4	GND	ground (0 V)
5	1Y2	data output
6	1Y3	data output
7	V <sub>CC</sub>	supply voltage
8	2Y0	data output
9	2Y1	data output
10	GND	ground (0 V)
11	2Y2	data output
12	2Y3	data output
13	3Y0	data output
14	3Y1	data output
15	GND	ground (0 V)
16	3Y2	data output
17	3Y3	data output
18	V <sub>CC</sub>	supply voltage
19	4Y0	data output
20	4Y1	data output
21	GND	ground (0 V)
22	4Y2	data output
23	4Y3	data output
24	4OE	output enable input (active LOW)
25	3OE	output enable input (active LOW)
26	4A3	data input
27	4A2	data input
28	GND	ground (0 V)
29	4A1	data input
30	4A0	data input
31	V <sub>CC</sub>	supply voltage
32	3A3	data input
33	3A2	data input
34	GND	ground (0 V)
35	3A1	data input
36	3A0	data input
37	2A3	data input

PIN	SYMBOL	DESCRIPTION
38	2A2	data input
39	GND	ground (0 V)
40	2A1	data input
41	2A0	data input
42	V <sub>CC</sub>	supply voltage
43	1A3	data input
44	1A2	data input
45	GND	ground (0 V)
46	1A1	data input
47	1A0	data input
48	2OE	output enable input (active LOW)

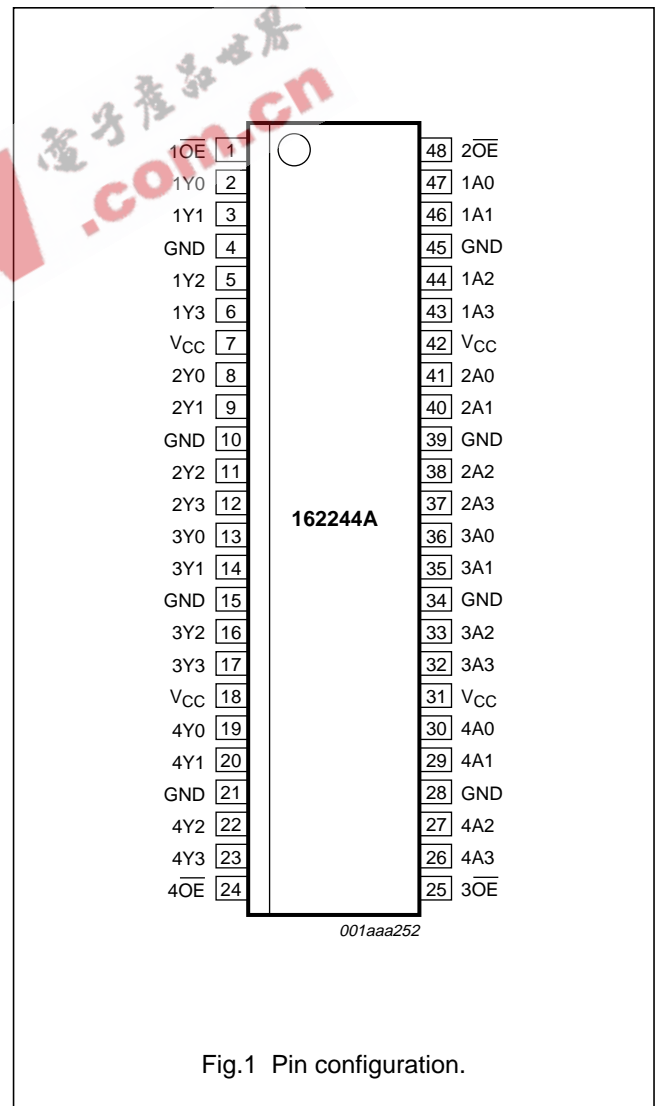
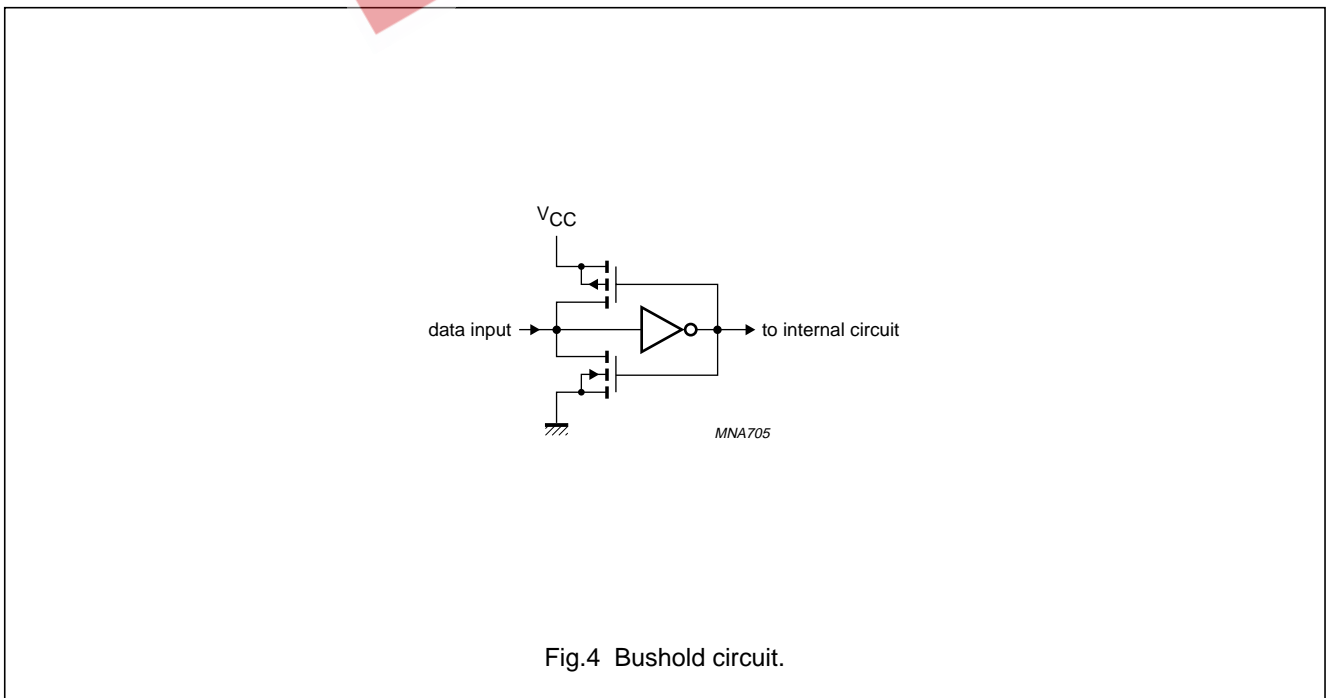
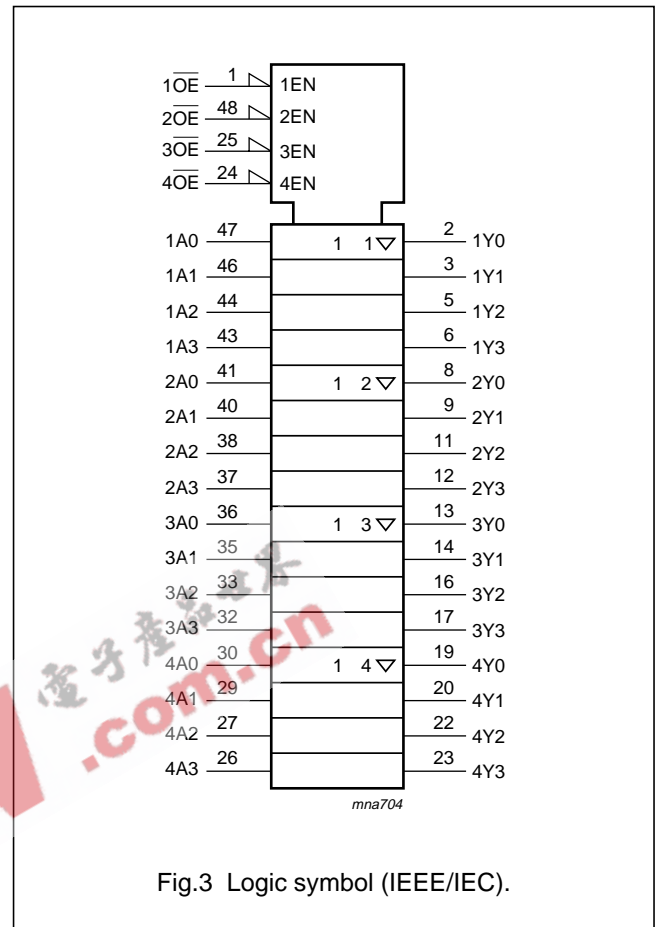
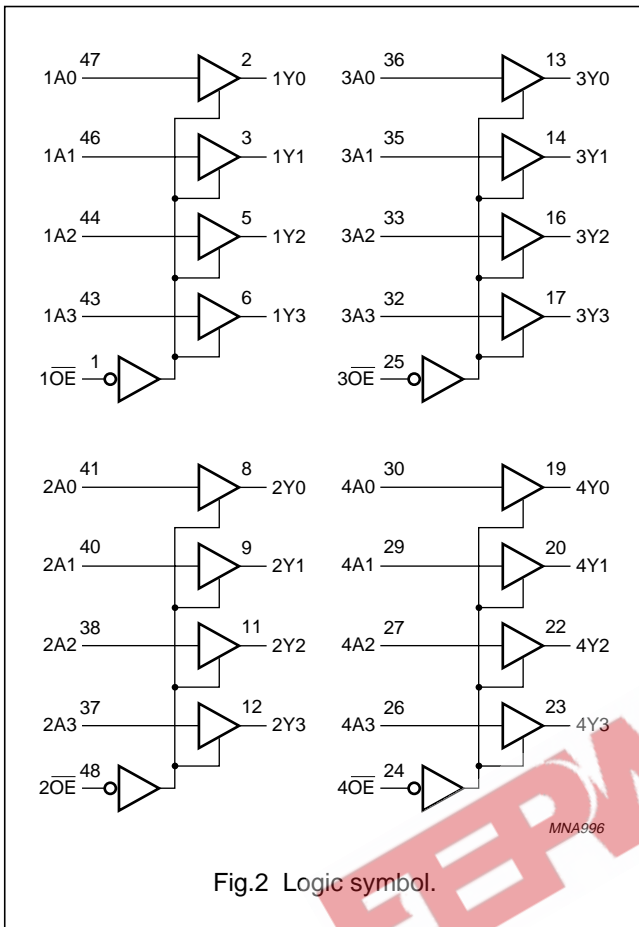


Fig.1 Pin configuration.

16-bit buffer/line driver, 30 Ω series termination resistors; 5 V tolerant input/output; 3-state

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#### RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage	for maximum speed performance	2.7	3.6	V
		for low voltage applications	1.2	3.6	V
V <sub>I</sub>	input voltage		0	5.5	V
V <sub>O</sub>	output voltage	output HIGH or LOW state	0	V <sub>CC</sub>	V
		output 3-state	0	5.5	V
T <sub>amb</sub>	operating ambient temperature	in free air	-40	+125	°C
t <sub>r</sub> , t <sub>f</sub>	input rise and fall times	V <sub>CC</sub> = 1.2 to 2.7 V	0	20	ns/V
		V <sub>CC</sub> = 2.7 to 3.6 V	0	10	ns/V

#### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage		-0.5	+6.5	V
I <sub>IK</sub>	input diode current	V <sub>I</sub> < 0		-50	mA
V <sub>I</sub>	input voltage	note 1	-0.5	+6.5	V
I <sub>OK</sub>	output diode current	V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0	-	±50	mA
V <sub>O</sub>	output voltage	output HIGH or LOW state; note 1	-0.5	V <sub>CC</sub> + 0.5	V
		output 3-state; note 1	-0.5	+6.5	V
I <sub>O</sub>	output source or sink current	V <sub>O</sub> = 0 to V <sub>CC</sub>	-	±50	mA
I <sub>CC</sub> , I <sub>GND</sub>	V <sub>CC</sub> or GND current		-	±100	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	power dissipation	T <sub>amb</sub> = -40 to +125 °C; note 2	-	500	mW

#### Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 60 °C the value of P<sub>tot</sub> derates linearly with 5.5 mW/K.

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### DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C; note 1</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.2	V <sub>CC</sub>	–	–	V
			2.7 to 3.6	2.0	–	–	V
V <sub>IL</sub>	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -100 $\mu$ A I <sub>O</sub> = -6 mA I <sub>O</sub> = -12 mA	2.7 to 3.6	V <sub>CC</sub> - 0.2	V <sub>CC</sub> <sup>(2)</sup>	–	V
			2.7	V <sub>CC</sub> - 0.5	–	–	V
			3.0	V <sub>CC</sub> - 0.8	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 100 $\mu$ A I <sub>O</sub> = 6 mA I <sub>O</sub> = 12 mA	2.7 to 3.6	–	GND <sup>(2)</sup>	0.20	V
			2.7	–	–	0.40	V
			3.0	–	–	0.55	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; note 3	3.6	–	$\pm$ 0.1	$\pm$ 5	$\mu$ A
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND; note 3	3.6	–	$\pm$ 0.1	$\pm$ 5	$\mu$ A
I <sub>off</sub>	power off leakage supply current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0.0	–	$\pm$ 0.1	$\pm$ 10	$\mu$ A
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	3.6	–	0.1	20	$\mu$ A
$\Delta$ I <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0	2.7 to 3.6	–	5 <sup>(2)</sup>	500	$\mu$ A
I <sub>BHL</sub>	bushold LOW sustaining current	V <sub>I</sub> = 0.8 V; notes 4 and 5	3.0	75	–	–	$\mu$ A
I <sub>BHH</sub>	bushold HIGH sustaining current	V <sub>I</sub> = 2.0 V; notes 4 and 5	3.0	-75	–	–	$\mu$ A
I <sub>BHLO</sub>	bushold LOW overdrive current	notes 4 and 6	3.6	500	–	–	$\mu$ A
I <sub>BHNO</sub>	bushold HIGH overdrive current	notes 4 and 6	3.6	-500	–	–	$\mu$ A

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.2	V <sub>CC</sub>	–	–	V
			2.7 to 3.6	2.0	–	–	V
V <sub>IL</sub>	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -100 $\mu$ A I <sub>O</sub> = -6 mA I <sub>O</sub> = -12 mA	2.7 to 3.6	V <sub>CC</sub> - 0.3	–	–	V
			2.7	V <sub>CC</sub> - 0.65	–	–	V
			3.0	V <sub>CC</sub> - 1	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 100 $\mu$ A I <sub>O</sub> = 6 mA I <sub>O</sub> = 12 mA	2.7 to 3.6	–	–	0.3	V
			2.7	–	–	0.6	V
			3.0	–	–	0.8	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; note 3	3.6	–	–	$\pm$ 20	$\mu$ A
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND; note 3	3.6	–	–	$\pm$ 20	$\mu$ A
I <sub>off</sub>	power off leakage supply current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0.0	–	–	$\pm$ 20	$\mu$ A
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	3.6	–	–	80	$\mu$ A
$\Delta$ I <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0	2.7 to 3.6	–	–	5000	$\mu$ A
I <sub>BHL</sub>	bushold LOW sustaining current	V <sub>I</sub> = 0.8 V; notes 4 and 5	3.0	60	–	–	$\mu$ A
I <sub>BHH</sub>	bushold HIGH sustaining current	V <sub>I</sub> = 2.0 V; notes 4 and 5	3.0	-60	–	–	$\mu$ A
I <sub>BHLO</sub>	bushold LOW overdrive current	notes 4 and 6	3.6	500	–	–	$\mu$ A
I <sub>BHHO</sub>	bushold HIGH overdrive current	notes 4 and 6	3.6	-500	–	–	$\mu$ A

#### Notes

1. All typical values are measured T<sub>amb</sub> = 25 °C.
2. Value is measured at V<sub>CC</sub> = 3.3 V.
3. For bushold parts, the bushold circuit is switched off when V<sub>I</sub> > V<sub>CC</sub> allowing 5.5 V on the input terminal.
4. Valid for data inputs of bushold parts (LVCH162244A) only. For data inputs only, control inputs do not have a bushold circuit.
5. The specified sustaining current at the data input holds the input below the specified V<sub>I</sub> level.
6. The specified overdrive current at the data input forces the data input to the opposite logic input state.



16-bit buffer/line driver, 30  $\Omega$  series termination resistors; 5 V tolerant input/output; 3-state

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### AC CHARACTERISTICS

GND = 0 V;  $t_r = t_f \leq 2.5$  ns;  $C_L = 50$  pF;  $R_L = 500$   $\Omega$ .

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C; note1</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nAn to nYn	see Figs 5 and 7	1.2	–	11.0	–	ns
			2.7	1.0	–	6.7	ns
			3.0 to 3.6	1.0	3.0 <sup>(2)</sup>	5.8	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time n $\overline{OE}$ to nYn	see Figs 6 and 7	1.2	–	15.0	–	ns
			2.7	1.5	–	7.6	ns
			3.0 to 3.6	1.0	3.5 <sup>(2)</sup>	6.0	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time n $\overline{OE}$ to nYn	see Figs 6 and 7	1.2	–	10.0	–	ns
			2.7	1.5	–	4.7	ns
			3.0 to 3.6	1.5	2.8 <sup>(2)</sup>	4.5	ns
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nAn to nYn	see Figs 5 and 7	1.2	–	–	–	ns
			2.7	1.0	–	8.5	ns
			3.0 to 3.6	1.0	–	7.5	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time n $\overline{OE}$ to nYn	see Figs 6 and 7	1.2	–	–	–	ns
			2.7	1.5	–	9.5	ns
			3.0 to 3.6	1.0	–	7.5	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time n $\overline{OE}$ to nYn	see Figs 6 and 7	1.2	–	–	–	ns
			2.7	1.5	–	6.0	ns
			3.0 to 3.6	1.5	–	6.0	ns

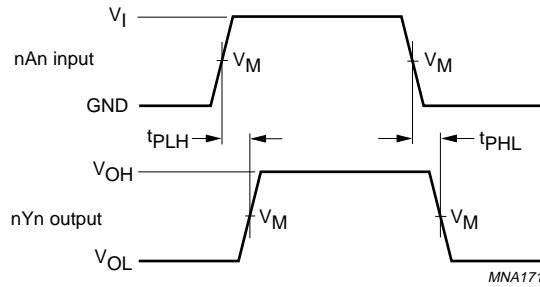
### Notes

1. All typical values are measured at T<sub>amb</sub> = 25 °C.
2. Value is measured at V<sub>CC</sub> = 3.3 V.

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AC WAVEFORMS



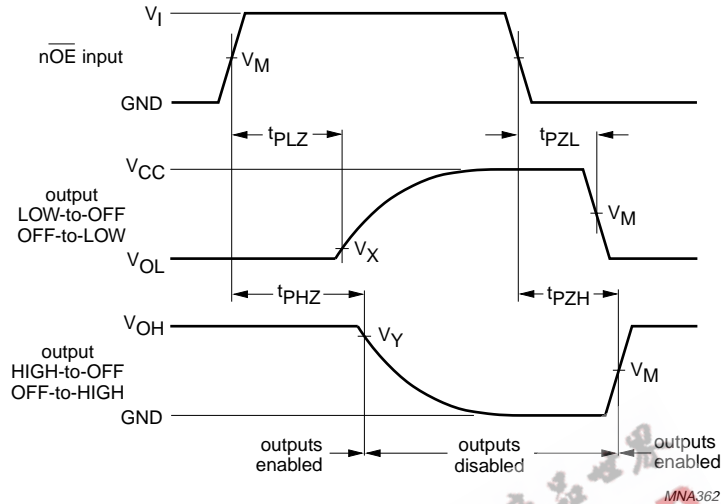
V <sub>CC</sub>	V <sub>M</sub>	INPUT	
		V <sub>I</sub>	t <sub>r</sub> = t <sub>f</sub>
1.2 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	≤ 2.5 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

Fig.5 The input nAn to output nYn propagation delays.

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V <sub>CC</sub>	V <sub>M</sub>	INPUT	
		V <sub>I</sub>	t <sub>r</sub> = t <sub>f</sub>
1.2 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	≤ 2.5 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns

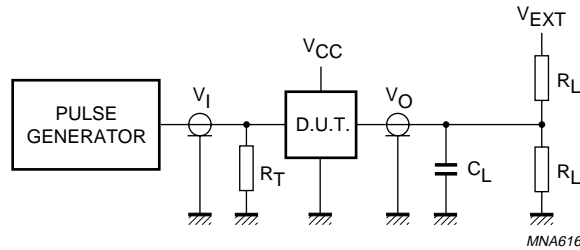
$V_X = V_{OL} + 0.3 \text{ V}$  at  $V_{CC} \geq 2.7 \text{ V}$ ;  
 $V_X = V_{OL} + 0.1 \text{ V}$  at  $V_{CC} < 2.7 \text{ V}$ ;  
 $V_Y = V_{OH} - 0.3 \text{ V}$  at  $V_{CC} \geq 2.7 \text{ V}$ ;  
 $V_Y = V_{OH} - 0.1 \text{ V}$  at  $V_{CC} < 2.7 \text{ V}$ .

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

Fig.6 3-state enable and disable times.

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V <sub>CC</sub>	V <sub>I</sub>	C <sub>L</sub>	R <sub>L</sub>	V <sub>EXT</sub>		
				t <sub>PLH</sub> /t <sub>PHL</sub>	t <sub>PZH</sub> /t <sub>PHZ</sub>	t <sub>PZL</sub> /t <sub>PLZ</sub>
1.2 V	V <sub>CC</sub>	50 pF	500 Ω <sup>(1)</sup>	open	GND	2 × V <sub>CC</sub>
2.7 V	2.7 V	50 pF	500 Ω	open	GND	2 × V <sub>CC</sub>
3.0 to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	2 × V <sub>CC</sub>

**Note**

1. The circuit performs better when R<sub>L</sub> = 1000 Ω.

Definitions for test circuits:

R<sub>L</sub> = Load resistor.

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

R<sub>T</sub> = Termination resistance should be equal to the output impedance Z<sub>o</sub> of the pulse generator.

Fig.7 Load circuitry for switching times.

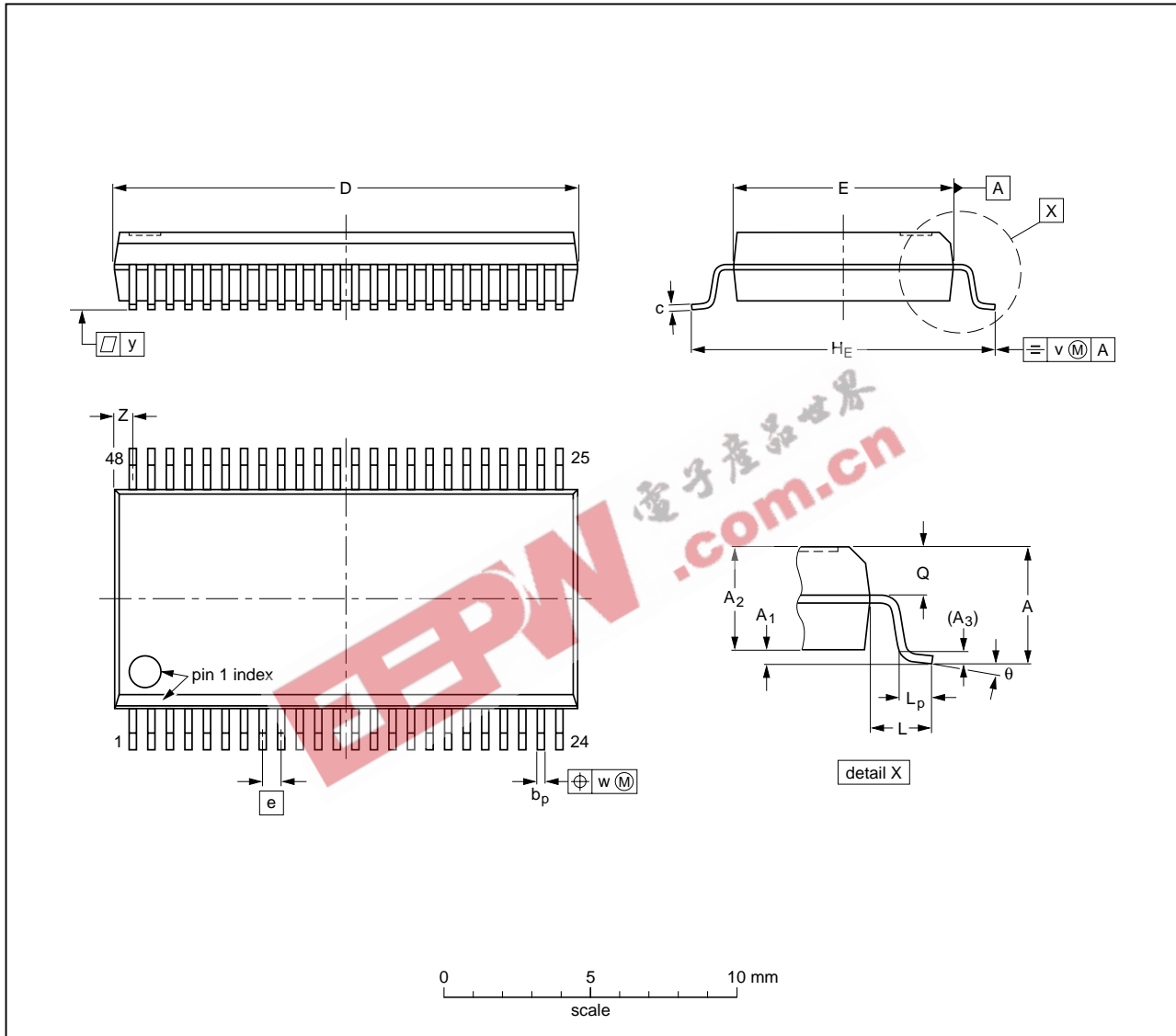
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PACKAGE OUTLINES

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note  
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

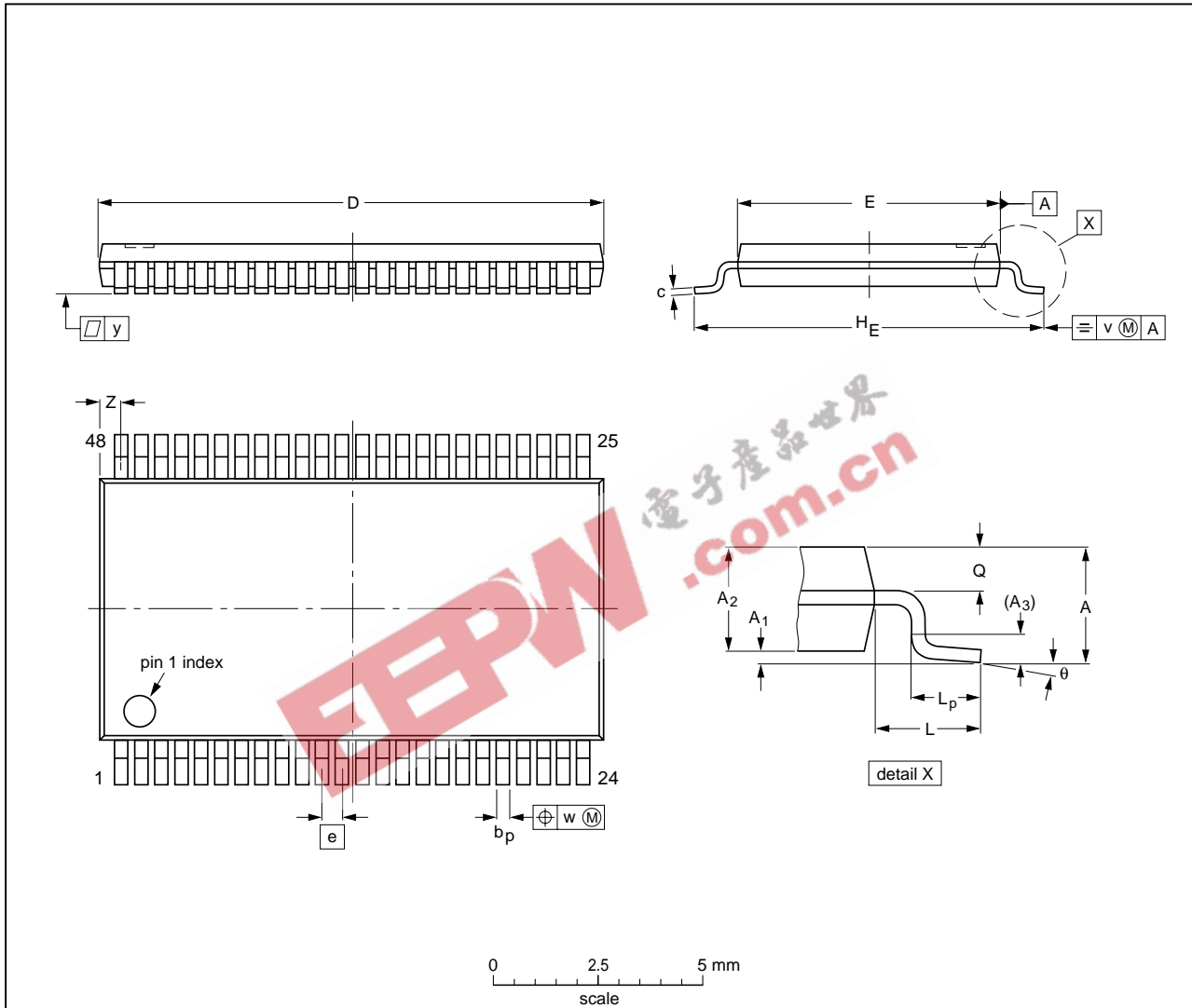
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT370-1		MO-118			99-12-27 03-02-19

16-bit buffer/line driver, 30 Ω series termination resistors; 5 V tolerant input/output; 3-state

74LVC162244A;  
74LVCH162244A

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1



**DIMENSIONS** (mm are the original dimensions).

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT362-1		MO-153			99-12-27 03-02-19

16-bit buffer/line driver, 30  $\Omega$  series termination resistors; 5 V tolerant input/output; 3-state

74LVC162244A;  
74LVCH162244A

#### DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

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1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

#### DEFINITIONS

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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