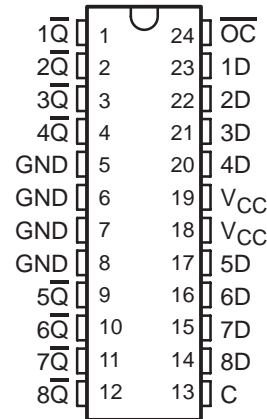


54AC11533, 74AC11533 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SCAS004 – D2957, JULY 1987 – REVISED APRIL 1993

- 8-Latches in a Single Package
- 3-State Bus-Driving Inverting Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

54AC11533 . . . JT PACKAGE
74AC11533 . . . DW OR NT PACKAGE
(TOP VIEW)



description

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

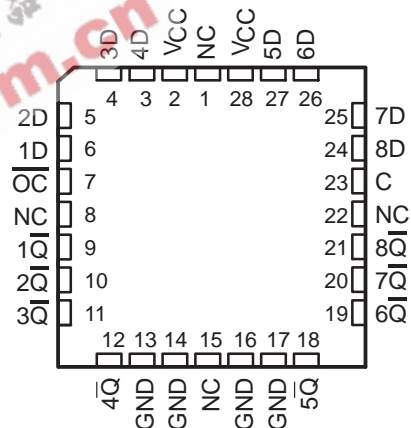
The eight latches of the 'AC11533 are transparent D-type latches. While the enable (C) is high, the \bar{Q} outputs will follow the complements of the (D) inputs. When the output control \bar{OC} is taken low, the \bar{Q} outputs will be latched. The 'AC11533 is functionally equivalent to the 'AC11373 except for having inverted outputs.

A buffered output-control (\bar{OC}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control (\bar{OC}) does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The 54AC11533 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74AC11533 is characterized for operation from -40°C to 85°C .

54AC11533 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

EPIC is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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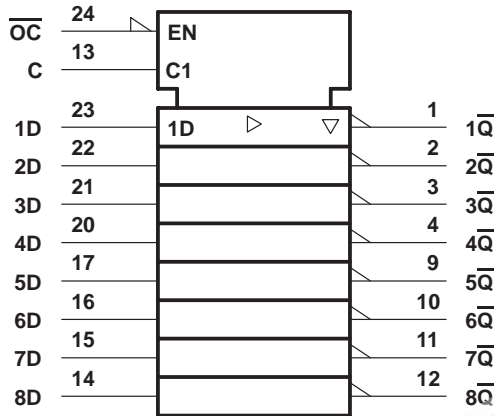
54AC11533, 74AC11533 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

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FUNCTION TABLE
(each latch)

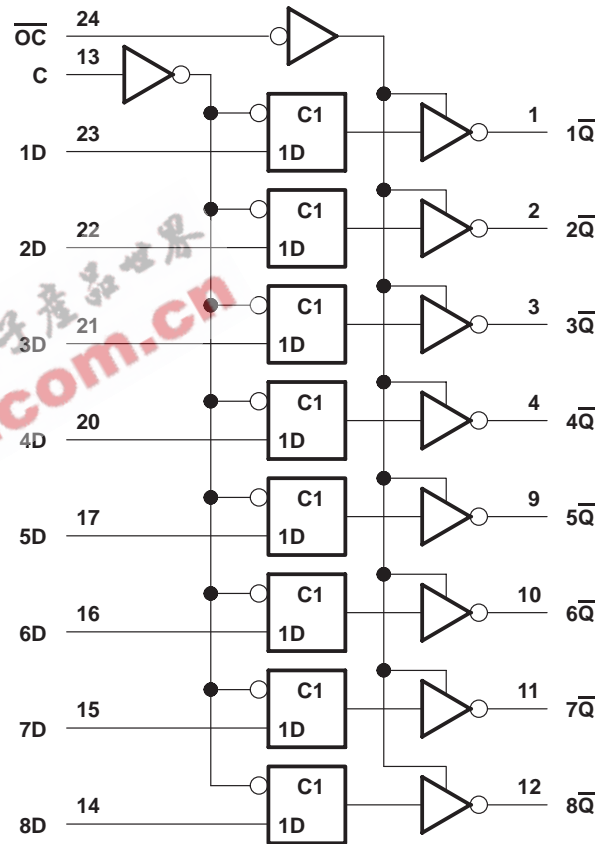
INPUTS			OUTPUT
\overline{OC}	C	D	Q
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q_0}$
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 6 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 200 mA
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

54AC11533, 74AC11533 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

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recommended operating conditions

		54AC11533			74AC11533			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	3	5	5.5	3	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 3 V		2.1	2.1		V	
		V _{CC} = 4.5 V		3.15	3.15			
		V _{CC} = 5.5 V		3.85	3.85			
V _{IL}	Low-level input voltage	V _{CC} = 3 V			0.9		V	
		V _{CC} = 4.5 V			1.35			
		V _{CC} = 5.5 V			1.65			
V _I	Input voltage	0		V _{CC}	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	0		V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 3 V			-4		mA	
		V _{CC} = 4.5 V			-24			
		V _{CC} = 5.5 V			-24			
I _{OL}	Low-level output current	V _{CC} = 3 V			12		mA	
		V _{CC} = 4.5 V			24			
		V _{CC} = 5.5 V			24			
Δt/Δv	Input transition rise or fall rate	0		10	0		10	ns/V
T _A	Operating free-air temperature	-55		125	-40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC11533		74AC11533		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	3 V	2.9			2.9		2.9	V	
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
	I _{OH} = -24 mA	5.5 V	4.94			4.7		4.8		
		5.5 V				3.85				
V _{OL}	I _{OL} = 50 μA	3 V				0.1		0.1	V	
		4.5 V				0.1		0.1		
		5.5 V				0.1		0.1		
	I _{OL} = 12 mA	3 V				0.36		0.44		
		4.5 V				0.36		0.44		
	I _{OL} = 24 mA	5.5 V				0.36		0.44		
		5.5 V					1.65			
I _{OL} = 75 mA†	5.5 V						1.65			
	5.5 V						1.65			
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.5		±10	±5	μA	
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1	±1	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160	80	μA	
C _i	V _I = V _{CC} or GND	5 V			4				pF	
C _o	V _O = V _{CC} or GND	5 V			10				pF	

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.



54AC11533, 74AC11533 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

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timing requirements (see Figure 1)

	V _{CC} RANGE	T _A = 25°C		54AC11533		74AC11533		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w Pulse duration, C high	3.3 ± 0.3 V	5.5		5.5		5.5		ns
	5 ± 0.5 V	4		4		4		
t _{su} Setup time, data before C	3.3 ± 0.3 V	4		4		4		ns
	5 ± 0.5 V	3.5		3.5		3.5		
t _h Hold time, data after C↓	3.3 ± 0.3 V	2		2		2		ns
	5 ± 0.5 V	2		2		2		

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			54AC11533		74AC11533		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	D	Q̄	1.5	8.5	12.6	1.5	15.2	1.5	14.3	ns
t _{PHL}			1.5	7.5	10.1	1.5	12	1.5	11.3	
t _{PLH}	C	Any Q̄	1.5	10	14.5	1.5	17.6	1.5	16.5	ns
t _{PHL}			1.5	9.5	12.8	1.5	15.2	1.5	14.3	
t _{PZH}	OC̄	Any Q̄	1.5	9	13.1	1.5	15.7	1.5	14.7	ns
t _{PZL}			1.5	8.5	11.6	1.5	14.1	1.5	13.1	
t _{PHZ}	OC̄	Any Q̄	1.5	9.5	12	1.5	13.2	1.5	12.8	ns
t _{PLZ}			1.5	7.5	10.2	1.5	11.4	1.5	11	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			54AC11533		74AC11533		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	D	Q̄	1.5	5.5	8.4	1.5	10.6	1.5	9.8	ns
t _{PHL}			1.5	5	7.1	1.5	8.6	1.5	8	
t _{PLH}	C	Any Q̄	1.5	6.5	10	1.5	12.1	1.5	11.3	ns
t _{PHL}			1.5	6.5	9.1	1.5	11	1.5	10.3	
t _{PZH}	OC̄	Any Q̄	1.5	6.5	9.5	1.5	11.7	1.5	10.8	ns
t _{PZL}			1.5	6	8.6	1.5	10.9	1.5	9.7	
t _{PHZ}	OC̄	Any Q̄	1.5	8.5	10.7	1.5	11.7	1.5	11.4	ns
t _{PLZ}			1.5	6	8.2	1.5	9.3	1.5	8.9	

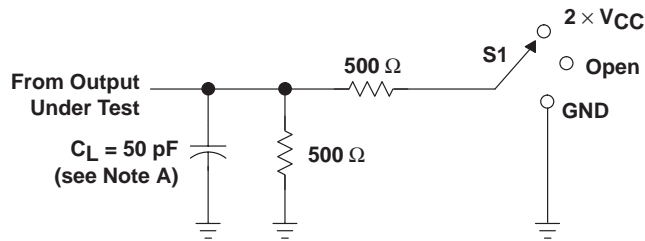
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per latch	C _L = 50 pF, f = 1 MHz	55	pF
			44	

54AC11533, 74AC11533 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

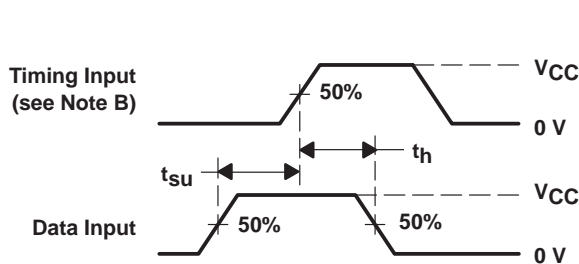
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PARAMETER MEASUREMENT INFORMATION

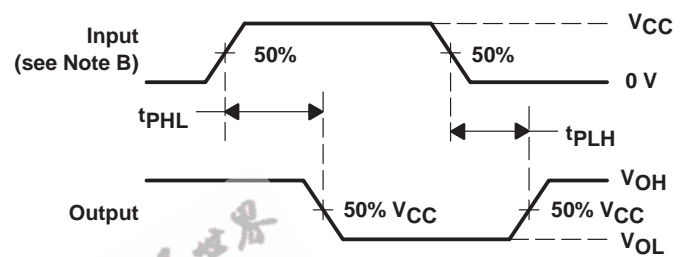


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

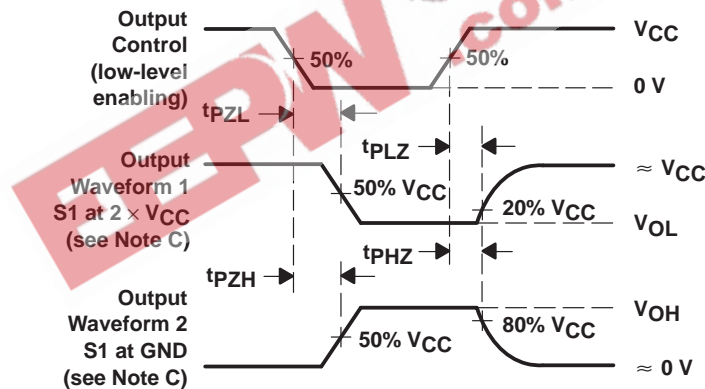
LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r = 3$ ns, $t_f = 3$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74AC11533DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
74AC11533NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI
74AC11533NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI
74AC11533NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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