

DATA SHEET

74ABT16899

74ABTH16899

18-bit latched transceiver with 16-bit
parity generator/checker (3-State)

Product specification
Supersedes data of 1997 Mar 28
IC23 Data Handbook

1998 Feb 25

18-bit latched transceiver with 16-bit parity generator/checker (3-State)

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FEATURES

- Symmetrical (A and B bus functions are identical)
- Selectable generate parity or "feed-through" parity for A-to-B and B-to-A directions
- Independent transparent latches for A-to-B and B-to-A directions
- Selectable ODD/EVEN parity
- Continuously checks parity of both A bus and B bus latches as \overline{ERRA} and \overline{ERRB}
- Open-collector \overline{ERR} output
- Ability to simultaneously generate and check parity
- Can simultaneously read/latch A and B bus data
- Output capability: +64 mA/−32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power up 3-State
- Power-up reset
- Live insertion/extraction permitted
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs

DESCRIPTION

The 74ABT/H16899 is a 16-bit to 16-bit parity transceiver with separate transparent latches for the A bus and B bus. Either bus can generate or check parity. The parity bit can be fed-through with no change or the generated parity can be substituted with the SEL input.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	$C_L = 50\text{pF}; V_{CC} = 5\text{V}$	2.7	ns
t_{PLH} t_{PHL}	Propagation delay An to \overline{ERRA}	$C_L = 50\text{pF}; V_{CC} = 5\text{V}$	5.0	ns
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}	4	pF
$C_{I/O}$	Output capacitance	Outputs disabled; $V_O = 0\text{V}$ or V_{CC}	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; $V_{CC} = 5.5\text{V}$	500	μA
I_{CCL}		Output Low; $V_{CC} = 5.5\text{V}$	10.5	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	−40°C to +85°C	74ABT16899 DL	BT16899 DL	SOT371-1
56-Pin Plastic TSSOP Type II	−40°C to +85°C	74ABT16899 DGG	BT16899 DGG	SOT364-1
56-Pin Plastic SSOP Type III	−40°C to +85°C	74ABTH16899 DL	BH16899 DL	SOT371-1
56-Pin Plastic TSSOP Type II	−40°C to +85°C	74ABTH16899 DGG	BH16899 DGG	SOT364-1

Parity error checking of the A and B bus latches is continuously provided with \overline{ERRA} and \overline{ERRB} , even with both buses in 3-State.

The 74ABT/H16899 features independent latch enables for the A and B bus latches, a select pin for ODD/EVEN parity, and separate error signal output pins for checking parity.

FUNCTIONAL DESCRIPTION

The 74ABT/H16899 has three principal modes of operation which are outlined below. All modes apply to both the A-to-B and B-to-A directions.

Transparent latch, Generate parity, Check A and B bus parity:

Bus A (B) communicates to Bus B (A), parity is generated and passed on to the B (A) Bus as BPAR (APAR). If LEA and LEB are High and the Mode Select (\overline{SEL}) is Low, the parity generated from A0-A7 and B0-B7 can be checked and monitored by \overline{ERRA} and \overline{ERRB} . (Fault detection on both input and output buses.)

Transparent latch, Feed-through parity, Check A and B bus parity:

Bus A (B) communicates to Bus B (A) in a feed-through mode if \overline{SEL} is High. Parity is still generated and checked as \overline{ERRA} and \overline{ERRB} and can be used as an interrupt to signal a data/parity bit error to the CPU.

Latched input, Generate/Feed-through parity, Check A (and B) bus parity:

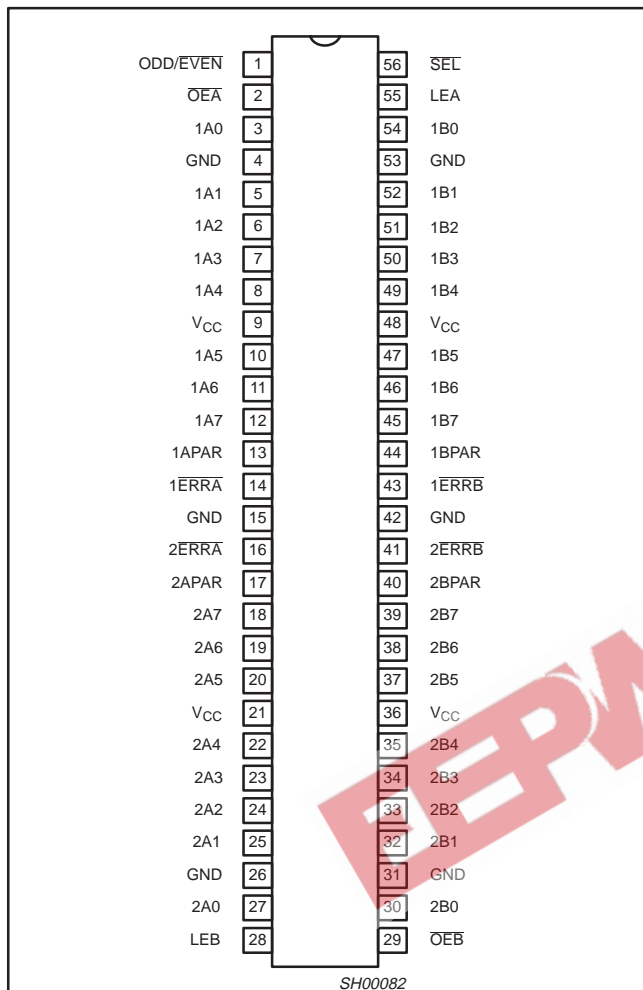
Independent latch enables (LEA and LEB) allow other permutations of:

- Transparent latch / 1 bus latched / both buses latched
- Feed-through parity / generate parity
- Check in bus parity / check out bus parity / check in and out bus parity

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PIN CONFIGURATION



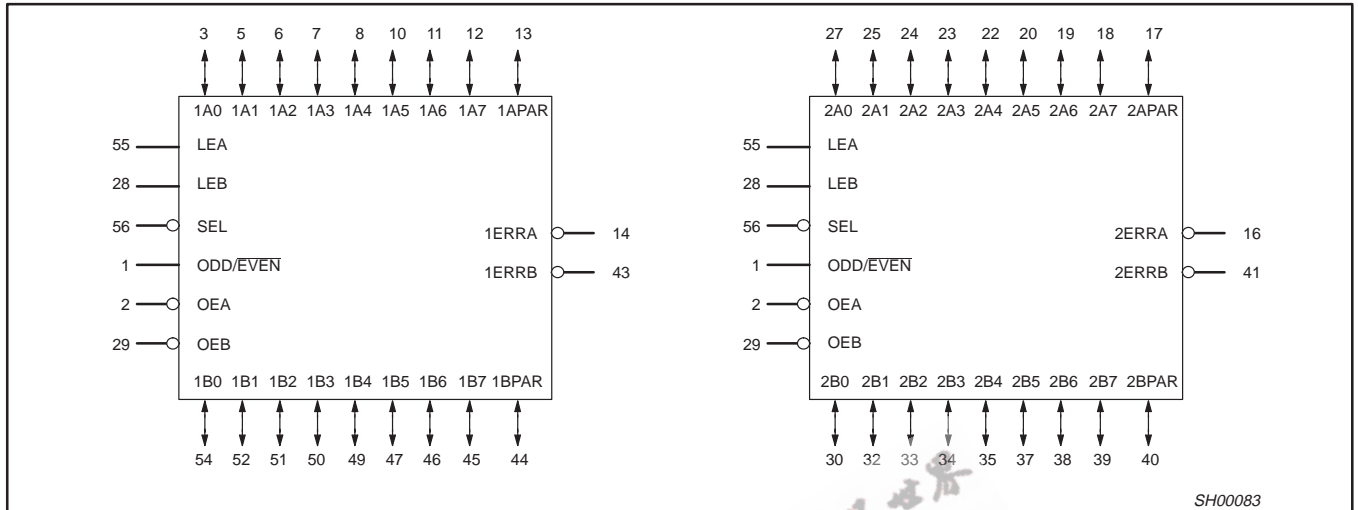
PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
1A0 - 1A7 2A0 - 2A7	3, 5, 6, 7, 8, 10, 11, 12 27, 25, 24, 23, 22, 20, 19, 18	Latched A bus 3-State inputs/outputs
1B0 - 1B7 2B0 - 2B7	54, 52, 51, 50, 49, 47, 46, 45 30, 32, 33, 34, 35, 37, 38, 39	Latched B bus 3-State inputs/outputs
1APAR 2APAR	13, 17	A bus parity 3-State input
1BPAR 2BPAR	44, 40	B bus parity 3-State input
ODD/EVEN	1	Parity select input (Low for EVEN parity)
OE \bar{A} , OE \bar{B}	2, 29	Output enable inputs (gate A to B, B to A)
SEL	56	Mode select input (Low for generate)
LEA, LEB	55, 28	Latch enable inputs (transparent High)
1ERRA, 1ERRB 2ERRA, 2ERRB	14, 43, 16, 41	Error signal outputs (active-Low)
GND	4, 15, 26, 31, 42, 53	Ground (0V)
V _{CC}	9, 21, 36, 48	Positive supply voltage

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LOGIC SYMBOL



PARITY AND ERROR FUNCTION TABLE

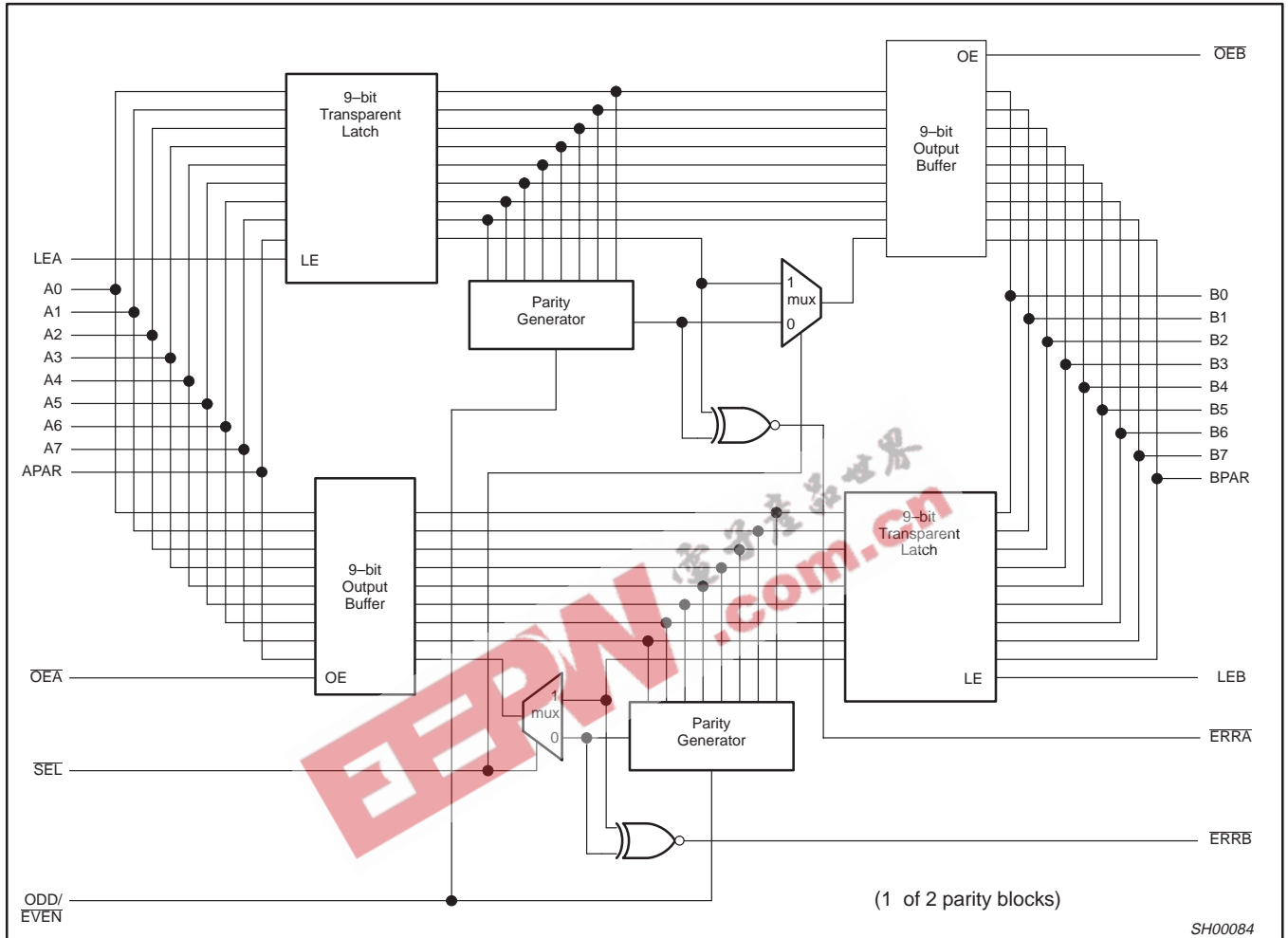
INPUTS				OUTPUTS			PARITY MODES	
SEL	ODD/EVEN	xPAR (A or B)	Σ of High Inputs	xPAR (B or A)	ERRt	ERRr*		
H	H	H	Even Odd	H H	H L	H L	Feed-through/check parity	
H	H	L	Even Odd	L L	L H	L H		
H	L	H	Even Odd	H H	L H	L H		
H	L	L	Even Odd	L L	H L	H L		
L	H	H	Even Odd	H L	H L	H H	Generate parity	
L	H	L	Even Odd	H L	L H	H H		
L	L	H	Even Odd	L H	L H	H H		
L	L	L	Even Odd	L H	H L	H H		

H = High voltage level
 L = Low voltage level
 t = Transmit—if the data path is from A→B then ERRt is ERRA
 r = Receive—if the data path is from A→B then ERRr is ERRB
 * Blocked if latch is not transparent

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BLOCK DIAGRAM



FUNCTION TABLE

INPUTS					OPERATING MODE
OEB	OEA	SEL	LEA	LEB	
H	H	X	X	X	3-State A bus and B bus (input A & B simultaneously)
H	L	L	L	H	B → A, transparent B latch, generate parity from B0 - B7, check B bus parity
H	L	L	H	H	B → A, transparent A & B latch, generate parity from B0 - B7, check A & B bus parity
H	L	L	X	L	B → A, B bus latched, generate parity from latched B0 - B7 data, check B bus parity
H	L	H	X	H	B → A, transparent B latch, parity feed-through, check B bus parity
H	L	H	H	H	B → A, transparent A & B latch, parity feed-through, check A & B bus parity
L	H	L	H	X	A → B, transparent A latch, generate parity from A0 - A7, check A bus parity
L	H	L	H	H	A → B, transparent A & B latch, generate parity from A0 - A7, check A & B bus parity
L	H	L	L	X	A → B, A bus latched, generate parity from latched A0 - A7 data, check A bus parity
L	H	H	H	L	A → B, transparent A latch, parity feed-through, check A bus parity
L	H	H	H	H	A → B, transparent A & B latch, parity feed-through, check A & B bus parity
L	L	X	X	X	Output to A bus and B bus (NOT ALLOWED)

H = High voltage level
L = Low voltage level
X = Don't care

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ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage ³		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage ³	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
		output in High state	-64	
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		-32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT	
			T _{amb} = +25°C			T _{amb} = -40°C to +85°C			
			Min	Typ	Max	Min	Max		
V _{IK}	Input clamp voltage	V _{CC} = 4.5V; I _{IK} = -18mA		-0.7	-1.2		-1.2	V	
V _{OH}	High-level output voltage	V _{CC} = 4.5V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}	2.5	3.1		2.5		V	
		V _{CC} = 5.0V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}	3.0	3.6		3.0		V	
		V _{CC} = 4.5V; I _{OH} = -32mA; V _I = V _{IL} or V _{IH}	2.0	2.7		2.0		V	
V _{OL}	Low-level output voltage	V _{CC} = 4.5V; I _{OL} = 64mA; V _I = V _{IL} or V _{IH}		0.36	0.55		0.55	V	
V _{RST}	Power-up output low voltage ³	V _{CC} = 5.5V; I _O = 1mA; V _I = GND or V _{CC}		0.13	0.55		0.55	V	
I _I	Input leakage current	Control pins	V _{CC} = 5.5V; V _I = GND or 5.5V		±0.2	±1.0		±1.0	μA
		Data pins	V _{CC} = 5.5V; V _I = GND or 5.5V		±1.0	±100		±100	μA
I _{HOLD}	Bushold current A or B inputs ⁵ 74ABTH16899	V _{CC} = 4.5V; V _I = 0.8V	75			75		μA	
		V _{CC} = 4.5V; V _I = 2.0V	-75			-75			
		V _{CC} = 5.5V; V _I = 0 to 5.5V	±500						
I _{OFF}	Power-off leakage current	V _{CC} = 0.0V; V _O or V _I ≤ 4.5V		±2.0	±100		±100	μA	
I _{PU} /I _{PD}	Power-up/down 3-State output current ⁴	V _{CC} = 2.1V; V _O = 0.5V; V _I = GND or V _{CC}		±5.0	±50		±50	μA	
I _{IH} + I _{OZH}	3-State output High current	V _{CC} = 5.5V; V _O = 2.7V; V _I = V _{IL} or V _{IH}		2.0	50		50	μA	
I _{IL} + I _{OZL}	3-State output Low current	V _{CC} = 5.5V; V _O = 0.5V; V _I = V _{IL} or V _{IH}		-2.0	-50		-50	μA	
I _{CEX}	Output High leakage current	V _{CC} = 5.5V; V _O = 5.5V; V _I = GND or V _{CC}		2.0	50		50	μA	
I _O	Output current ¹	V _{CC} = 5.5V; V _O = 2.5V	-50	-100	-180	-50	-180	mA	
I _{CCH}	Quiescent supply current	V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC}		0.5	1		1	mA	
I _{CCL}		V _{CC} = 5.5V; Outputs Low, V _I = GND or V _{CC}		10.5	19		19	mA	
I _{CCZ}		V _{CC} = 5.5V; Outputs 3-State; V _I = GND or V _{CC}		0.5	1		1	mA	
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 5.5V; one input at 3.4V, other inputs at V _{CC} or GND		0.2	1.5		1.5	mA	

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100μsec is permitted.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

18-bit latched transceiver with 16-bit parity generator/checker (3-State)

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AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	1	1.0 1.0	2.7 2.2	4.5 3.5	1.0 1.0	5.5 6.9	ns
t_{PLH} t_{PHL}	Propagation delay An to BPAR or Bn to APAR	2	2.5 2.5	4.9 5.0	7.2 7.4	2.5 2.5	8.8 8.7	ns
t_{PLH} t_{PHL}	Propagation delay An to $\overline{\text{ERRA}}$ or Bn to $\overline{\text{ERRB}}$	3	2.8 2.8	5.0 4.9	9.3 8.0	2.8 2.8	11.0 10.2	ns
t_{PLH} t_{PHL}	Propagation delay APAR to BPAR or BPAR to APAR	1	1.5 1.5	3.1 2.5	3.9 3.1	1.5 1.5	4.8 3.9	ns
t_{PLH} t_{PHL}	Propagation delay APAR to $\overline{\text{ERRA}}$ or BPAR to $\overline{\text{ERRB}}$	6	1.0 1.0	2.5 2.5	3.3 3.3	1.0 1.0	4.3 3.9	ns
t_{PLH} t_{PHL}	Propagation delay ODD/EVEN to APAR or BPAR	5	2.5 2.5	4.1 3.9	5.1 5.0	2.5 2.5	6.1 5.7	ns
t_{PLH} t_{PHL}	Propagation delay ODD/EVEN to $\overline{\text{ERRA}}$ or $\overline{\text{ERRB}}$	4	2.5 2.5	4.1 4.0	6.1 5.5	2.5 2.5	7.1 6.6	ns
t_{PLH} t_{PHL}	Propagation delay SEL to APAR or BPAR	8	1.5 1.5	3.1 2.6	4.0 3.4	1.5 1.5	5.0 4.2	ns
t_{PLH} t_{PHL}	Propagation delay SEL to $\overline{\text{ERRA}}$ or $\overline{\text{ERRB}}$	8	2.5 2.5	5.0 4.4	7.5 5.9	2.5 2.5	8.3 7.1	ns
t_{PLH} t_{PHL}	Propagation delay LEA to Bn or LEB to An	9	1.0 1.0	3.1 2.8	4.2 4.3	1.0 1.0	5.2 4.7	ns
t_{PLH} t_{PHL}	Propagation delay LEA to BPAR or LEB to APAR	9	2.8 2.8	5.5 5.1	8.0 7.7	2.8 2.8	9.7 9.1	ns
t_{PLH} t_{PHL}	Propagation delay LEA to $\overline{\text{ERRA}}$ or LEB to $\overline{\text{ERRB}}$	7	1.1 1.2	5.4 5.8	8.0 8.0	1.1 1.2	9.2 9.6	ns
t_{PZH} t_{PZL}	Output enable time $\overline{\text{OEA}}$ to An, APAR or $\overline{\text{OEB}}$ to Bn, BPAR	11, 12	1.0 1.0	2.6 2.3	3.6 3.2	1.0 1.0	5.1 4.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{\text{OEA}}$ to An, APAR or $\overline{\text{OEB}}$ to Bn, BPAR	11, 12	2.5 1.5	3.9 2.8	5.6 4.1	2.5 1.5	6.0 4.4	ns

AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$, $R_L = 500\Omega$

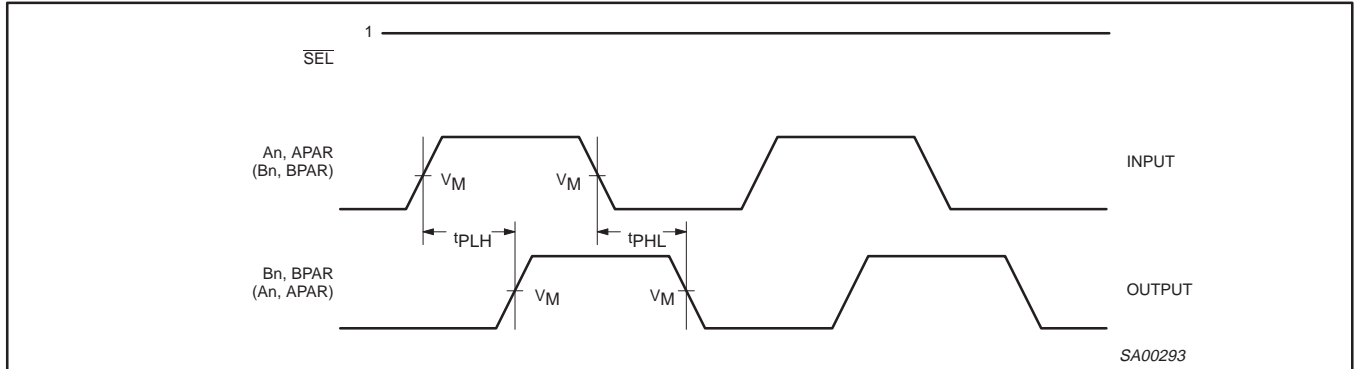
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		$T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$	
			Min	Typ	Min	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low An, APAR to LEA or Bn, BPAR to LEB	10	1.5 1.0	0.3 -0.1	1.5 1.0	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low An, APAR to LEA or Bn, BPAR to LEB	10	1.5 1.0	0.1 -0.2	1.5 1.0	ns
$t_w(\text{H})$	Pulse width, High LEA or LEB	10	3.0	1.0	3.0	ns

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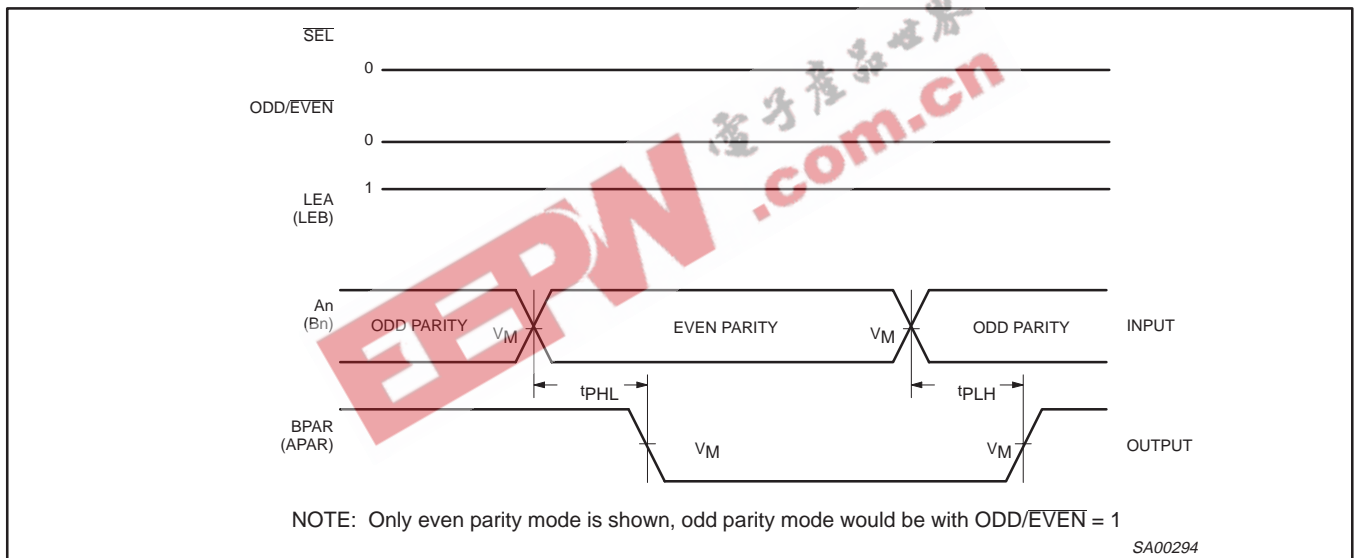
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AC WAVEFORMS

$V_M = 1.5V, V_{IN} = GND \text{ to } 3.0V$

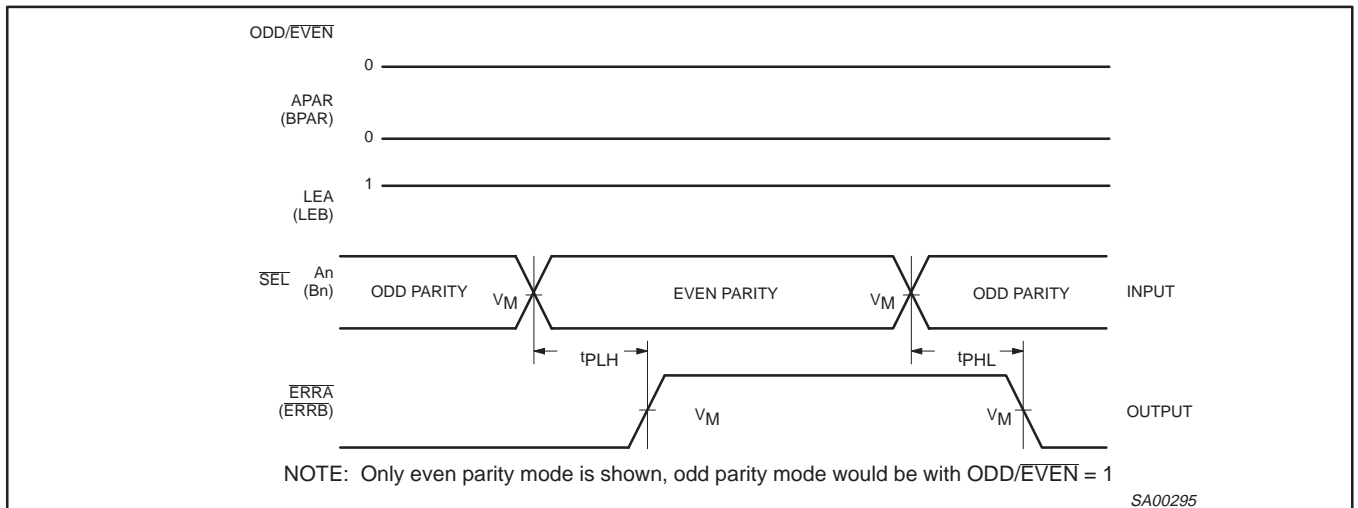


Waveform 1. Propagation Delay, An to Bn, Bn to An, APAR to BPAR, BPAR to APAR



NOTE: Only even parity mode is shown, odd parity mode would be with ODD/EVEN = 1

Waveform 2. Propagation Delay, An to BPAR or Bn to APAR

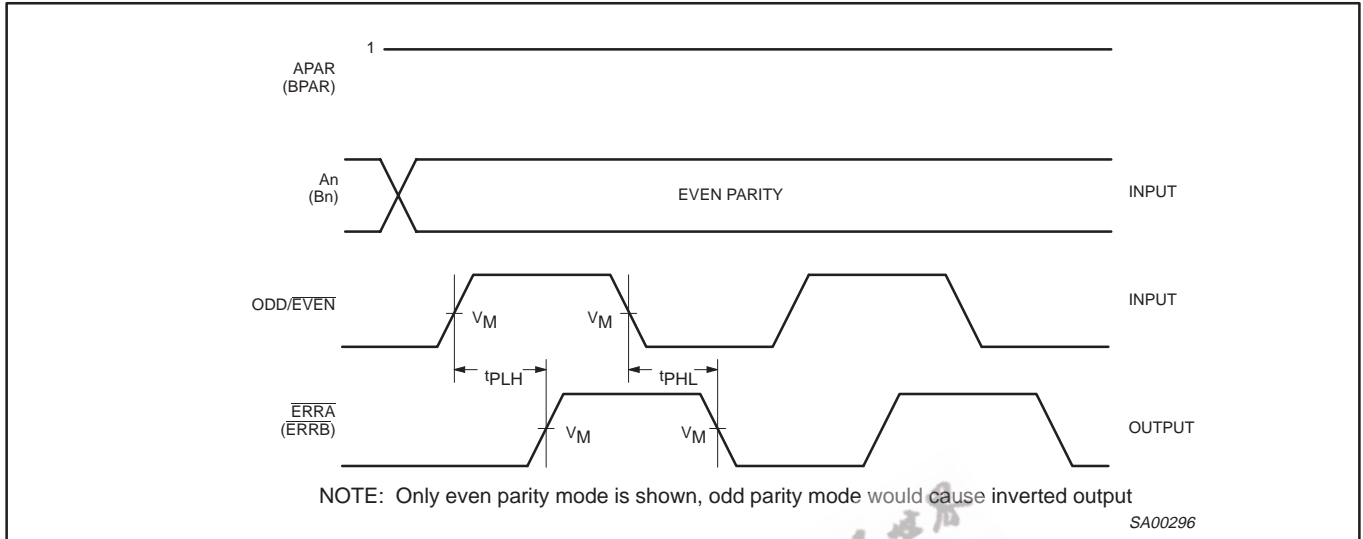


NOTE: Only even parity mode is shown, odd parity mode would be with ODD/EVEN = 1

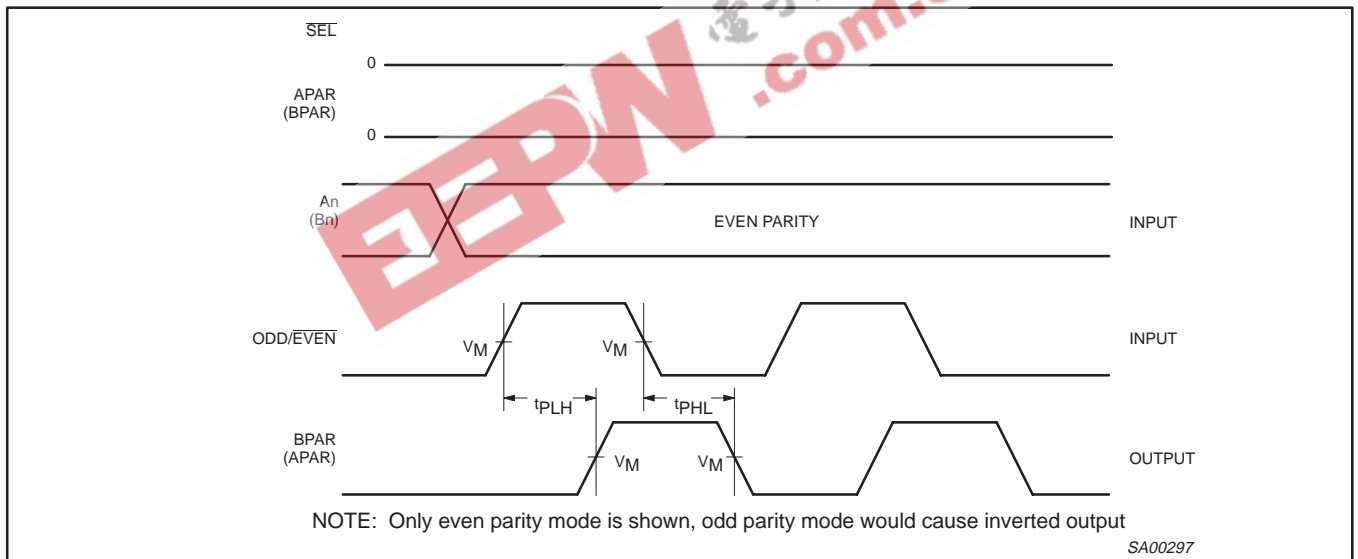
Waveform 3. Propagation Delay, An to ERR̄A or Bn to ERR̄B

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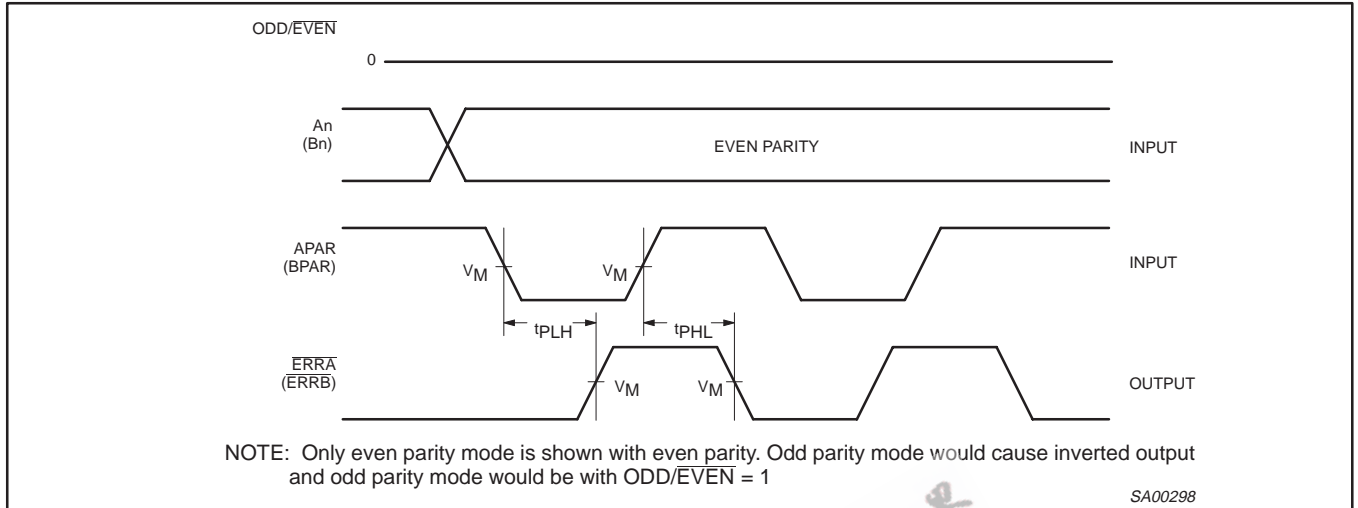
Waveform 4. Propagation Delay, ODD/EVEN to ERRA or ODD/EVEN to ERRB



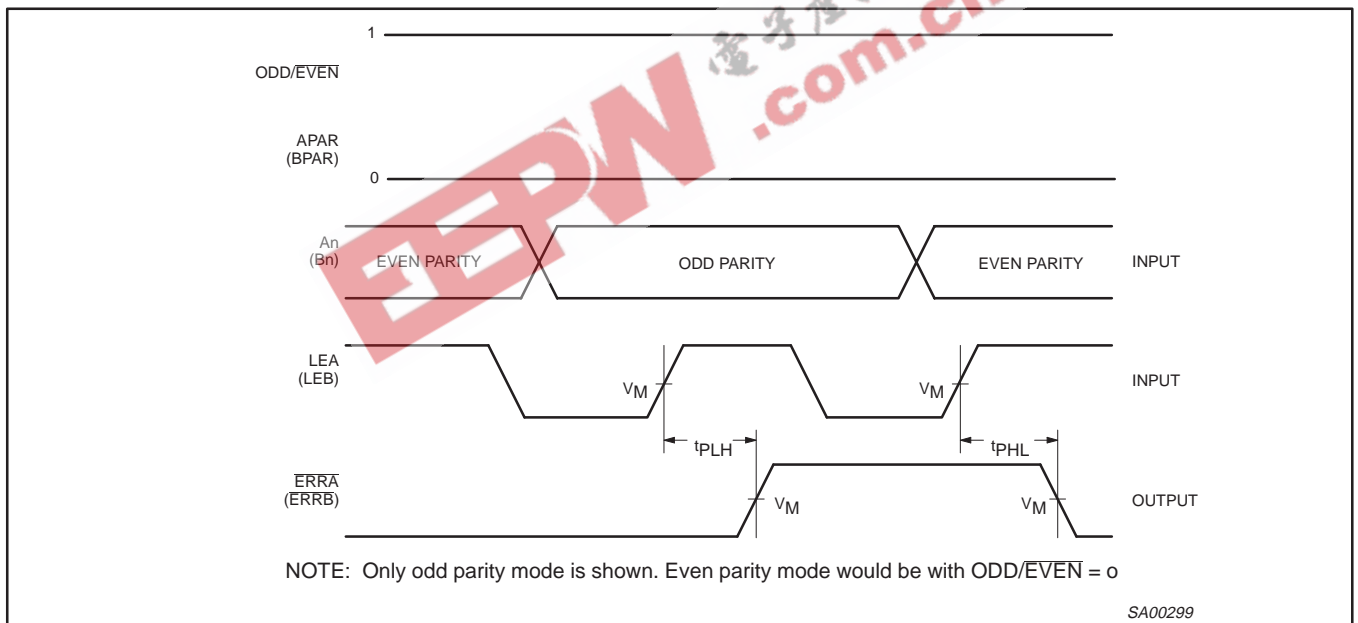
Waveform 5. Propagation Delay, ODD/EVEN to APAR or ODD/EVEN to BPAR

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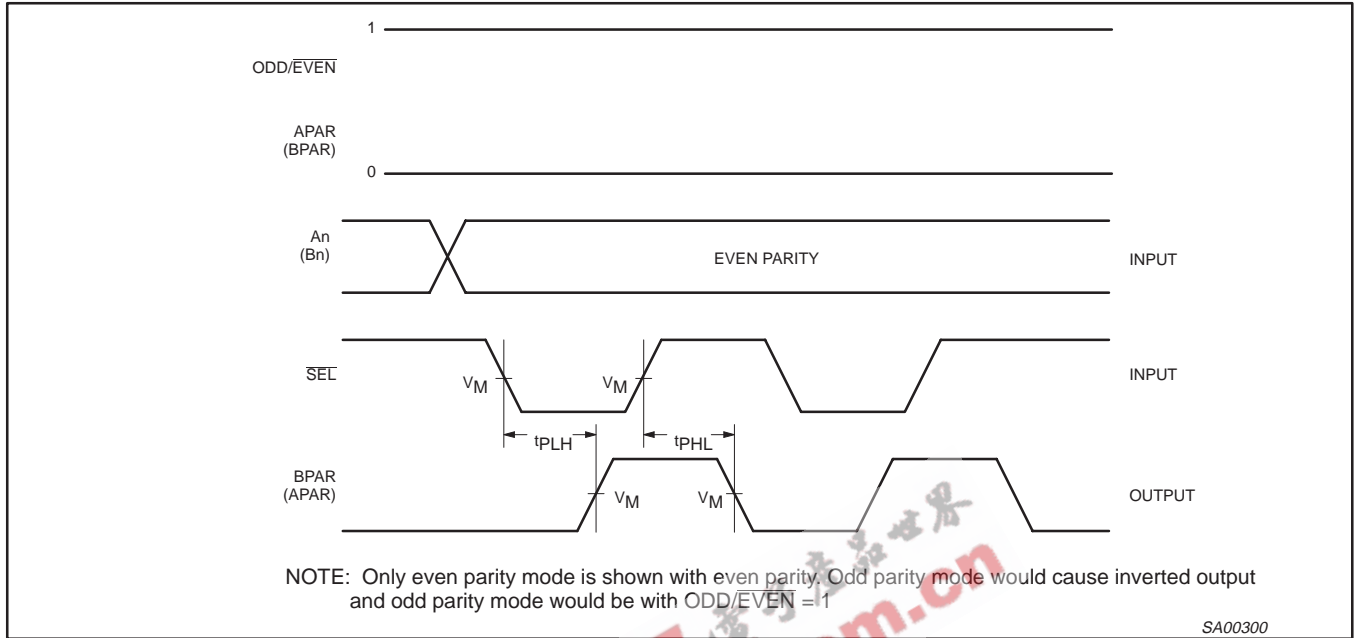
Waveform 6. Propagation Delay, APAR to ERRA or BPAR to ERRB



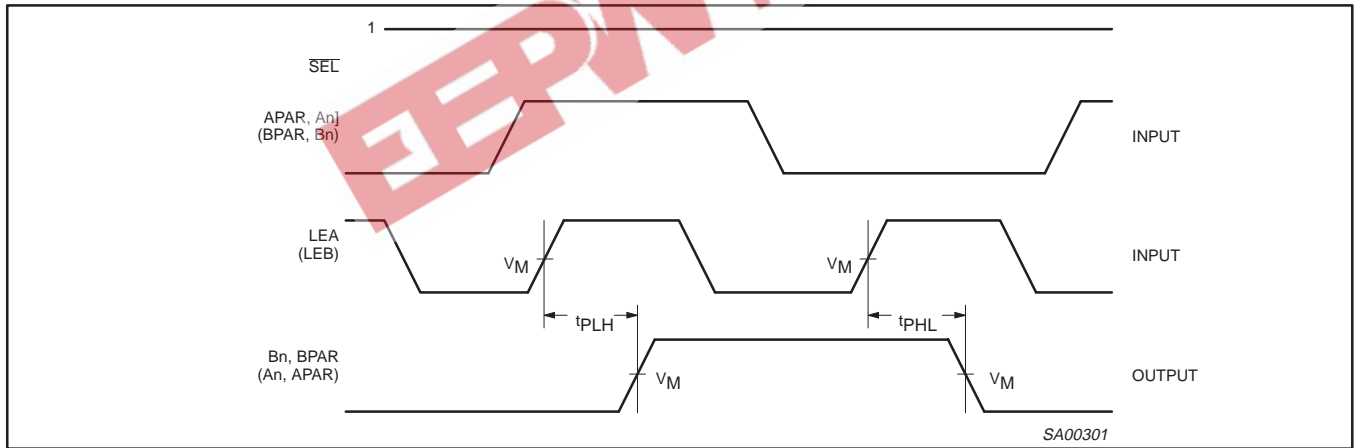
Waveform 7. Propagation Delay, LEA to ERRA or LEB to ERRB

18-bit latched transceiver with 16-bit parity generator/checker (3-State)

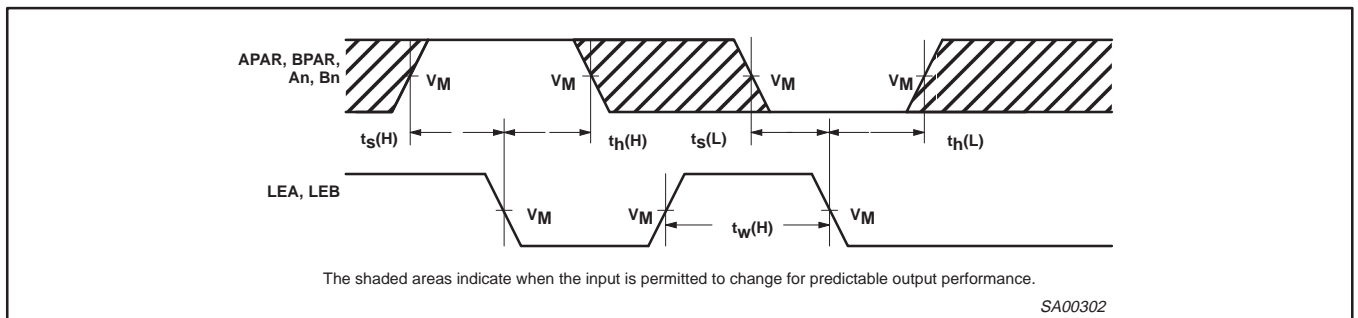
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Waveform 8. Propagation Delay, SEL to BPAR or SEL to APAR



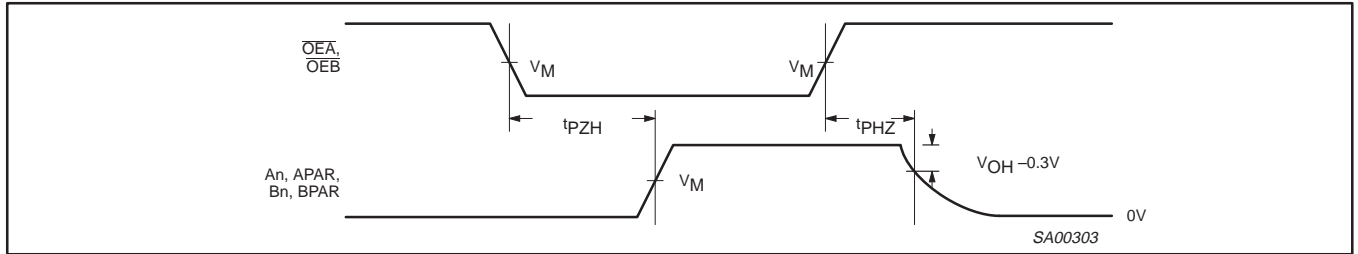
Waveform 9. Propagation Delay, LEA to BPAR or LEB to APAR, LEA to Bn or LEB to An



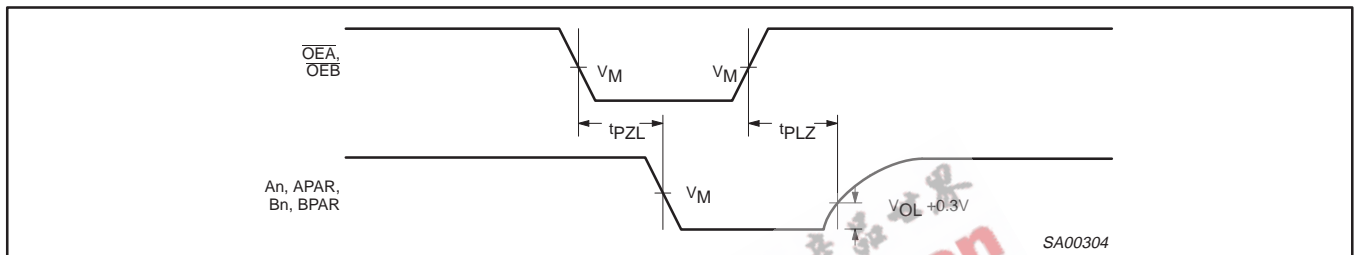
Waveform 10. Data Setup and Hold Times, Pulse Width High

18-bit latched transceiver with 16-bit parity generator/checker (3-State)

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Waveform 11. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 12. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM

Test Circuit for Open Collector Outputs

Input Pulse Definition

SWITCH POSITION	
TEST	SWITCH
t _{PLZ}	closed
t _{PZL}	closed
All other	open

LOAD VALUES		
OUTPUT	R _X	V _X
ERROR	100 Ω	V _{CC}
All other	500 Ω	7.0V

DEFINITIONS:

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t _w	t _R	t _F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

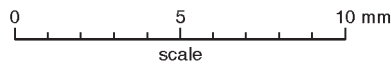
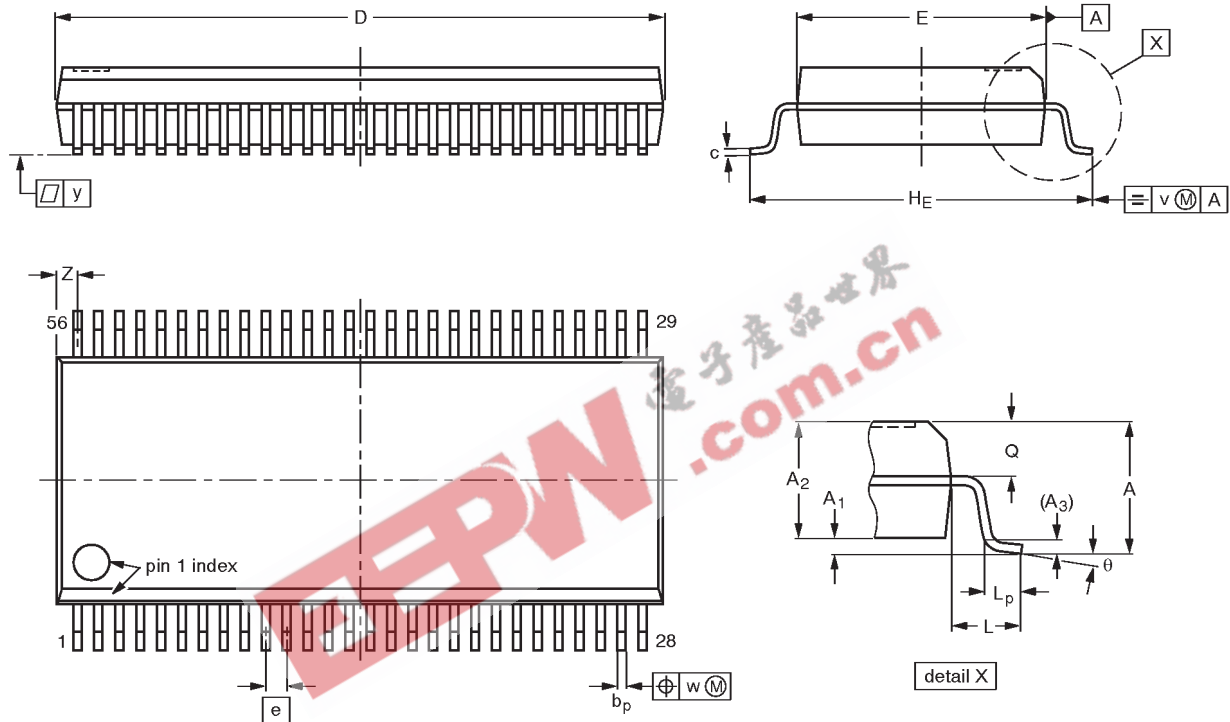
SH00009

18-bit latched transceiver with 16-bit parity generator/checker (3-State)

74ABT16899
74ABTH16899

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

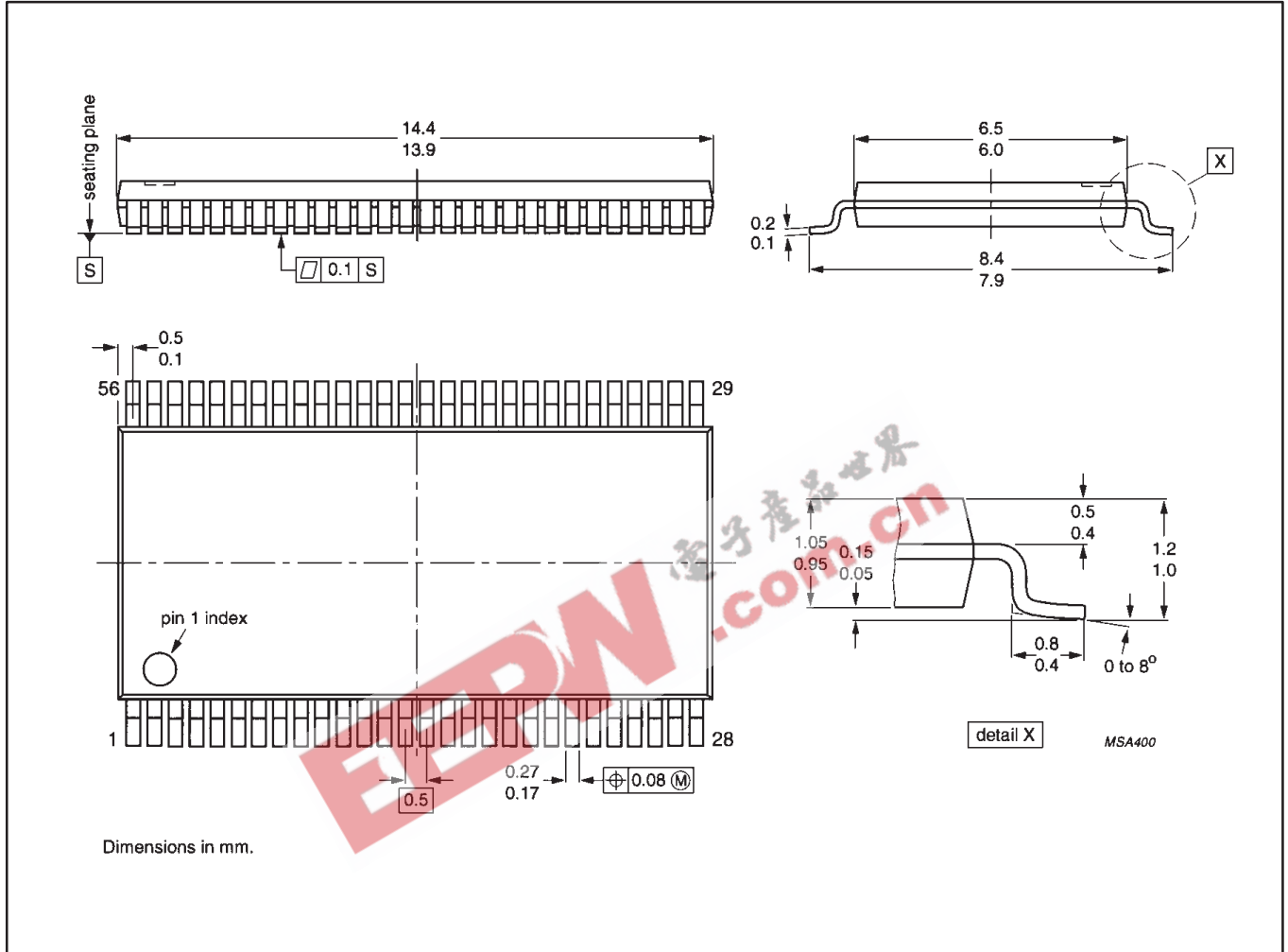
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118AB				93-11-02 95-02-04

18-bit latched transceiver with 16-bit parity generator/checker (3-State)

74ABT16899
74ABTH16899

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



18-bit latched transceiver with 16-bit parity generator/checker (3-State)

74ABT16899
74ABTH16899

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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