Octal inverting transceiver with parity generator/checker (3–State)

74ABT834

FEATURES

- Low static and dynamic power dissipation with high speed and high output drive
- Open–collector $\overline{\text{ERROR}}$ output
- Output capability: +64mA/–32mA
- Latch–up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model
- Power up/down 3–State

DESCRIPTION

The 74ABT834 high–performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT834 is an octal inverting transceiver with a parity generator/checker and is intended for bus–oriented applications.

When Output Enable A ($\overline{\text{OEA}}$) is High, it will place the A outputs in a high impedance state. Output Enable B ($\overline{\text{OEB}}$) controls the B outputs in the same way.

The parity generator creates an odd parity output (PARITY) when $\overline{\text{OEB}}$ is Low. When $\overline{\text{OEA}}$ is Low, the parity of the B port, including the PARITY input, is checked for odd parity. When an error is detected, the error data is sent to the input of a storage register. If a Low–to–High transition happens at the clock input (CP), the error data is stored in the register and the Open–collector error flag ($\overline{\text{ERROR}}$) will go Low. The error flag register is cleared with a Low pulse on the $\overline{\text{CLEAR}}$ input.

If both $\overline{\text{OEA}}$ and $\overline{\text{OEB}}$ are Low, data will flow from the A bus to the B bus and the part is forced into an error condition which creates an inverted PARITY output. This error condition can be used by the designer for system diagnostics.

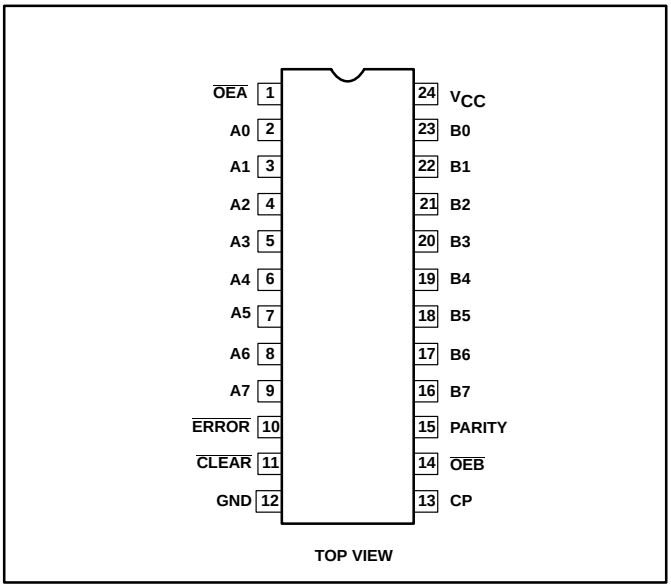
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	3.4	ns
t_{PLH} t_{PHL}	Propagation delay An to PARITY	C_L = 50pF; V_{CC} = 5V	7.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	50	µA

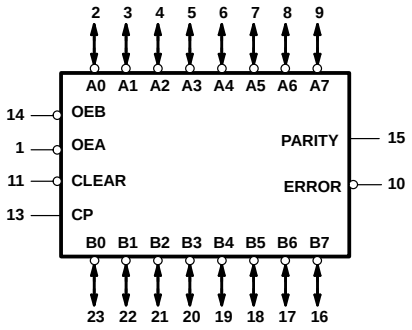
ORDERING INFORMATION

PACKAGES	CONDITIONS T_{amb} = 25°C; GND = 0V	ORDER CODE
24–pin plastic DIP (300mil)	–40°C to +85°C	74ABT834N
24–pin plastic SOL (300mil)	–40°C to +85°C	74ABT834D

PIN CONFIGURATION



LOGIC SYMBOL



Octal inverting transceiver with parity generator/checker (3–State) 74ABT834

PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
A0 – A7	2, 3, 4, 5, 6, 7, 8, 9	A port 3–State inputs/outputs
B0 – B7	23, 22, 21, 20, 19, 18, 17, 16	B port 3–State inputs/outputs
$\overline{OEA}$	1	Enables the A outputs when Low
$\overline{OEB}$	14	Enables the B outputs when Low
PARITY	15	Parity output
$\overline{ERROR}$	10	Error output
$\overline{CLEAR}$	11	Clears the error flag register when Low
CP	13	Clock input
GND	12	Ground (0V)
V_{CC}	24	Positive supply voltage

FUNCTION TABLE

MODE	INPUTS				OUTPUTS		
	$\overline{OEB}$	$\overline{OEA}$	An Σ of Highs	Bn + Parity Σ of Lows	An	Bn	PARITY
$\overline{A}$ data to B bus and generate odd parity output	L	H	Odd Even	NA (output)	NA (input)	$\overline{An}$	H L
$\overline{B}$ data to A bus and check for parity error[1]	H	L	NA (output)	Odd Even	$\overline{Bn}$	NA (input)	NA (input)
A bus and B bus disabled[2]	H	H	X	X	Z	Z	Z
$\overline{A}$ data to B bus and generate inverted parity output	L	L	Odd Even	NA (output)	NA (input)	$\overline{An}$	L H

NOTES:
1. Error checking is detailed in the Error Flag Function Table below.
2. When clocked, the error output is Low if the sum of A inputs is even or High if the sum of A inputs is odd.

ERROR FLAG FUNCTION TABLE

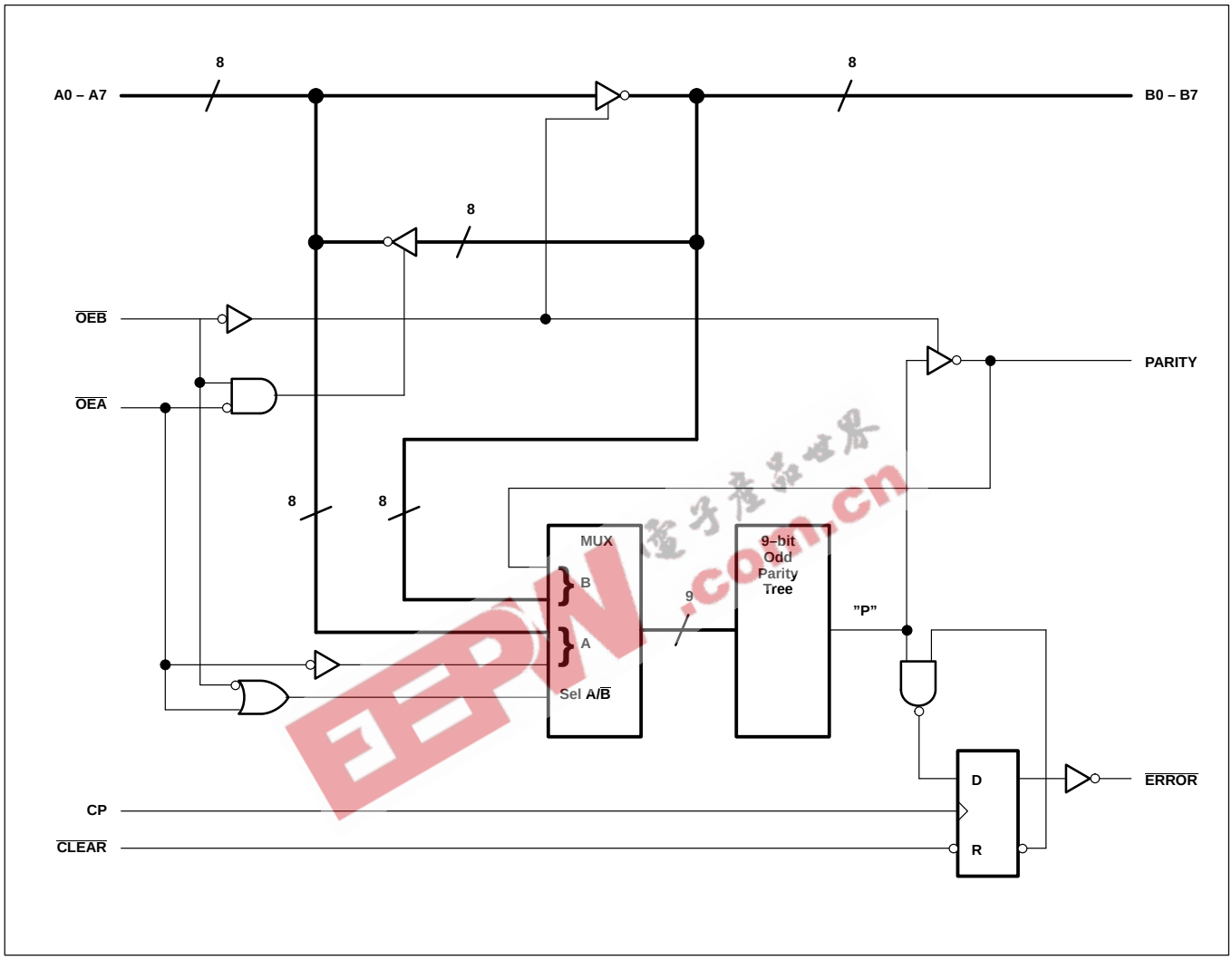
MODE	INPUTS			Internal node	Output	
	$\overline{CLEAR}$	CP	Bn + Parity Σ of Lows	Point "P"	Pre–state $\overline{ERROR}$n–1	$\overline{ERROR}$ OUTPUT
Sample	H H H	↑ ↑ X	Odd Even X	H L X	H X L	H L L
Hold	H	↥	X	X	X	NC
Clear	L	X	X	X	X	H

H = High voltage level steady state
L = Low voltage level steady state
X = Don't care
NA = Not applicable
NC = No change
Z = High impedance "off" state
↑ = Low–to–High clock transition
↥ = Not a Low–to–High clock transition

Octal inverting transceiver with parity generator/checker (3–State)

74ABT834

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
2. The performance capability of a high–performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High–level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
V_{OH}	High–level output voltage, $\overline{ERROR}$		5.5	V
I_{OH}	High–level output current		–32	mA
I_{OL}	Low–level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free–air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
I_{OH}	High–level output current $\overline{ERROR}$ ONLY		V_{CC} = 5.5V; V_{OH} = 5.5V; V_I = V_{IL} or V_{IH}			20		20	µA
V_{OH}	High–level output voltage		V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		V
			V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		V
V_{OL}	Low–level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±5	±100		±100	µA
I_{IH} + I_{OZH}	3–State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3–State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_O	Output current[1]		V_{CC} = 5.5V; V_O = 2.5V	–50	–80	–180	–50	–180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		50	250		250	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		20	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}		50	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]		V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.3	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORMS	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = –40 to +85°C, V_{CC} = +5.0V ±10%		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2						ns
t_{PLH} t_{PHL}	Propagation delay An to PARITY	1, 2						ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OEA}$ to PARITY	1, 2						ns
t_{PLH}	Propagation delay $\overline{CLEAR}$ to $\overline{ERROR}$	5						ns
t_{PHL}	Propagation delay CP to $\overline{ERROR}$	1						ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEA}$ to An or $\overline{OEB}$ to Bn, PARITY	3, 4						ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEA}$ to An or $\overline{OEB}$ to Bn, PARITY	3, 4						ns

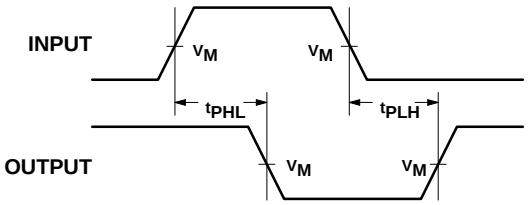
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

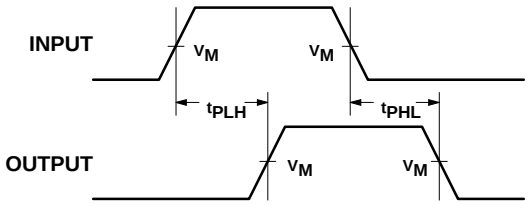
SYMBOL	PARAMETER	WAVEFORMS	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = –40 to +85°C, V_{CC} = +5.0V ±10%		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Bn or PARITY to CP	6						ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Bn or PARITY to CP	6						ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CP	6						ns
$t_w(L)$	Pulse width, Low $\overline{CLEAR}$	5						ns
t_{rec}	Recovery time $\overline{CLEAR}$ to CP	5						ns

AC WAVEFORMS

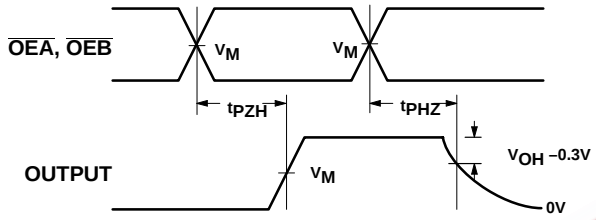
V_M = 1.5V, V_{IN} = GND to 3.0V



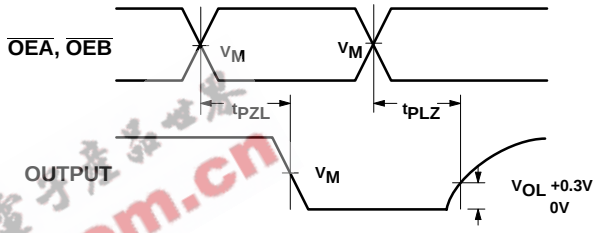
Waveform 1. Propagation Delay For Inverting Output



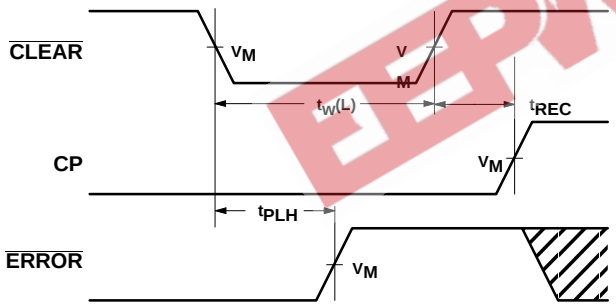
Waveform 2. Propagation Delay For Non–Inverting Output



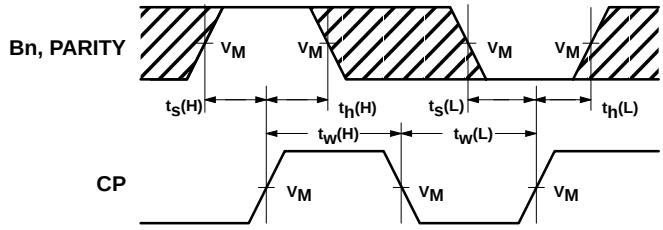
Waveform 3. 3–State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. 3–State Output Enable Time to Low Level and Output Disable Time from Low Level



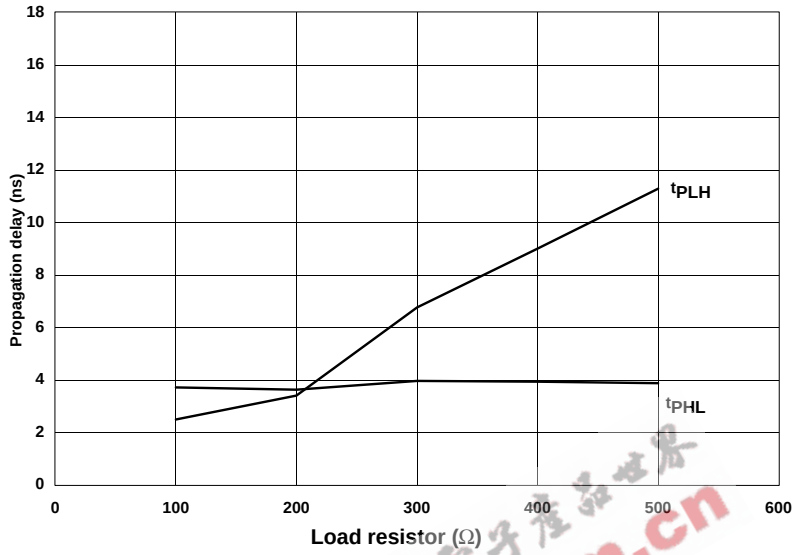
Waveform 5. $\overline{\text{CLEAR}}$ Pulse Width, $\overline{\text{CLEAR}}$ to $\overline{\text{ERROR}}$ Delay and $\overline{\text{CLEAR}}$ to Clock Recovery Time



Waveform 6. Data Setup and Hold Times and Clock Pulse Width

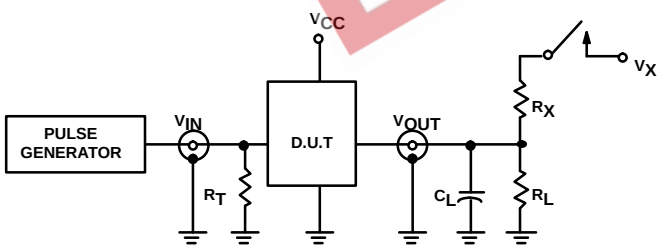
NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS

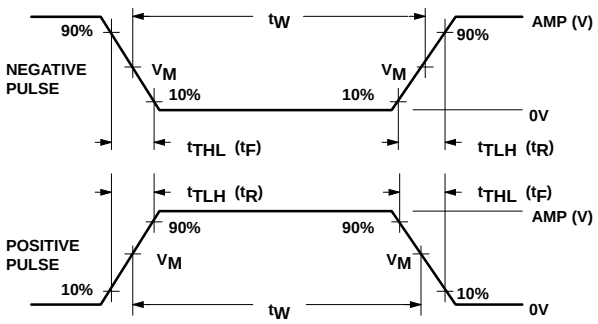


NOTE:
When using Open–Collector parts, the value of the pull–up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull–up resistor value from 500Ω to 100Ω will improve the t_{PLH} over 300% with only a slight change in the t_{PHL}. However, if the value of the pull–up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers does not exceed the I_{OL} maximum specification.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3–State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

LOAD VALUES

OUTPUT	R_X	V_X
$\overline{\text{ERROR}}$	100Ω	V_{CC}
All other	500Ω	7.0V

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns