

October 1991 Revised August 1999

74FR240

Octal Buffer/Line Driver with 3-STATE Outputs

General Description

The 74FR240 is an inverting octal buffer and line driver designed to be employed as memory and address driver, clock driver and bus oriented transmitter or receiver.

Features

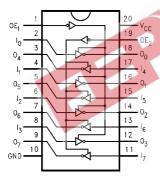
- 3-STATE outputs drive bus lines or buffer memory address registers
- Outputs sink 64 mA and source 15 mA
- Guaranteed pin-to-pin skew

Ordering Code:

Order Number	Package Number	Package Description
74FR240SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74FR240SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74FR240PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code

Connection Diagram



Pin Descriptions

Pin Names	Description
\overline{OE}_1 , \overline{OE}_2	Output Enable Input (Active-LOW)
I ₀ -I ₇	Inputs
$\overline{O}_0 - \overline{O}_7$	Outputs

Truth Tables

Inputs		Outputs				
OE ₁	I _n	(Pins 12, 14, 16, 18)				
L	L	Н				
L	Н	L				
Н	Х	Z				

Inp	outs	Outputs
OE ₂	I _n	(Pins 3, 5, 7, 9)
L	L	Н
L	Н	L
Н	Х	Z

H = HIGH Voltage Level

L = LOW Voltage Level X = Immaterial

Z = High Impedance

Absolute Maximum Ratings(Note 1)

Recommended Operating Conditions

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Ambient Temperature under Bias -55° C to +125 $^{\circ}$ C Junction Temperature under Bias -55° C to +150 $^{\circ}$ C

 $\begin{array}{lll} \text{V}_{\text{CC}} \text{ Pin Potential to Ground Pin} & -0.5 \text{V to } +7.0 \text{V} \\ \text{Input Voltage (Note 2)} & -0.5 \text{V to } +7.0 \text{V} \\ \text{Input Current (Note 2)} & -30 \text{ mA to } +5.0 \text{ mA} \\ \end{array}$

Voltage Applied to Output

in HIGH State (with $V_{CC} = 0V$)

Standard Output -0.5V to V_{CC} 3-STATE Output -0.5V to +5.5V

Current Applied to Output

in LOW State (Max) Twice the Rated I_{OL} (mA)

ESD Last Passing Voltage (Min) 40

Free Air Ambient Temperature $0^{\circ}\text{C} \text{ to } +70^{\circ}\text{C}$ Supply Voltage +4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Тур	Max	Units	V _{CC}	Conditions
			тур	IVIAA	4.	A C C	
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	$I_{IN} = -18 \text{ mA}$
V _{OH}	Output HIGH Voltage	2.4	4	V31	V	Min	$I_{OH} = -3 \text{ mA}$
		2.0		100	V	Min	I _{OH} = -15 mA
V _{OL}	Output LOW Voltage			0.55	V	Min	I _{OL} = 64 mA
I _{IH}	Input HIGH Current			5	μА	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current			7	^	Max	V 7.0V
	Breakdown Test			,	μА	IVIAX	$V_{IN} = 7.0V$
I _{IL}	Input Low Current			-150	μΑ	Max	V _{IN} = 0.5V
V _{ID}	Input Leakage Test	4.75			V	0.0	$I_{ID} = 1.9 \mu A$,
							All Other Pins Grounded
I _{OD}	Output Circuit Leakage Current			3.75	μА	0.0	V _{IOD} = 150 mV,
							All Other Pins Grounded
l _{OZH}	Output Leakage Current			20	μΑ	Max	V _{OUT} = 2.7V
l _{OZL}	Output Leakage Current			-20	μА	Max	V _{OUT} = 0.5V
los	Output Short-Circuit Current	-100		-225	mA	Max	V _{OUT} = 0.0V
I _{CEX}	Output HIGH Leakage Current			50	μА	Max	$V_{OUT} = V_{CC}$
I _{ZZ}	Bus Drainage Test			100	μΑ	0.0	V _{OUT} = 5.25V
Іссн	Power Supply Current		9	13	mA	Max	All Outputs HIGH
I _{CCL}	Power Supply Current		37	45	mA	Max	All Outputs LOW
I _{CCZ}	Power Supply Current		31	38	mA	Max	Outputs 3-STATE
C _{IN}	Input Capacitance		8.0		pF	5.0	

AC Electrical Characteristics

Symbol	Parameter		$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$		$T_A = 0$ °C to +70°C $V_{CC} = +5.0V$ $C_L = 50$ pF		Units
		Min	Тур	Max	Min	Max	
t _{PLH}	Propagation Delay	1.0	3.3	4.7	1.0	4.7	ns
t _{PHL}	A _n to B _n or B _n to A _n	1.0	2.9	4.7	1.0	4.7	115
t _{PZH}	Output Enable Time	2.6	4.0	7.0	2.6	7.0	
t_{PZL}		2.6	6.3	7.0	2.6	7.0	ns
t _{PHZ}	Output Disable Time	1.7	3.3	6.6	1.7	6.6	ns
t_{PLZ}		1.7	2.9	6.6	1.7	6.6	115

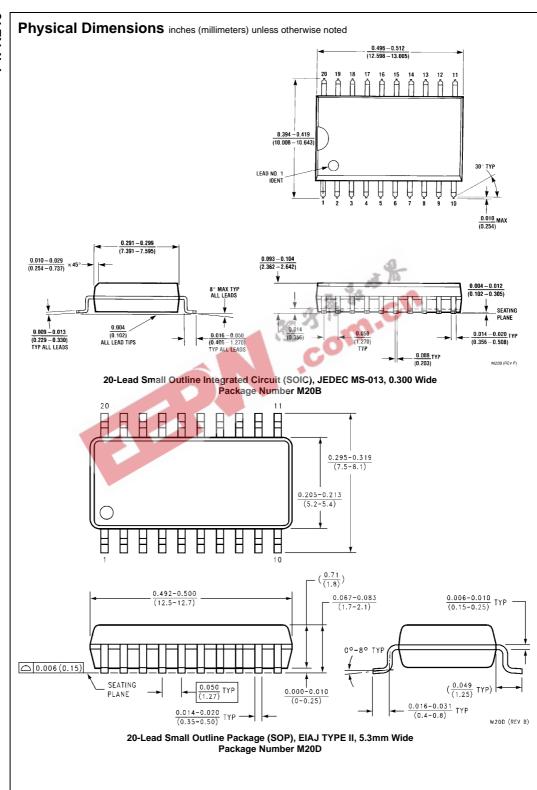
Extended AC Electrical Characteristics

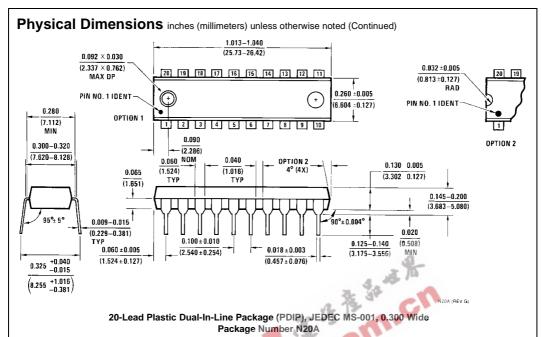
Symbol	Parameter	$T_A = 0^{\circ}C \text{ to } +70^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$ Eight Outputs Switching (Note 3)		$T_A = 0^{\circ}C \text{ to } +70^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 250 \text{ pF}$ (Note 4)		Units
		Min	Max	Min	Max	
t _{PLH}	Propagation Delay	1.0	6.4	2.3	8.3	
t _{PHL}	A_n to B_n or B_n to A_n	1.0	6.4	2.3	8.3	ns
t _{PZH}	Output Enable Time	2.6	7.2			ns
t _{PZL}		2.6	7.2			115
t _{PHZ}	Output Disable Time	1.7	6.8			ns
t _{PLZ}		1.7	6.8			113
toshl	Pin-to-Pin Skew		2.0			ns
(Note 5)	for HL Transitions		2.0			113
t _{OSLH}	Pin-to-Pin Skew		1.1			ns
(Note 5)	for LH Transitions		1.1			113
t _{OST}	Pin-to-Pin Skew		3.1			ns
(Note 5)	for HL/LH Transitions		3.1			115

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase, i.e., all LOW-to-HIGH, HIGH-to-LOW, 3-STATE-to-HIGH, etc.

Note 4: These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 5: Skew is defined as the absolute value of the difference between the actual propagation delays for any two outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW, (toSHL), LOW-to-HIGH, (toSLH), or HIGH-to-LOW and/or LOW-to-HIGH, (toST). Specifications guaranteed with all outputs switching in phase.





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