

74LVT125

3.3 V quad buffer; 3-state

Rev. 05 — 10 February 2005

Product data sheet

1. General description

The LVT125 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V.

This device combines low static and dynamic power dissipation with high speed and high output drive. The 74LVT125 device is a quad buffer that is ideal for driving bus lines. The device features four output enable inputs ($\overline{1OE}$, $\overline{2OE}$, $\overline{3OE}$ and $\overline{4OE}$), each controlling one of the 3-state outputs.

2. Features

- Quad bus interface
- 3-state buffers
- Output capability: +64 mA and –32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- No bus current loading when output is tied to 5 V bus
- Power-up 3-state
- Latch-up protection:
 - ◆ JESD78: exceeds 500 mA
- ESD protection:
 - ◆ MIL STD 883 method 3015: exceeds 2000 V
 - ◆ Machine model: exceeds 200 V

3. Quick reference data

Table 1: Quick reference data

$GND = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	propagation delay nA to nY	$C_L = 50\text{ pF}$; $V_{CC} = 3.3\text{ V}$	-	2.7	-	ns
t_{PHL}	propagation delay nA to nY	$C_L = 50\text{ pF}$; $V_{CC} = 3.3\text{ V}$	-	2.9	-	ns
C_I	input capacitance	$V_I = 0\text{ V}$ or 3.0 V	-	4	-	pF
C_O	output capacitance	outputs disabled; $V_O = 0\text{ V}$ or 3.0 V	-	8	-	pF
I_{CC}	quiescent supply current	outputs disabled; $V_{CC} = 3.6\text{ V}$	-	0.13	-	mA

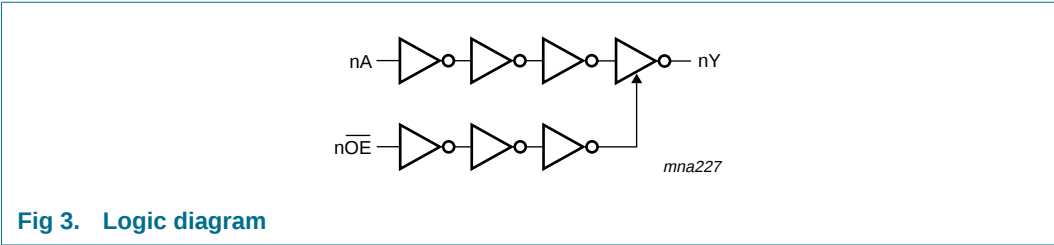
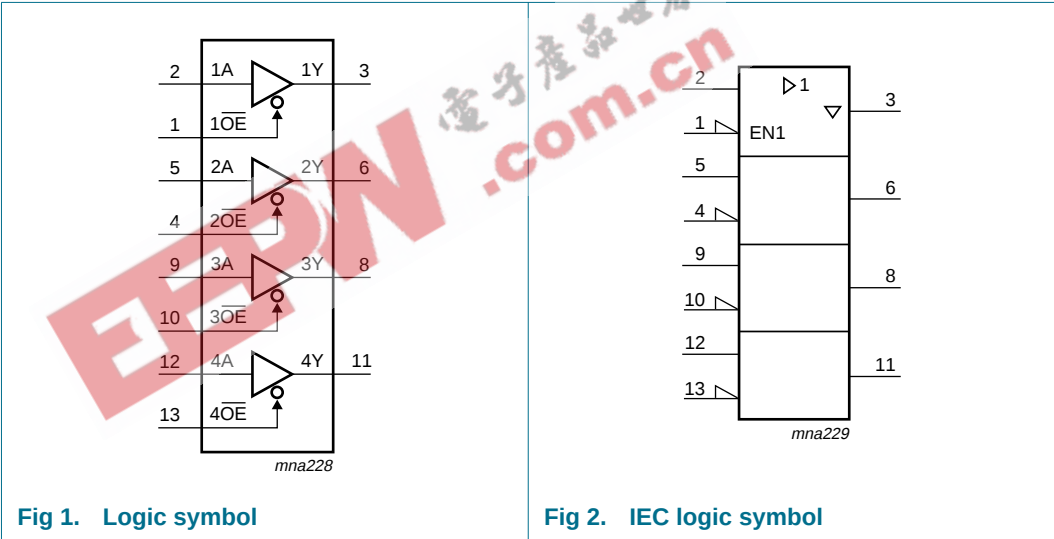
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4. Ordering information

Table 2: Ordering information

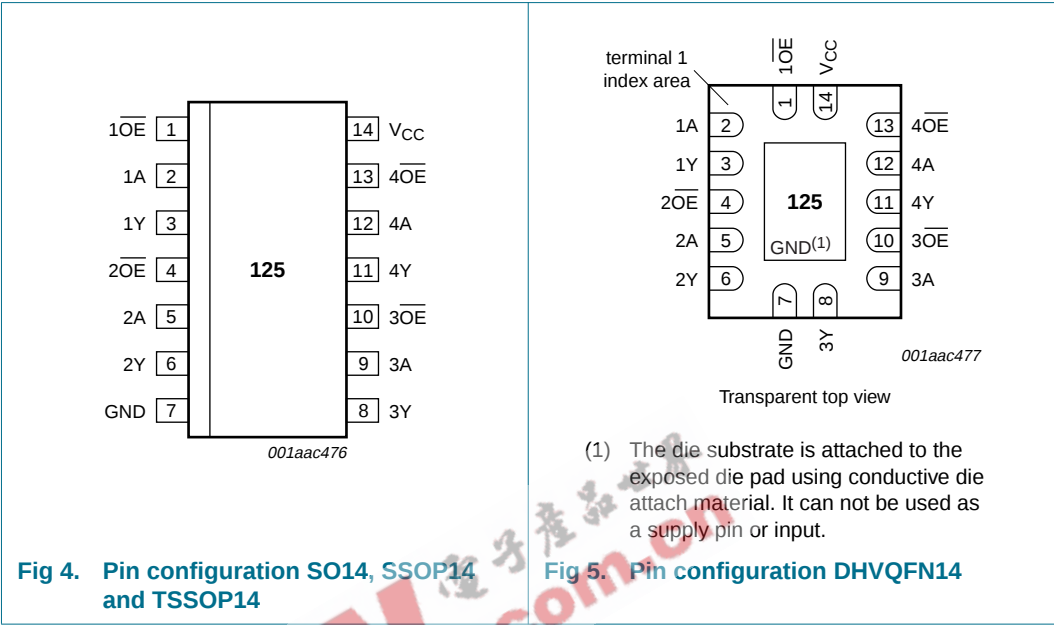
Type number	Package			
	Temperature range	Name	Description	Version
74LVT125D	−40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVT125DB	−40 °C to +85 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LVT125PW	−40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVT125BQ	−40 °C to +85 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 leads terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

5. Functional diagram



6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
1OE	1	1 output enable input (active LOW)
1A	2	1 data input
1Y	3	1 data output
2OE	4	2 output enable input (active LOW)
2A	5	2 data input
2Y	6	2 data output
GND	7	ground (0 V)
3Y	8	3 data output
3A	9	3 data input
3OE	10	3 output enable input (active LOW)
4Y	11	4 data output
4A	12	4 data input
4OE	13	4 output enable input (active LOW)
VCC	14	supply voltage

7. Functional description

7.1 Function table

Table 4: Function table ^[1]

Input		Output
nOE	nA	nY
L	L	L
L	H	H
H	X	Z

- [1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care;
 Z = high-impedance OFF-state.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
V _I	input voltage		^[1] -0.5	+7.0	V
V _O	output voltage	output in OFF-state or HIGH-state	^[1] -0.5	+7.0	V
I _{IK}	input diode current	V _I < 0 V	-	-50	mA
I _{OK}	output diode current	V _O < 0 V	-	-50	mA
I _O	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-	-64	mA
T _{stg}	storage temperature		-65	+150	°C
T _j	junction temperature		^[2] -	150	°C

- [1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
- [2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.7	-	3.6	V
V_I	input voltage		0	-	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		-	-	-32	mA
I_{OL}	LOW-level output current	none	-	-	32	mA
		current duty cycle $\leq 50\%$; $f \geq 1$ kHz	-	-	64	mA
$\Delta t/\Delta V$	input transition rise or fall rate		0	-	10	ns/V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C

10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = -40\text{ °C to }+85\text{ °C}$ [1]						
V_{IK}	input diode voltage	$I_{IK} = -18\text{ mA}$; $V_{CC} = 2.7\text{ V}$	-	-0.9	-1.2	V
V_{OH}	HIGH-level output voltage	$I_{OH} = -100\text{ }\mu\text{A}$; $V_{CC} = 2.7\text{ V to }3.6\text{ V}$;	$V_{CC} - 0.2$	$V_{CC} - 0.1$	-	V
		$I_{OH} = -8\text{ mA}$; $V_{CC} = 2.7\text{ V}$	2.4	2.5	-	V
		$I_{OH} = -32\text{ mA}$; $V_{CC} = 3.0\text{ V}$	2.0	2.2	-	V
V_{OL}	LOW-level output voltage	$V_{CC} = 2.7\text{ V}$				
		$I_{OL} = 100\text{ }\mu\text{A}$	-	0.1	0.2	V
		$I_{OL} = 24\text{ mA}$	-	0.3	0.5	V
		$V_{CC} = 3.0\text{ V}$				
		$I_{OL} = 16\text{ mA}$	-	0.25	0.4	V
I_{LI}	input leakage current	$I_{OL} = 32\text{ mA}$	-	0.3	0.5	V
		$I_{OL} = 64\text{ mA}$	-	0.4	0.55	V
I_{OFF}	power-down output current	$V_{CC} = 0\text{ V}$ or 3.6 V ; $V_I = 5.5\text{ V}$	-	1	10	μA
		$V_{CC} = 3.6\text{ V}$; V_{CC} or GND	-	± 0.1	± 1	μA
		$V_{CC} = 3.6\text{ V}$; $V_I = V_{CC}$	[2] -	0.1	1	μA
		$V_{CC} = 3.6\text{ V}$; $V_I = 0\text{ V}$	[2] -	-1	-5	μA
I_{HOLD}	bus hold current nA input	$V_{CC} = 0\text{ V}$; V_I or $V_O = 0\text{ V to }4.5\text{ V}$	-	1	± 100	μA
		$V_{CC} = 3\text{ V}$; $V_I = 0.8\text{ V}$	[3] 75	150	-	μA
		$V_{CC} = 3\text{ V}$; $V_I = 2.0\text{ V}$	-75	-150	-	μA
		$V_{CC} = 0\text{ V to }3.6\text{ V}$; $V_I = 3.6\text{ V}$	± 500	-	-	μA

Table 7: Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{EX}	external current into output	output in HIGH-state when $V_O > V_{CC}$; $V_O = 5.5$ V and $V_{CC} = 3.0$ V	-	60	125	μ A
I_{PU}, I_{PD}	power-up or power-down 3-state output current	$V_{CC} \leq 1.2$ V; $V_O = 0.5$ V to V_{CC} ; $V_I = \text{GND or } V_{CC}$; $n\overline{OE} = \text{don't care}$	[4] -	± 1	± 100	μ A
I_{OZ}	3-state output current	$V_{CC} = 3.6$ V; $V_I = V_{IH}$ or V_{IL}				
		output HIGH: $V_O = 3.0$ V	-	1	5	μ A
		output LOW: $V_O = 0.5$ V	-	-1	-5	μ A
I_{CC}	quiescent supply current	$V_{CC} = 3.6$ V; $V_I = \text{GND or } V_{CC}$; $I_O = 0$ A				
		outputs HIGH	-	0.13	0.19	mA
		outputs LOW	-	2	7	mA
		outputs disabled	[5] -	0.13	0.19	mA
ΔI_{CC}	additional supply current per input pin	$V_{CC} = 3$ V to 3.6 V; one input at $V_{CC} - 0.6$ V and other inputs at V_{CC} or GND;	[6] -	0.1	0.2	mA
C_I	input capacitance	$V_I = 0$ V or 3.0 V	-	4	-	pF
C_O	output capacitance	outputs disabled; $V_O = 0$ V or 3.0 V	-	8	-	pF

[1] Typical values are measured at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C.[2] Unused pins at V_{CC} or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From $V_{CC} = 1.2$ V to $V_{CC} = 3.3$ V ± 0.3 V a transition time of 100 μ s is permitted. This parameter is valid for $T_{amb} = 25$ °C only.[5] I_{CC} is measured with outputs pulled to V_{CC} or GND.[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

11. Dynamic characteristics

Table 8: Dynamic characteristicsGND = 0 V; $t_r = t_f = 2.5$ ns; $C_L = 50$ pF; $R_L = 500$ Ω ; for test circuit see Figure 8.

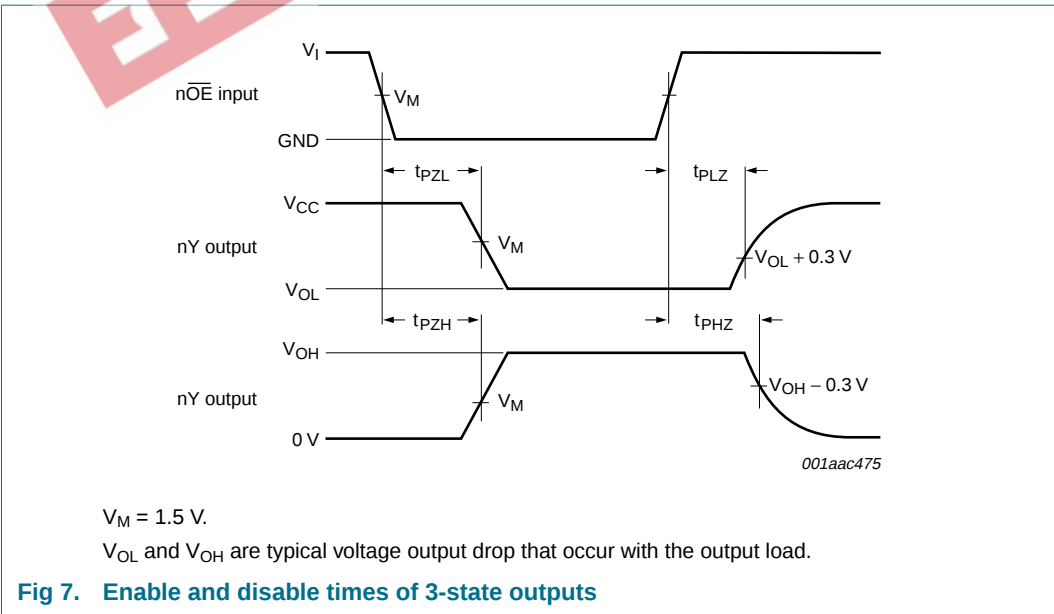
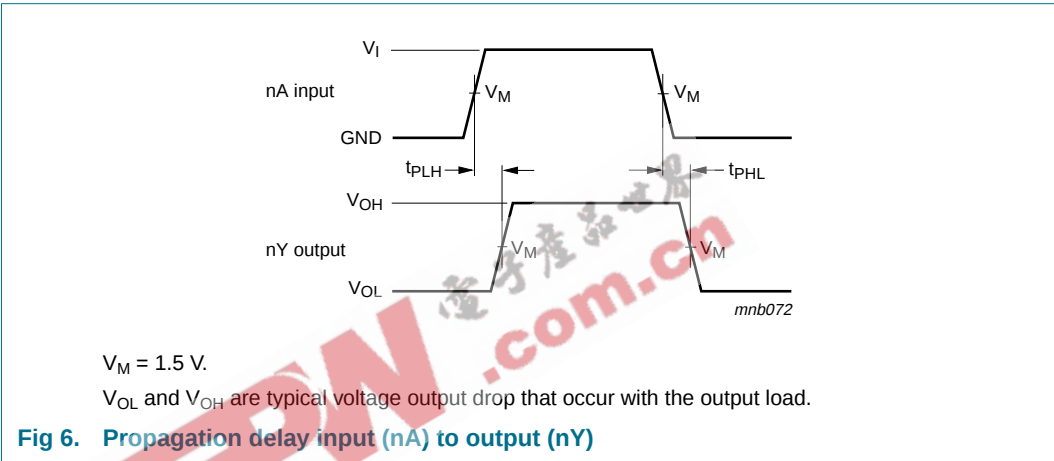
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = -40$ °C to $+85$ °C [1]						
t_{PLH}	propagation delay nA to nY	$V_{CC} = 2.7$ V	-	-	4.5	ns
		$V_{CC} = 3.3$ V ± 0.3 V	1.0	2.7	4.0	ns
t_{PHL}	propagation delay nA to nY	$V_{CC} = 2.7$ V	-	-	4.9	ns
		$V_{CC} = 3.3$ V ± 0.3 V	1.0	2.9	3.9	ns
t_{PZH}	output enable time $n\overline{OE}$ to nY	$V_{CC} = 2.7$ V	-	-	6.0	ns
		$V_{CC} = 3.3$ V ± 0.3 V	1.0	3.4	4.7	ns
t_{PZL}	output enable time $n\overline{OE}$ to nY	$V_{CC} = 2.7$ V	-	-	6.5	ns
		$V_{CC} = 3.3$ V ± 0.3 V	1.1	3.4	4.7	ns

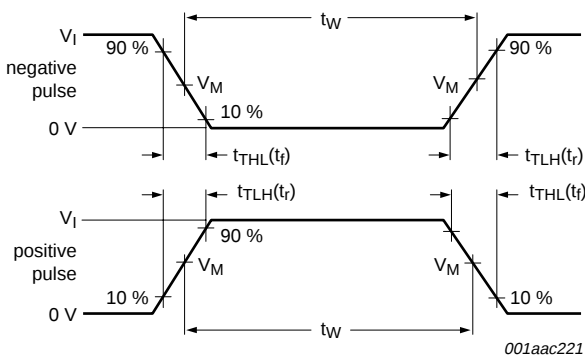
Table 8: Dynamic characteristics ...continued
GND = 0 V; $t_r = t_f = 2.5$ ns; $C_L = 50$ pF; $R_L = 500$ Ω ; for test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHZ}	output disable time $\overline{nOE}$ to nY	$V_{CC} = 2.7$ V	-	-	5.7	ns
		$V_{CC} = 3.3$ V ± 0.3 V	1.8	3.7	5.1	ns
t_{PLZ}	output disable time $\overline{nOE}$ to nY	$V_{CC} = 2.7$ V	-	-	4.0	ns
		$V_{CC} = 3.3$ V ± 0.3 V	1.3	2.6	4.5	ns

[1] Typical values are at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C.

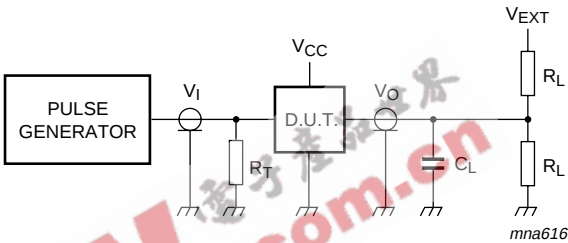
12. Waveforms





$V_M = 1.5\text{ V}$.

a. Input pulse definition



Test data is given in [Table 9](#).
Definitions test circuit:
 R_L = Load resistor.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.
 V_{EXT} = Test voltage for switching times.

b. Test circuit

Fig 8. Load circuitry for switching times

Table 9: Test data

Input				Load		V_{EXT}		
V_I	f_i	t_w	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	$\leq 10\text{ MHz}$	500 ns	$\leq 2.5\text{ ns}$	50 pF	500 Ω	GND	6 V	open

13. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

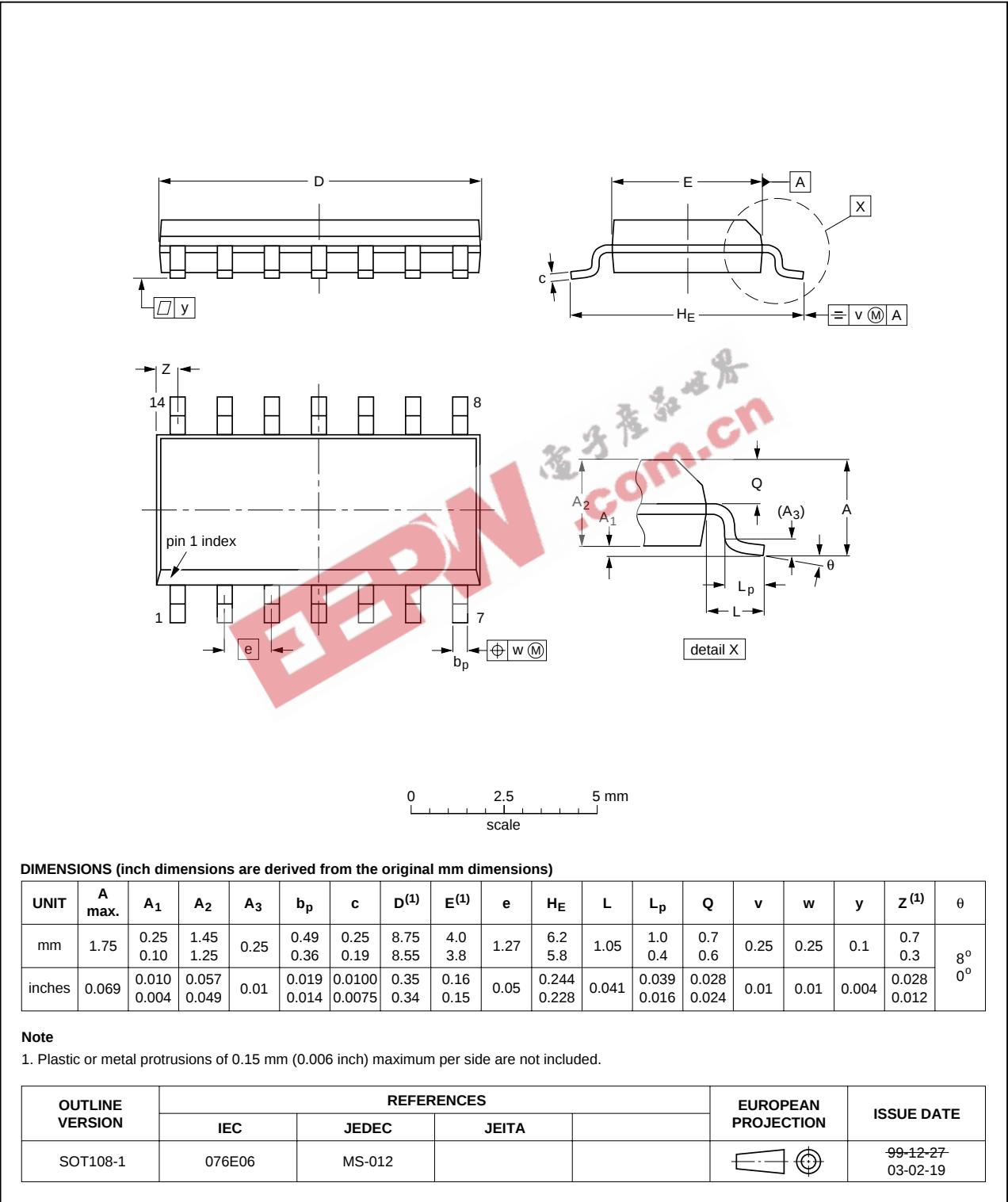


Fig 9. Package outline SO14 (SOT108-1)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

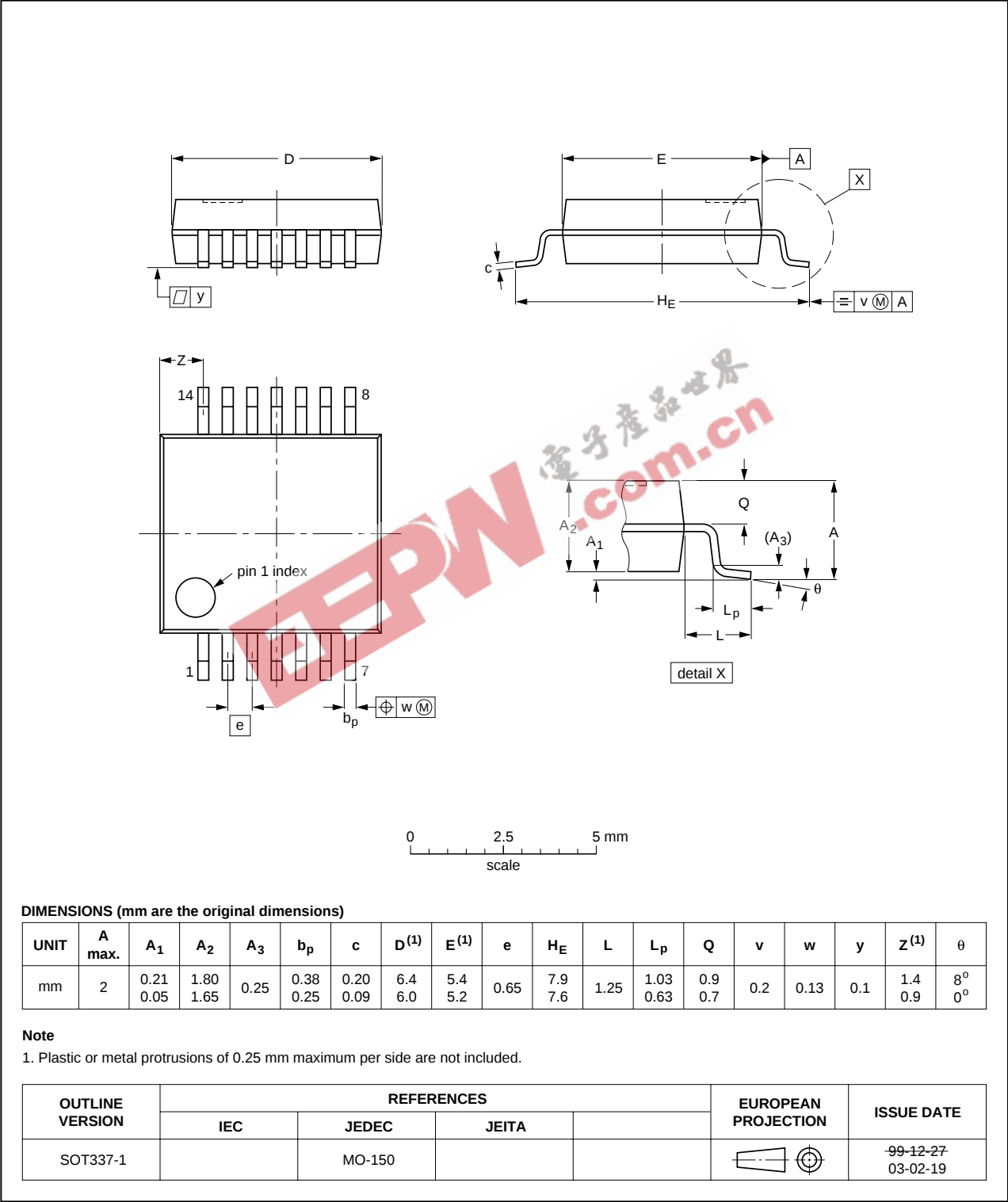


Fig 10. Package outline SSOP14 (SOT337-1)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

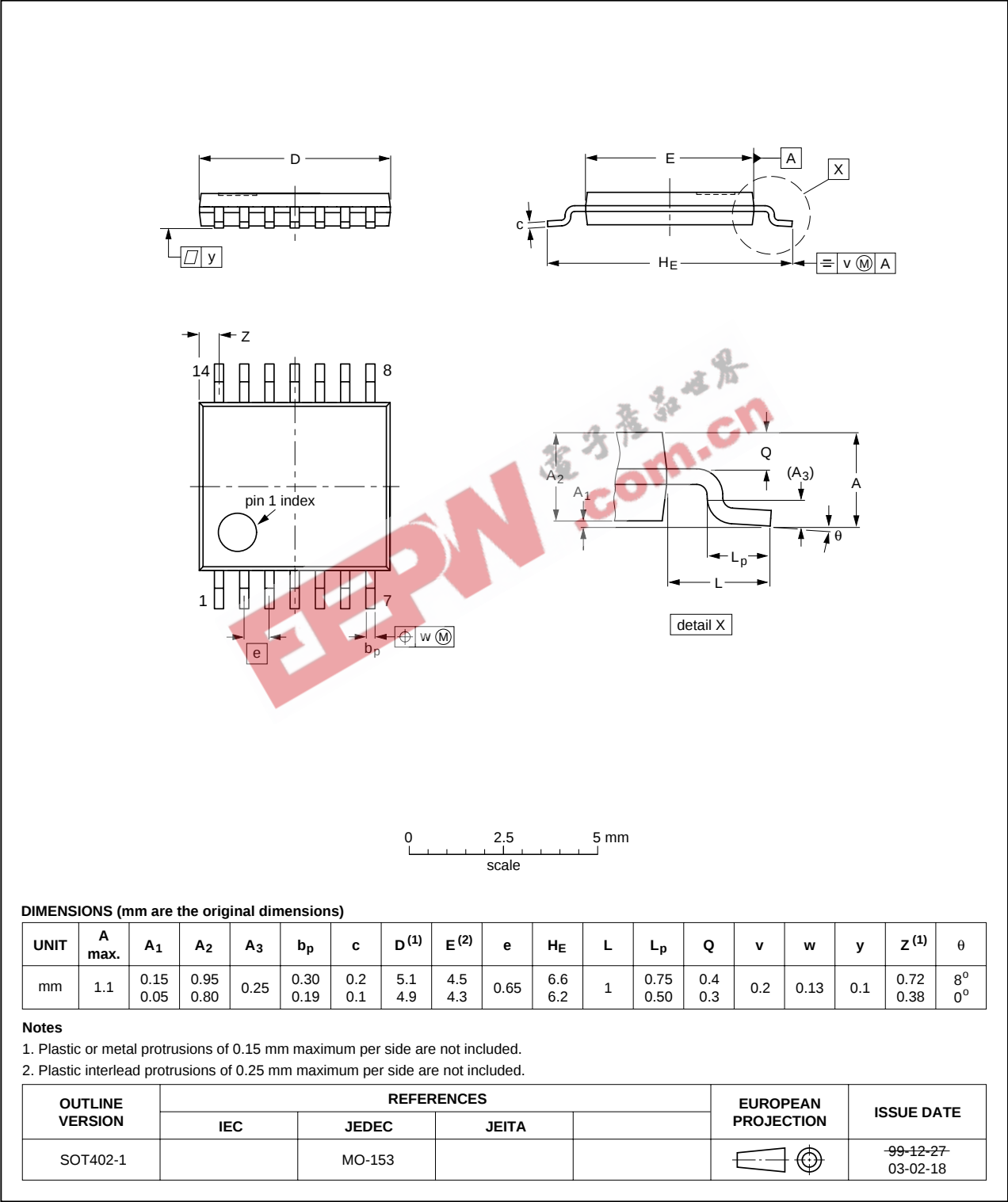


Fig 11. Package outline TSSOP14 (SOT402-1)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm SOT762-1

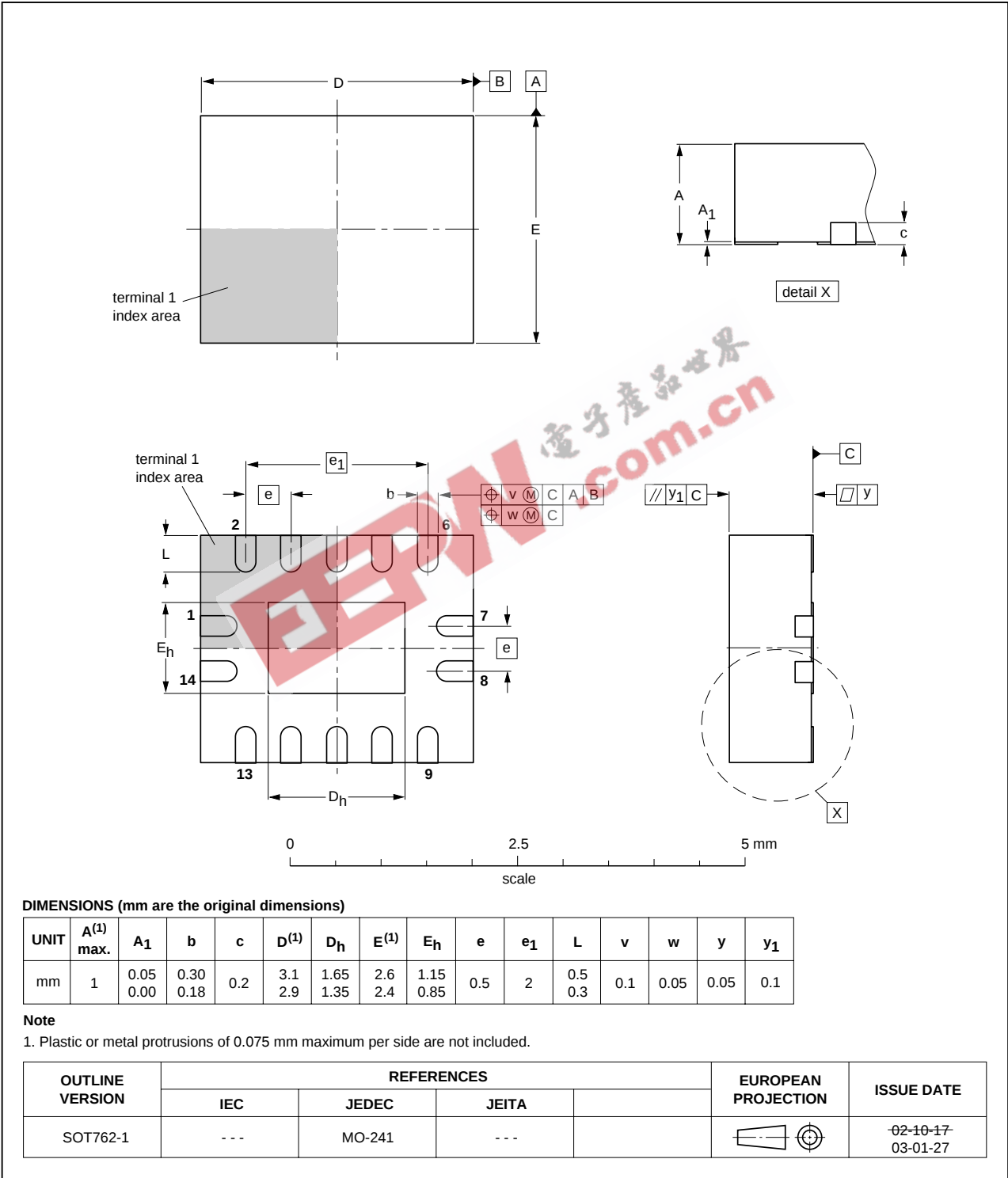


Fig 12. Package outline DHVQFN14 (SOT762-1)



14. Revision history

Table 10: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74LVT125_5	20050210	Product data sheet	-	9397 750 14703	74LVT125_4
Modifications: • Table 2: Corrected type number					
74LVT125_4	20050207	Product data sheet	-	9397 750 14552	74LVT125_3
74LVT125_3	20040624	Product data sheet	-	9397 750 13535	74LVT125_2
74LVT125_2	19980219	Product specification	-	9397 750 03514	74LVT125_1
74LVT125_1	-	-	-	-	-



15. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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