FAIRCHILD
SEMICONDUCTOR™

June 1993
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74LVX574
Low Voltage Octal D-Type Flip-Flop with 3-STATE Outputs

General Description

The LVX574 is a high-speed octal D-type flip-flop which is controlled by an edge-triggered clock input (CP) and a buffered common Output Enable ($\overline{OE}$) input. When the $\overline{OE}$ input is HIGH, the eight outputs are in a high impedance state. The LVX574 is functionally identical to the LVX374 but with inputs and outputs on opposite sides of the package. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

Features

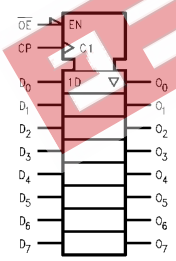
- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Ordering Code:

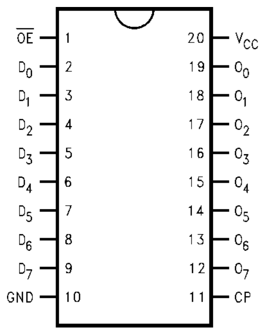
Order Number	Package Number	Package Description
74LVX574M	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300” Wide
74LVX574SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVX574MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	3-STATE Output Enable Input
O_0–O_7	3-STATE Outputs

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Functional Description

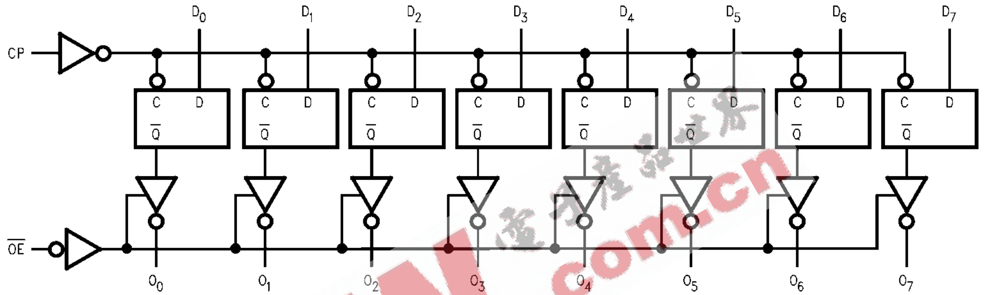
The LVX574 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H	↗	L	H
L	↗	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↗ = LOW-to-HIGH Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
DC Input Voltage (V_I)	−0.5V to 7V
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source	
or Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current	
(I_{CC} or I_{GND})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation	180 mW

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time (Δt/ΔV)	0 ns/V to 100 ns/V

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	HIGH Level	2.0	1.5			1.5				
	Input Voltage	3.0	2.0			2.0		V		
		3.6	2.4			2.4				
V_{IL}	LOW Level	2.0			0.5		0.5			
	Input Voltage	3.0			0.8		0.8	V		
		3.6			0.8		0.8			
V_{OH}	HIGH Level	2.0	1.9	2.0		1.9			$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\ \mu A$
	Output Voltage	3.0	2.9	3.0		2.9		V		$I_{OH} = -50\ \mu A$
		3.0	2.58			2.48				$I_{OH} = -4$ mA
V_{OL}	LOW Level	2.0		0.0	0.1		0.1		$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\ \mu A$
	Output Voltage	3.0		0.0	0.1		0.1	V		$I_{OL} = 50\ \mu A$
		3.0			0.36		0.44			$I_{OL} = 4$ mA
I_{OZ}	3-STATE Output	3.6			±0.25		±2.5	μA	$V_{IN} = V_{IH}$ or V_{IL}	
	Off-State Current								$V_{OUT} = V_{CC}$ or GND	
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	3.6			4.0		40.0	μA	$V_{IN} = V_{CC}$ or GND	

Noise Characteristics (Note 3)

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$		Units	C_L (pF)
			Typ	Limit		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.5	0.8	V	50
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.5	−0.8	V	50
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	3.3		2.0	V	50
V_{ILD}	Maximum LOW Level Dynamic Input Voltage	3.3		0.8	V	50

Note 3: (Input $t_r = t_f = 3$ ns)

AC Electrical Characteristics (Note 4)

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Min	$T_A = +25°C$ Typ	$T_A = +25°C$ Max	$T_A = -40°C$ to $+85°C$ Min	$T_A = -40°C$ to $+85°C$ Max	Units	Conditions
f_{MAX}	Maximum	2.7	60	115		50		MHZ	$C_L = 15$ pF
	Clock		45	60		40			$C_L = 50$ pF
	Frequency	3.3 ± 0.3	80	125		65			$C_L = 15$ pF
			50	75		45			$C_L = 50$ pF
t_{PLH}	Propagation	2.7		9.2	14.5	1.0	17.5	ns	$C_L = 15$ pF
t_{PHL}	Delay Time			11.5	18.0	1.0	21.0		$C_L = 50$ pF
	CP to O_n	3.3 ± 0.3		8.5	13.2	1.0	15.5		$C_L = 15$ pF
				11.0	16.7	1.0	19.0		$C_L = 50$ pF
t_{PZL}	3-STATE Output	2.7		9.8	15.0	1.0	18.5	ns	$C_L = 15$ pF, $R_L = 1$ kΩ
t_{PZH}	Enable Time			11.4	18.5	1.0	22.0		$C_L = 50$ pF, $R_L = 1$ kΩ
		3.3 ± 0.3		8.2	12.8	1.0	15.0		$C_L = 15$ pF, $R_L = 1$ kΩ
				10.7	16.3	1.0	18.5		$C_L = 50$ pF, $R_L = 1$ kΩ
t_{PLZ} t_{PHZ}	3-STATE Output	2.7		12.1	19.1	1.0	22.0	ns	$C_L = 50$ pF, $R_L = 1$ kΩ
	Disable Time	3.3 ± 0.3		11.0	15.0	1.0	17.0		$C_L = 50$ pF, $R_L = 1$ kΩ
t_W	CP Pulse	2.7	6.5			7.5		ns	
	Width	3.3 ± 0.3	5.0			5.0			
t_S	Setup Time	2.7	5.0			5.0		ns	
	D_n to CP	3.3 ± 0.3	3.5			3.5			
t_H	Hold Time	2.7	1.5			1.5		ns	
	D_n to CP	3.3 ± 0.3	1.5			1.5			
t_{OSHL}	Output to Output	2.7			1.5		1.5	ns	$C_L = 50$ pF
t_{OSLH}	Skew (Note 4)	3.3			1.5		1.5		

Note 4: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.

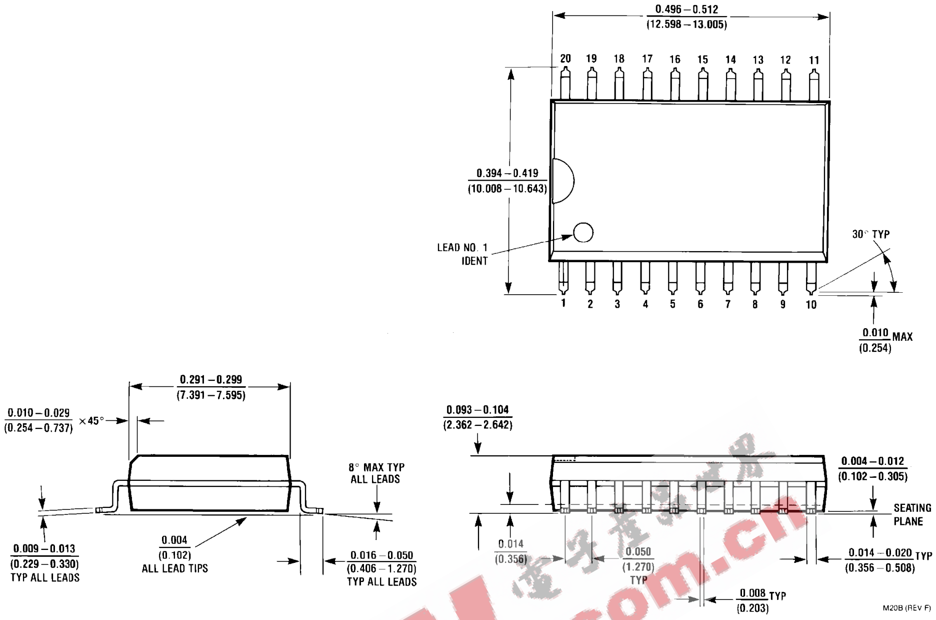
Capacitance

Symbol	Parameter	$T_A = +25°C$ Min	$T_A = +25°C$ Typ	$T_A = +25°C$ Max	$T_A = -40°C$ to $+85°C$ Min	$T_A = -40°C$ to $+85°C$ Max	Units
C_{IN}	Input Capacitance		4	10		10	pF
C_{OUT}	Output Capacitance		6				pF
C_{PD}	Power Dissipation Capacitance (Note 5)		27				pF

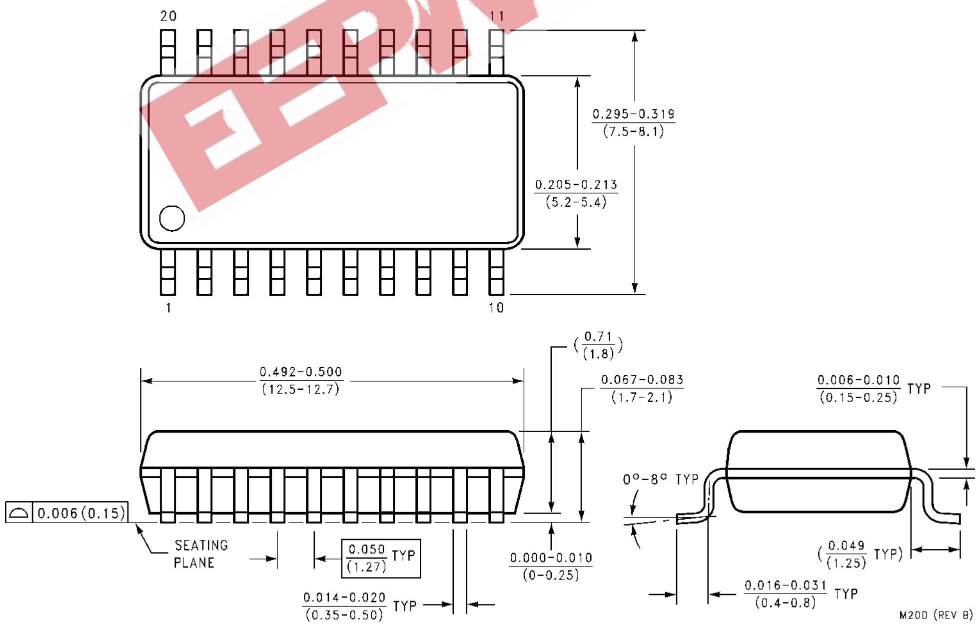
Note 5: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{8 \text{ (per latch)}}$

Physical Dimensions inches (millimeters) unless otherwise noted

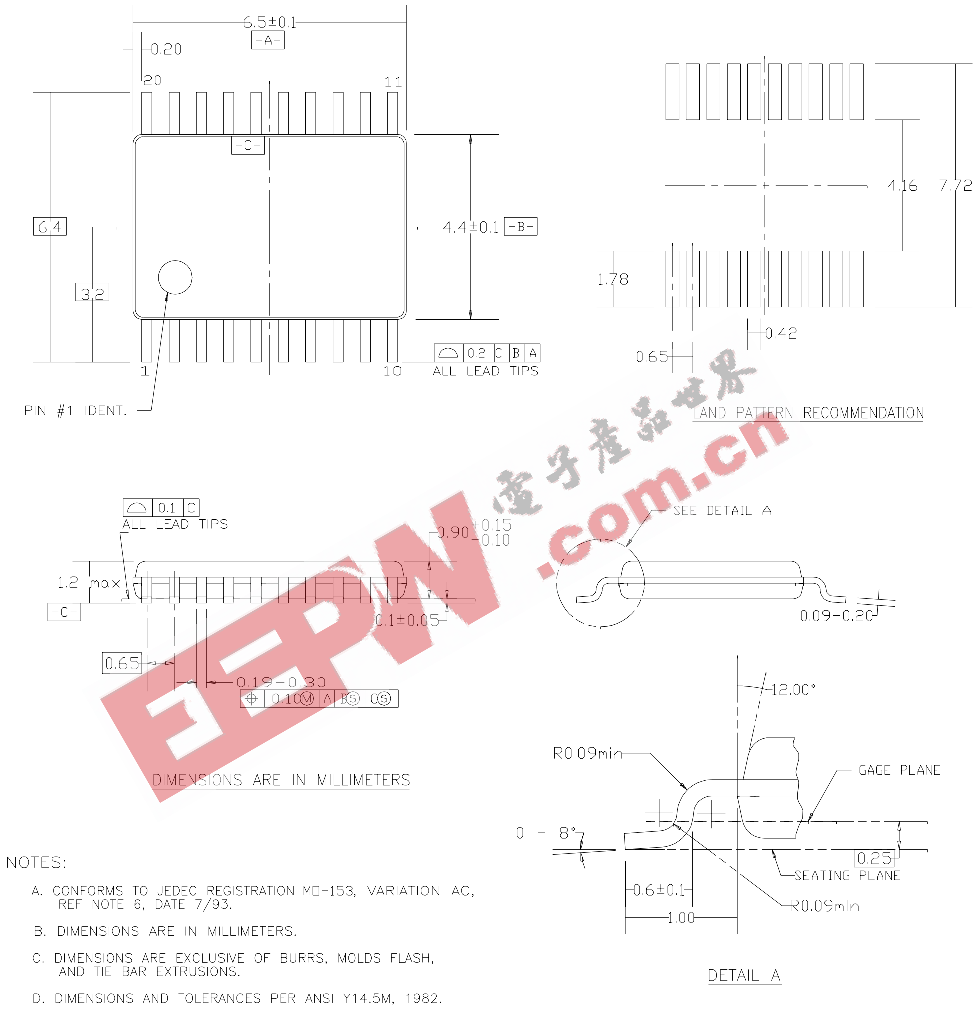


20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B



20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20