

Octal D-type flip-flop; positive-edge trigger (3-State)

74ABT374A

FEATURES

- 8-bit positive edge triggered register
- 3-State output buffers
- Output capability: +64mA/−32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Power-up reset
- Live insertion/extraction permitted

DESCRIPTION

The 74ABT374A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT374A is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable (\overline{OE}) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable (OE) controls all eight 3-State buffers independent of the clock operation.

When \overline{OE} is Low, the stored data appears at the outputs. When \overline{OE} is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

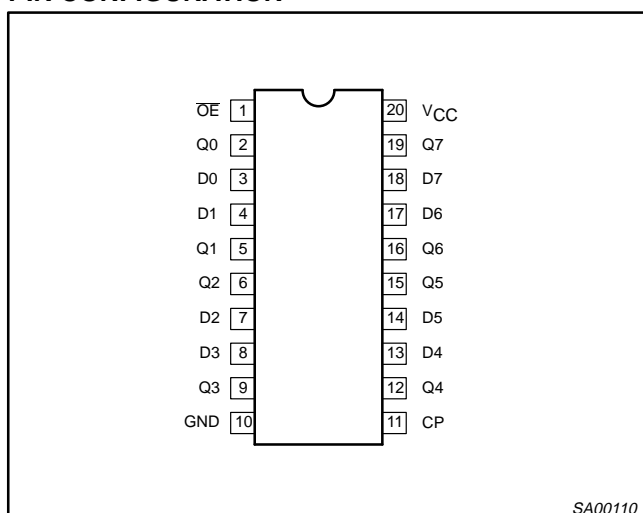
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	$C_L = 50\text{pF}; V_{CC} = 5\text{V}$	3.4 3.8	ns
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; $V_O = 0\text{V}$ or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; $V_{CC} = 5.5\text{V}$	110	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic DIP	−40°C to +85°C	74ABT374A N	74ABT374A N	SOT146-1
20-Pin plastic SO	−40°C to +85°C	74ABT374A D	74ABT374A D	SOT163-1
20-Pin Plastic SSOP Type II	−40°C to +85°C	74ABT374A DB	74ABT374A DB	SOT339-1
20-Pin Plastic TSSOP Type I	−40°C to +85°C	74ABT374A PW	74ABT374APW DH	SOT360-1

PIN CONFIGURATION



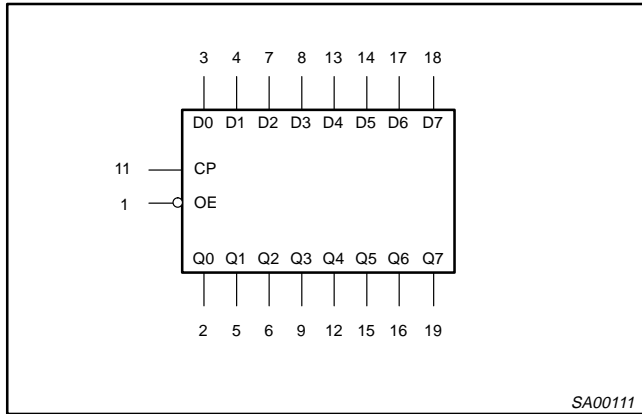
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	OE	Output enable input (active-Low)
3, 4, 7, 8, 13, 14, 17, 18	D0-D7	Data inputs
2, 5, 6, 9, 12, 15, 16, 19	Q0-Q7	Data outputs
11	CP	Clock pulse input (active rising edge)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

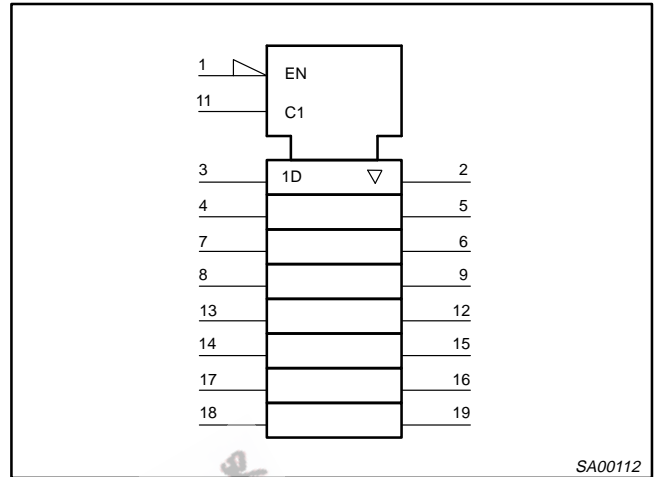
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LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

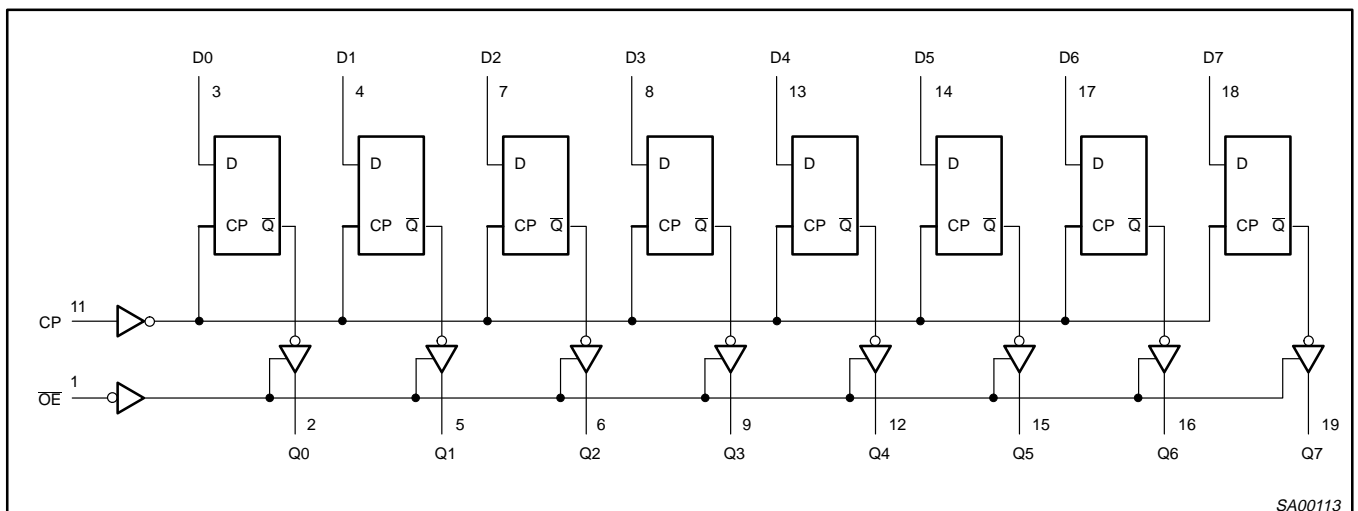


FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
OE	CP	Dn		Q0 – Q7	
L	↑	l	L	L	Latch and read register
L	↑	h	H	H	
L	↕	X	NC	NC	Hold
H	↕	X	NC	Z	Disable outputs
H	↑	Dn	Dn	Z	

H = High voltage level
 h = High voltage level one set-up time prior to the Low-to-High clock transition
 L = Low voltage level
 l = Low voltage level one set-up time prior to the Low-to-High clock transition
 NC= No change
 X = Don't care
 Z = High impedance "off" state
 ↑ = Low-to-High clock transition
 ↕ = not a Low-to-High clock transition

LOGIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage ³		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage ³	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		-32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 4.5V; I _{IK} = -18mA		-0.9	-1.2		-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 4.5V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}	2.5	2.9		2.5		V
		V _{CC} = 5.0V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}	3.0	3.4		3.0		V
		V _{CC} = 4.5V; I _{OH} = -32mA; V _I = V _{IL} or V _{IH}	2.0	2.4		2.0		V
V _{OL}	Low-level output voltage	V _{CC} = 4.5V; I _{OL} = 64mA; V _I = V _{IL} or V _{IH}		0.42	0.55		0.55	V
V _{RST}	Power-up output low voltage ³	V _{CC} = 5.5V; I _O = 1mA; V _I = GND or V _{CC}		0.13	0.55		0.55	V
I _I	Input leakage current	V _{CC} = 5.5V; V _I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I _{OFF}	Power-off leakage current	V _{CC} = 0.0V; V _O or V _I ≤ 4.5V		±5.0	±100		±100	µA
I _{PU} /I _{PD}	Power-up/down 3-State output current	V _{CC} = 0.0V; I _O = 1mA; V _I = GND or V _{CC} ; V _{OE} = Don't Care		±5.0	±50		±50	µA
I _{OZH}	3-State output High current	V _{CC} = 5.5V; V _O = 2.7V; V _I = V _{IL} or V _{IH}		5.0	50		50	µA
I _{OZL}	3-State output Low current	V _{CC} = 5.5V; V _O = 0.5V; V _I = V _{IL} or V _{IH}		-5.0	-50		-50	µA
I _{CEx}	Output High leakage current	V _{CC} = 5.5V; V _O = 0.5V; V _I = GND or V _{CC}		5.0	50		50	µA
I _O	Output current ¹	V _{CC} = 5.5V; V _O = 2.5V	-50	-100	-180	-50	-180	mA
I _{CCH}	Quiescent supply current	V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC}		110	250		250	µA
I _{CCL}		V _{CC} = 5.5V; Outputs Low, V _I = GND or V _{CC}		24	30		30	mA
I _{CCZ}		V _{CC} = 5.5V; Outputs 3-State; V _I = GND or V _{CC}		110	250		250	µA
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 5.5V; one input at 3.4V, other inputs at V _{CC} or GND		0.5	1.5		1.5	mA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

AC CHARACTERISTICS

GND = 0V, t_R = t_F = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V			T _{amb} = -40 to +85°C V _{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
f _{MAX}	Maximum clock frequency	1	200	300		200		ns
t _{PLH} t _{PHL}	Propagation delay CP to Qn	1	1.7 2.0	3.4 3.8	4.5 4.9	1.7 2.0	5.1 5.2	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	3 4	1.2 2.2	3.5 4.3	4.5 5.4	1.2 2.2	5.4 6.2	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	3 4	1.8 1.5	3.6 3.0	4.7 4.1	1.8 1.5	5.2 4.3	ns

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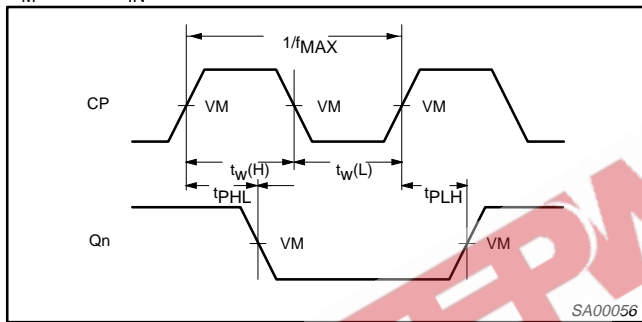
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

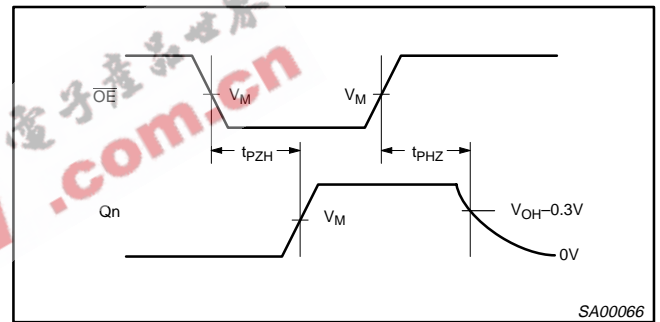
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$		$T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$	
			Min	Typ	Min	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low Dn to CP	2	1.5 1.2	0.6 0.3	1.5 1.2	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low Dn to CP	2	1.0 1.0	-0.3 -0.5	1.0 1.0	ns
$t_w(\text{H})$ $t_w(\text{L})$	CP pulse width High or Low	1	2.0 2.8	0.8 1.0	2.0 2.8	ns

AC WAVEFORMS

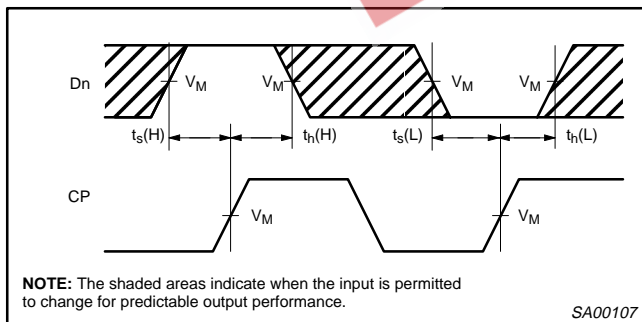
$V_M = 1.5\text{V}$, $V_{\text{IN}} = \text{GND to } 3.0\text{V}$



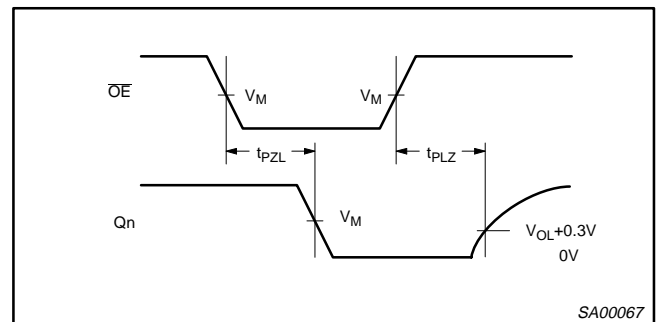
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 2. Data Setup and Hold Times



Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

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TEST CIRCUIT AND WAVEFORM

Test Circuit for 3-State Outputs

Input Pulse Definition

$V_M = 1.5V$

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012