

DATA SHEET

74ABT162827A

74ABTH162827A

20-bit buffer/line driver, non-inverting,
with 30Ω termination resistors (3-State)

Product specification
Supersedes data of 1997 Feb 26
IC23 Data Handbook

1998 Feb 27

20-bit buffer/line driver, non-inverting, with 30Ω termination resistors (3-State)

74ABT162827A 74ABTH162827A

FEATURES

- Multiple V_{CC} and GND pins minimize switching noise
- Live insertion/extraction permitted
- 3-State output buffers
- Power-up 3-State
- 74ABTH162827A incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT162827A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT162827A 20-bit buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. They have NOR Output Enables ($\overline{nOE1}$, $\overline{nOE2}$) for maximum control flexibility.

The 74ABT162827A is designed with 30Ω series resistance in both the pull-up and pull-down output structures. This design reduces line noise in applications such as memory address drivers, clock drivers and bus receivers/transmitters.

Two options are available, 74ABT162827A which does not have the bus-hold feature and 74ABTH162827A which incorporates the bus-hold feature.

QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | UNIT |
|------------------------|-------------------------------------|--|------------|---------------|
| | | $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$ | | |
| t_{PLH} t_{PHL} | Propagation delay nAx to nYx | $C_L = 50\text{pF}; V_{CC} = 5\text{V}$ | 1.8 1.9 | ns |
| C_{IN} | Input capacitance | $V_I = 0\text{V}$ or V_{CC} | 4 | pF |
| C_{OUT} | Output capacitance | $V_O = 0\text{V}$ or V_{CC} ; 3-State | 6 | pF |
| I_{CCZ} | Quiescent supply current | Outputs disabled; $V_{CC} = 5.5\text{V}$ | 500 | μA |
| I_{CCL} | | Outputs Low; $V_{CC} = 5.5\text{V}$ | 9 | mA |

ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | DWG NUMBER |
|------------------------------|-------------------|-----------------------|---------------|------------|
| 56-Pin Plastic SSOP Type III | -40°C to +85°C | 74ABT162827A DL | BT162827A DL | SOT371-1 |
| 56-Pin Plastic TSSOP Type II | -40°C to +85°C | 74ABT162827A DGG | BT162827A DGG | SOT364-1 |
| 56-Pin Plastic SSOP Type III | -40°C to +85°C | 74ABTH162827A DL | BH162827A DL | SOT371-1 |
| 56-Pin Plastic TSSOP Type II | -40°C to +85°C | 74ABTH162827A DGG | BH162827A DGG | SOT364-1 |

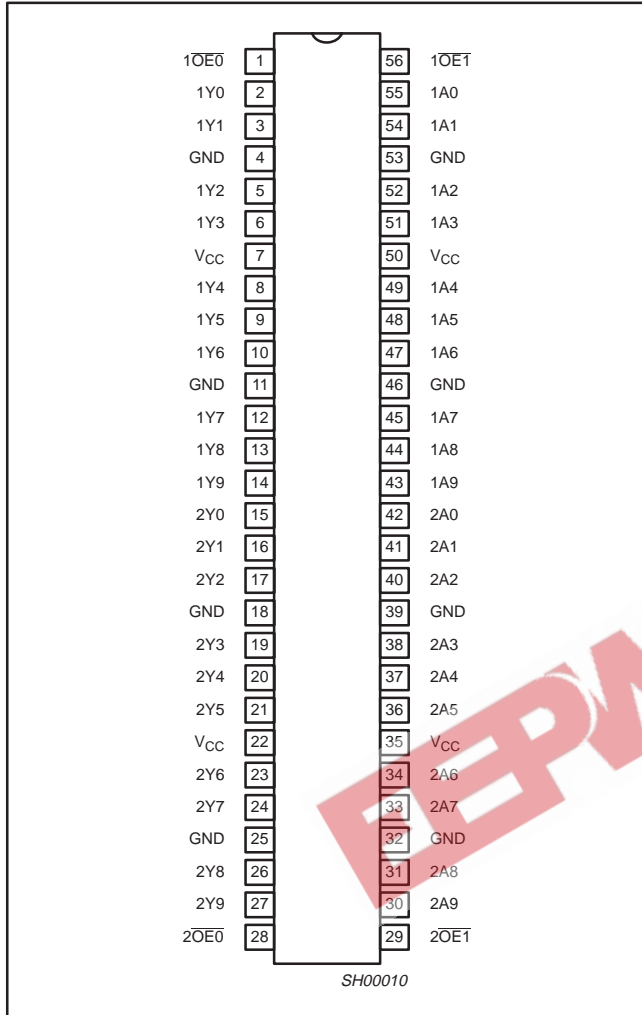
PIN DESCRIPTION

| PIN NUMBER | SYMBOL | FUNCTION |
|---|--|-----------------------------------|
| 55, 54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31, 30 | 1A0 - 1A9 2A0 - 2A9 | Data inputs |
| 2, 3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26, 27 | 1Y0 - 1Y9 2Y0 - 2Y9 | Data outputs |
| 1, 56, 28, 29 | $1\overline{OE}0$, $1\overline{OE}1$ $2\overline{OE}0$, $2\overline{OE}1$ | Output enable inputs (active-Low) |
| 4, 11, 18, 25, 32, 39, 46, 53 | GND | Ground (0V) |
| 7, 22, 35, 50 | V_{CC} | Positive supply voltage |

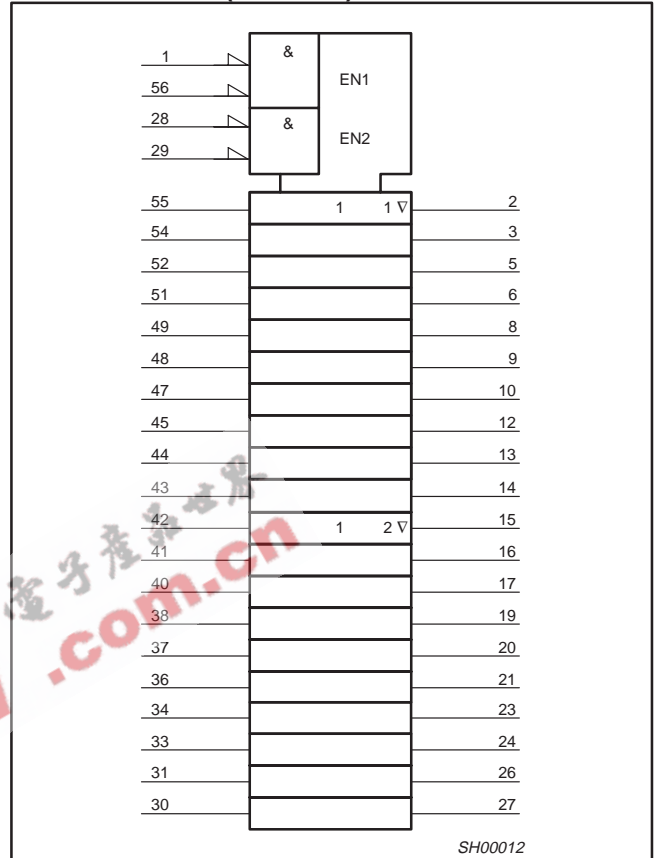
20-bit buffer/line driver, non-inverting,
with 30Ω termination resistors (3-State)

74ABT162827A
74ABTH162827A

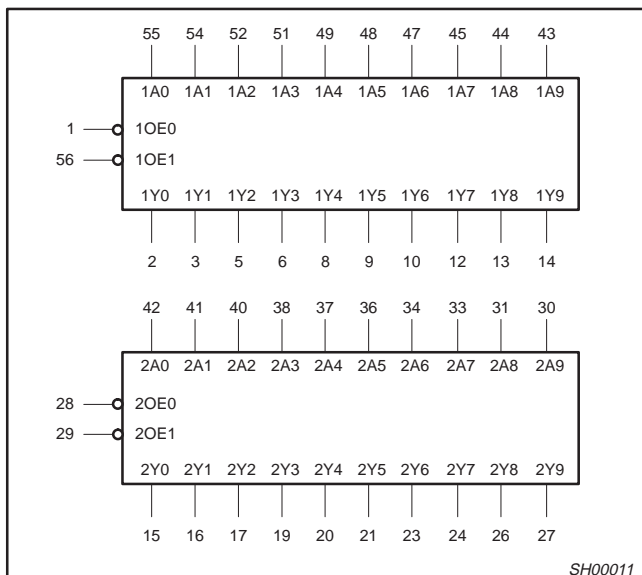
PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



FUNCTION TABLE

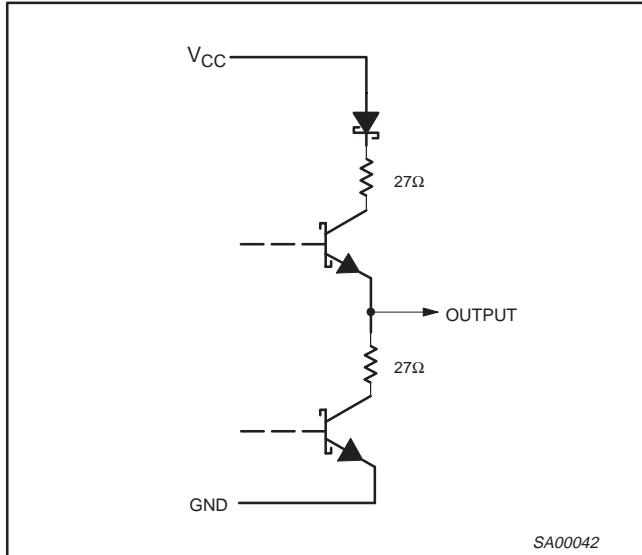
| INPUTS | | OUTPUTS | OPERATING MODE |
|------------------|-----------------|-----------------|----------------|
| nOE _x | nA _x | nY _x | |
| L | L | L | Transparent |
| L | H | H | Transparent |
| H | X | Z | High impedance |

- X = Don't care
- Z = High impedance "off" state
- H = High voltage level
- L = Low voltage level

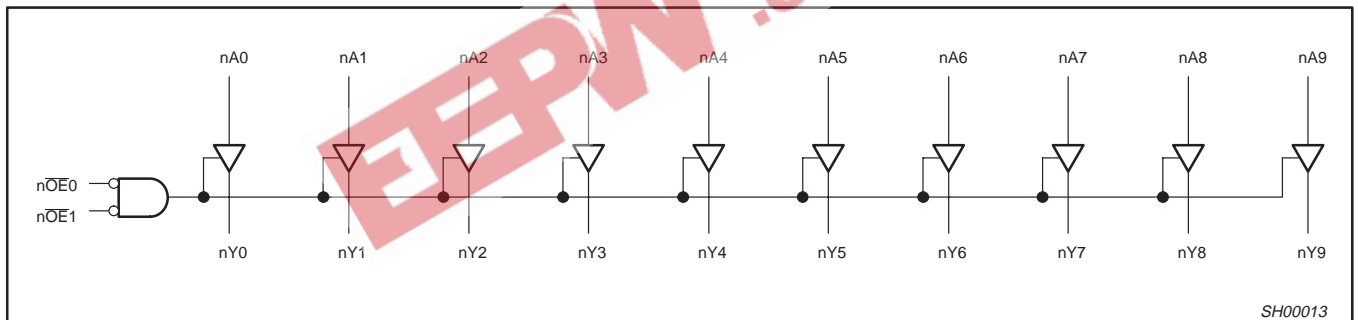
20-bit buffer/line driver, non-inverting,
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SCHEMATIC OF Y OUTPUTS



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS^{1, 2}

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|-----------|--------------------------------|-----------------------------|--------------|------|
| V_{CC} | DC supply voltage | | -0.5 to +7.0 | V |
| I_{IK} | DC input diode current | $V_I < 0$ | -18 | mA |
| V_I | DC input voltage ³ | | -1.2 to +7.0 | V |
| I_{OK} | DC output diode current | $V_O < 0$ | -50 | mA |
| V_{OUT} | DC output voltage ³ | Output in Off or High state | -0.5 to +5.5 | V |
| I_{OUT} | DC output current | Output in Low state | 128 | mA |
| | | Output in High state | -64 | mA |
| T_{stg} | Storage temperature range | | -65 to 150 | °C |

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

20-bit buffer/line driver, non-inverting, with 30Ω termination resistors (3-State)

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RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | UNIT |
|------------------|--------------------------------------|--------|-----------------|------|
| | | MIN | MAX | |
| V _{CC} | DC supply voltage | 4.5 | 5.5 | V |
| V _I | Input voltage | 0 | V _{CC} | V |
| V _{IH} | High-level input voltage | 2.0 | | V |
| V _{IL} | Low-level Input voltage | | 0.8 | V |
| I _{OH} | High-level output current | | -32 | mA |
| I _{OL} | Low-level output current | | 12 | mA |
| Δt/Δv | Input transition rise or fall rate | 0 | 10 | ns/V |
| T _{amb} | Operating free-air temperature range | -40 | +85 | °C |

DC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | | | UNIT |
|----------------------------------|---|---|--------------------------|------|------|-----------------------------------|------|------|
| | | | T _{amb} = +25°C | | | T _{amb} = -40°C to +85°C | | |
| | | | MIN | TYP | MAX | MIN | MAX | |
| V _{IK} | Input clamp voltage | V _{CC} = 4.5V; I _{IK} = -18mA | -0.9 | -1.2 | | -1.2 | V | |
| V _{OH} | High-level output voltage | V _{CC} = 4.5V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH} | 2.5 | 3.1 | | 2.5 | V | |
| | | V _{CC} = 5.0V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH} | 3.0 | 3.6 | | 3.0 | V | |
| | | V _{CC} = 4.5V; I _{OH} = -32mA; V _I = V _{IL} or V _{IH} | 2.0 | 2.7 | | 2.0 | V | |
| V _{OL} | Low-level output voltage | V _{CC} = 4.5V; I _{OH} = 8mA; V _I = V _{IL} or V _{IN} | | | 0.65 | 0.65 | V | |
| | | V _{CC} = 4.5V; I _{OL} = 12mA; V _I = V _{IL} | | | 0.80 | 0.80 | V | |
| I _I | Input leakage current | V _{CC} = 5.5V; V _I = GND or 5.5V | ±0.01 | ±1.0 | | ±1.0 | μA | |
| I _I | Input leakage current 74ABTH162827A | V _{CC} = 5.5V; V _I = 5.5V | 0.01 | 1 | | 1 | μA | |
| | | V _{CC} = 5.5V; V _I = V _{CC} or GND | ±0.01 | ±1 | | ±1 | μA | |
| | | V _{CC} = 5.5V; V _I = V _{CC} | 0.01 | 1 | | 1 | μA | |
| | | V _{CC} = 5.5V; V _I = 0 | -1 | -3 | | -5 | μA | |
| I _{HOLD} | Bus Hold current A inputs ⁵ 74ABTH162827A | V _{CC} = 4.5V; V _I = 0.8V | 35 | | | 35 | μA | |
| | | V _{CC} = 4.5V; V _I = 2.0V | -75 | | | -75 | | |
| | | V _{CC} = 5.5V; V _I = 0 to 5.5V | ±800 | | | | | |
| I _{OFF} | Power-off leakage current | V _{CC} = 0.0V; V _O = 4.5V; V _I = 0V or 5.5V | ±5.0 | ±100 | | ±100 | μA | |
| I _{PU} /I _{PD} | Power-up/down 3-State output current ³ | V _{CC} = 2.1V; V _O = 0.5V; V _I = GND or V _{CC} ; V _{OE} = Don't care | ±5.0 | ±50 | | ±50 | μA | |
| I _{OZH} | 3-State output High current | V _{CC} = 5.5V; V _O = 2.7V; V _I = V _{IL} or V _{IH} | 1.0 | 10 | | 10 | μA | |
| I _{OZL} | 3-State output Low current | V _{CC} = 5.5V; V _O = 0.5V; V _I = V _{IL} or V _{IH} | -1.0 | -10 | | -10 | μA | |
| I _{CEX} | Output High leakage current | V _{CC} = 5.5V; V _O = 5.5V; V _I = GND or V _{CC} | 1.0 | 50 | | 50 | μA | |
| I _O | Output current ¹ | V _{CC} = 5.5V; V _O = 2.5V | -50 | -70 | -180 | -50 | -180 | mA |
| I _{CCH} | Quiescent supply current | V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC} | 0.5 | 1 | | 1 | mA | |
| I _{CCL} | | V _{CC} = 5.5V; Outputs Low, V _I = GND or V _{CC} | 9 | 19 | | 19 | mA | |
| I _{CCZ} | | V _{CC} = 5.5V; Outputs 3-State; V _I = GND or V _{CC} | 0.5 | 1 | | 1 | mA | |
| ΔI _{CC} | Additional supply current per input pin ² | V _{CC} = 5.5V; one input at 3.4V, other inputs at V _{CC} or GND | 0.2 | 1 | | 1 | mA | |

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100μsec is permitted.
- Unused pins at V_{CC} or GND.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

20-bit buffer/line driver, non-inverting,
with 30Ω termination resistors (3-State)

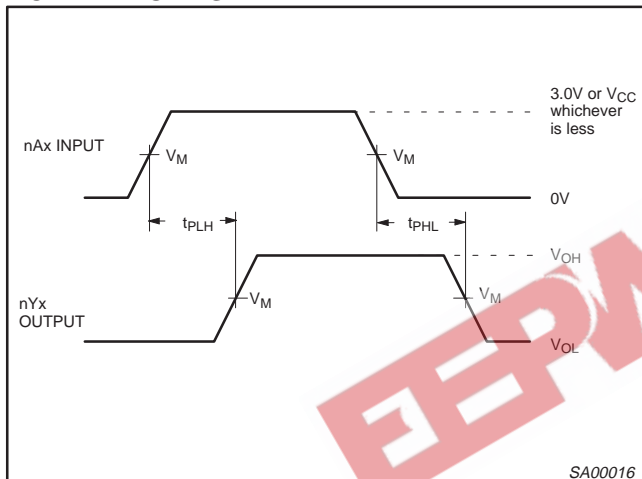
74ABT162827A
74ABTH162827A

AC CHARACTERISTICS

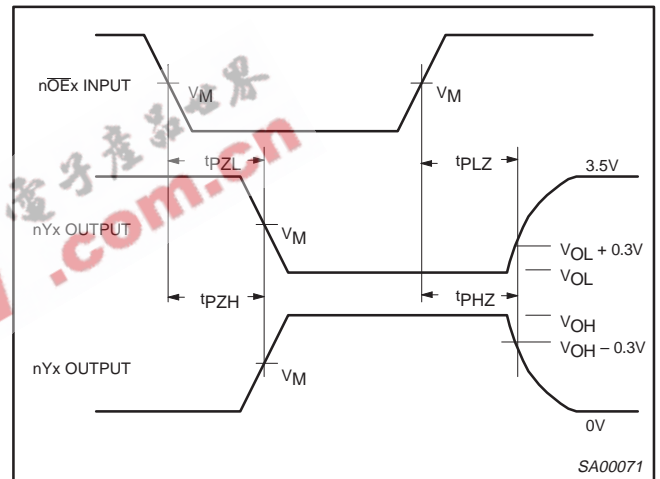
GND = 0V, $t_R = t_F = 2.5ns$, $C_L = 50pF$, $R_L = 500\Omega$

| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | | | UNIT |
|------------------------|--|----------|--|------------|------------|---|------------|------|
| | | | $T_{amb} = +25^{\circ}C$ $V_{CC} = +5.0V$ | | | $T_{amb} = -40$ to $+85^{\circ}C$ $V_{CC} = +5.0V \pm 0.5V$ | | |
| | | | MIN | TYP | MAX | MIN | MAX | |
| t_{PLH} t_{PHL} | Propagation delay nAx to nYx | 1 | 1.0 1.0 | 1.8 1.4 | 2.6 2.6 | 1.0 1.0 | 2.9 2.9 | ns |
| t_{PZH} t_{PZL} | Output enable time to High and Low level | 2 | 1.5 2.0 | 3.0 3.6 | 4.2 4.9 | 1.5 2.0 | 5.2 6.0 | ns |
| t_{PHZ} t_{PLZ} | Output disable time from High and Low level | 2 | 2.0 1.5 | 3.4 2.8 | 4.8 4.0 | 2.0 1.5 | 5.4 4.3 | ns |

AC WAVEFORMS



Waveform 1. Input (nAx) to Output (nYx) Propagation Delays

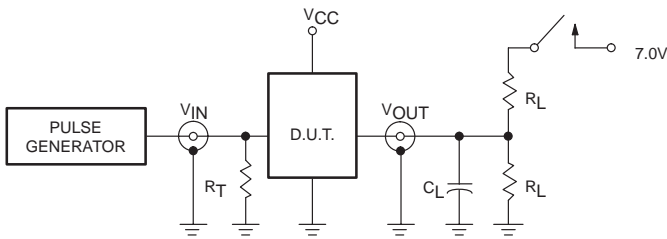


Waveform 2. 3-State Output Enable and Disable Times

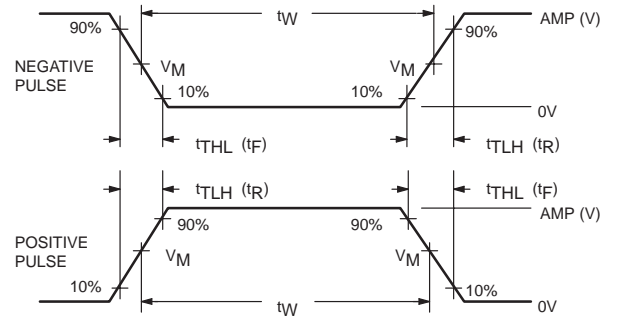
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TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



VM = 1.5V
Input Pulse Definition

SWITCH POSITION

| TEST | SWITCH |
|-----------|--------|
| tPLZ | closed |
| tPZL | closed |
| All other | open |

DEFINITIONS

- RL = Load resistor; see AC CHARACTERISTICS for value.
- CL = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- RT = Termination resistance should be equal to ZOUT of pulse generators.

| FAMILY | INPUT PULSE REQUIREMENTS | | | | |
|-----------|--------------------------|-----------|-------|-------|-------|
| | Amplitude | Rep. Rate | tW | tR | tF |
| 74ABT/H16 | 3.0V | 1MHz | 500ns | 2.5ns | 2.5ns |

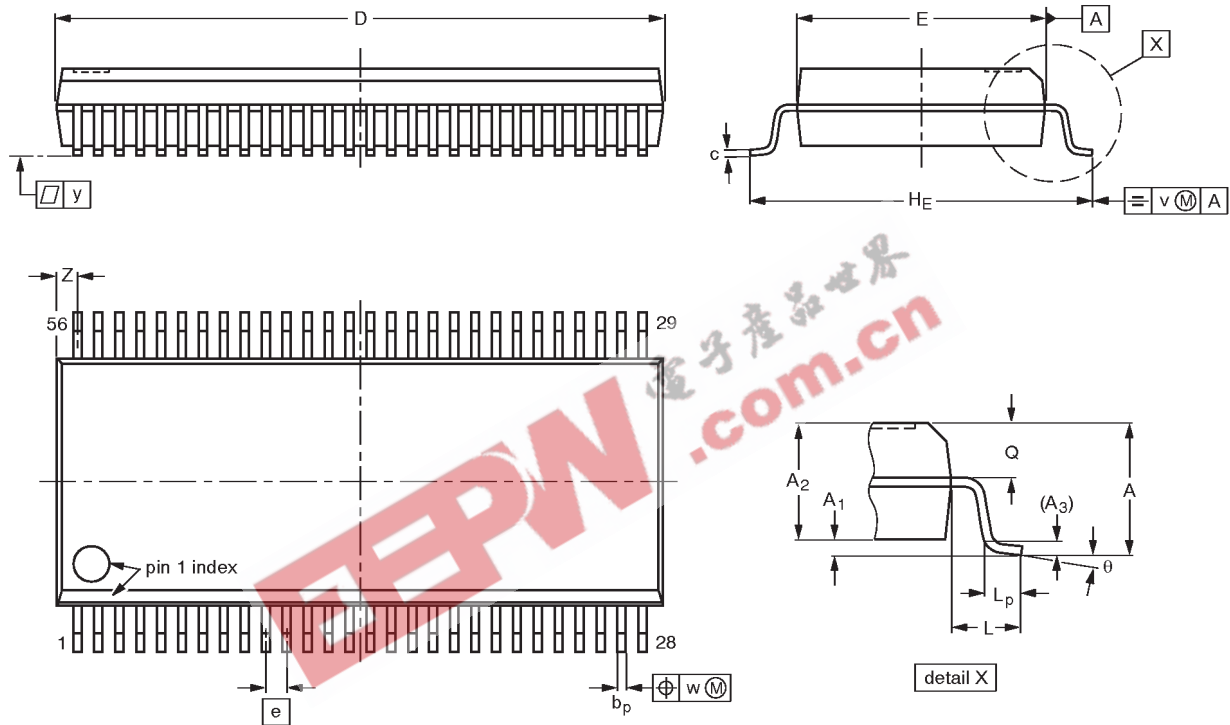
SA00018

20-bit buffer/line driver, non-inverting (3-State)

74ABT16827A
74ABTH16827A

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|-------|----------------|-----|----------------|------------|------|------|-----|------------------|----------|
| mm | 2.8 | 0.4 0.2 | 2.35 2.20 | 0.25 | 0.3 0.2 | 0.22 0.13 | 18.55 18.30 | 7.6 7.4 | 0.635 | 10.4 10.1 | 1.4 | 1.0 0.6 | 1.2 1.0 | 0.25 | 0.18 | 0.1 | 0.85 0.40 | 8° 0° |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

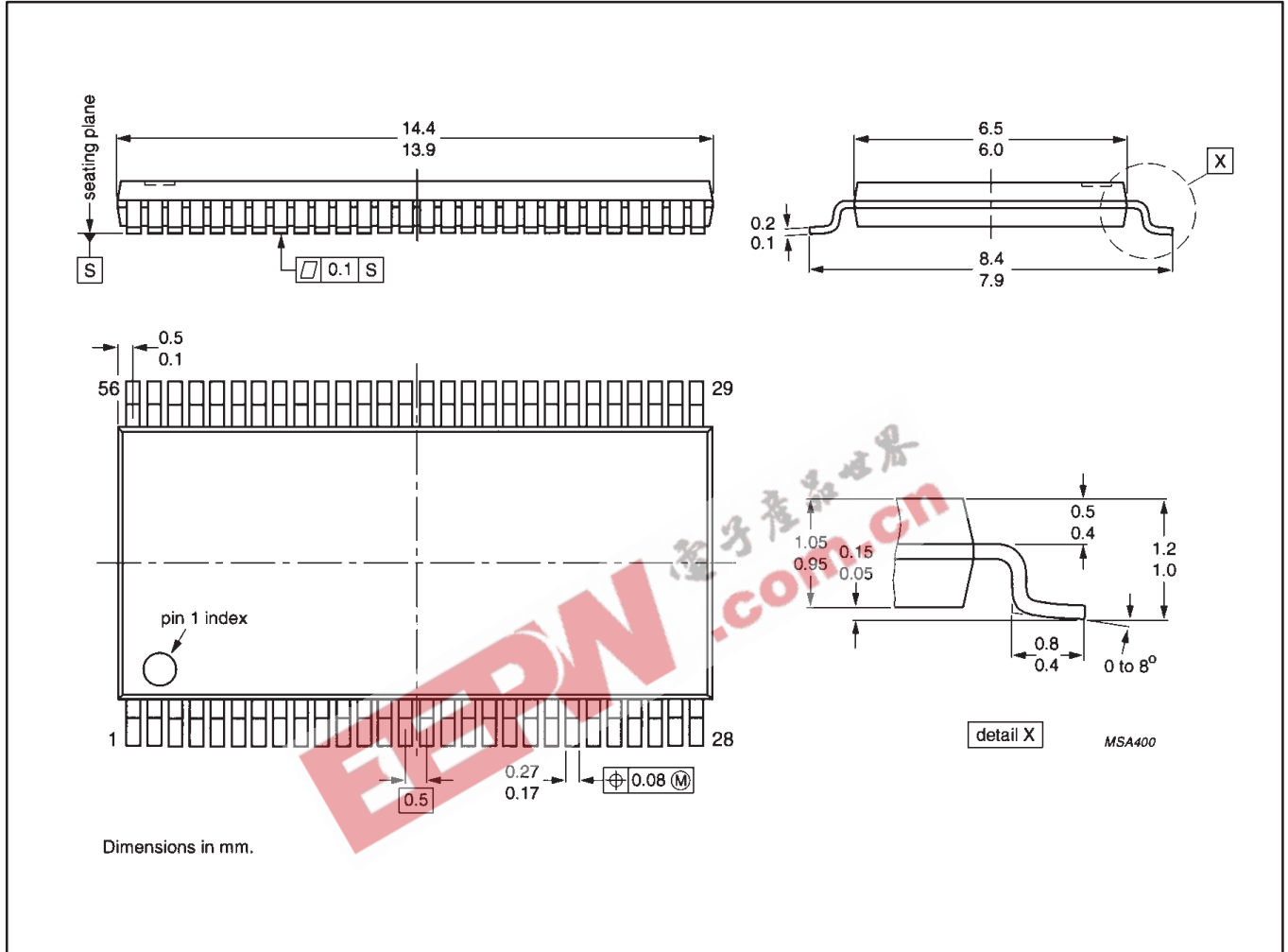
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT371-1 | | MO-118AB | | | | 93-11-02 95-02-04 |

20-bit buffer/line driver, non-inverting (3-State)

74ABT16827A
74ABTH16827A

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



20-bit buffer/line driver, non-inverting (3-State)

74ABT16827A
74ABTH16827A

NOTES



20-bit buffer/line driver, non-inverting, with 30Ω
termination resistors (3-State)

74ABT162827A
74ABTH162827A

Data sheet status

| Data sheet status | Product status | Definition [1] |
|---------------------------|----------------|--|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
| Preliminary specification | Qualification | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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