

## 74ALVC162244

### Low Voltage 16-Bit Buffer/Line Driver with 3.6V Tolerant Inputs and Outputs and 26Ω Series Resistor in Outputs

#### General Description

The ALVC162244 contains sixteen non-inverting buffers with 3-STATE outputs to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble (4-bit) controlled. Each nibble has separate 3-STATE control inputs which can be shorted together for full 16-bit operation.

The 74ALVC162244 is designed for low voltage (1.65V to 3.6V)  $V_{CC}$  applications with I/O capability up to 3.6V. The 74ALVC162244 is also designed with 26Ω series resistors in the outputs. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

The 74ALVC162244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

#### Features

- 1.65V to 3.6V  $V_{CC}$  supply operation
- 3.6V tolerant inputs and outputs
- 26Ω series resistors in outputs
- $t_{PD}$ 
  - 3.8 ns max for 3.0V to 3.6V  $V_{CC}$
  - 4.3 ns max for 2.3V to 2.7V  $V_{CC}$
  - 7.6 ns max for 1.65V to 1.95V  $V_{CC}$
- Power-off high impedance inputs and outputs
- Supports live insertion and withdrawal
- Uses patented noise/EMI reduction circuitry
- Latchup conforms to JEDEC JED78
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

**Note 1:** To ensure the high-impedance state during power up or power down, OE should be tied to  $V_{CC}$  through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

#### Ordering Code:

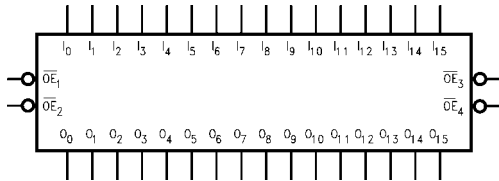
Order Number	Package Number	Package Description
74ALVC162244GX (Note 2)	BGA54A	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL]
74ALVC162244T (Note 3)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

**Note 2:** BGA package available in Tape and Reel only.

**Note 3:** Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

74ALVC162244 Low Voltage 16-Bit Buffer/Line Driver with 3.6V Tolerant Inputs and Outputs and 26Ω Series Resistor in Outputs

**Logic Symbol**

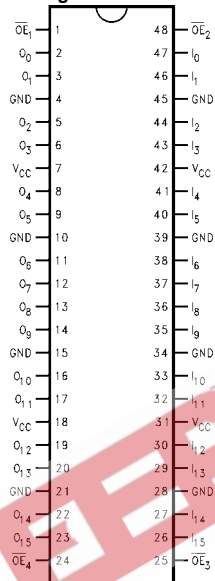


**Pin Descriptions**

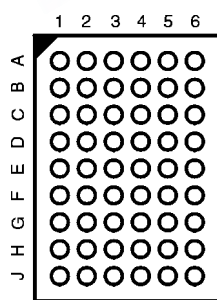
Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$I_0-I_{15}$	Inputs
$O_0-O_{15}$	Outputs
NC	No Connect

**Connection Diagrams**

**Pin Assignment for TSSOP**



**Pin Assignment for FBGA**



(Top Thru View)

**FBGA Pin Assignments**

	1	2	3	4	5	6
<b>A</b>	$O_0$	NC	$\overline{OE}_1$	$\overline{OE}_2$	NC	$I_0$
<b>B</b>	$O_2$	$O_1$	NC	NC	$I_1$	$I_2$
<b>C</b>	$O_4$	$O_3$	$V_{CC}$	$V_{CC}$	$I_3$	$I_4$
<b>D</b>	$O_6$	$O_5$	GND	GND	$I_5$	$I_6$
<b>E</b>	$O_8$	$O_7$	GND	GND	$I_7$	$I_8$
<b>F</b>	$O_{10}$	$O_9$	GND	GND	$I_9$	$I_{10}$
<b>G</b>	$O_{12}$	$O_{11}$	$V_{CC}$	$V_{CC}$	$I_{11}$	$I_{12}$
<b>H</b>	$O_{14}$	$O_{13}$	NC	NC	$I_{13}$	$I_{14}$
<b>J</b>	$O_{15}$	NC	$\overline{OE}_4$	$\overline{OE}_3$	NC	$I_{15}$

**Truth Tables**

Inputs		Outputs
$\overline{OE}_1$	$I_0-I_3$	$O_0-O_3$
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	$I_4-I_7$	$O_4-O_7$
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	$I_8-I_{11}$	$O_8-O_{11}$
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	$I_{12}-I_{15}$	$O_{12}-O_{15}$
L	L	L
L	H	H
H	X	Z

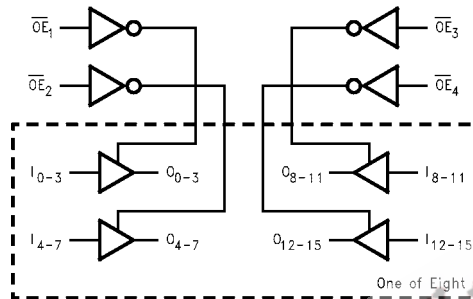
H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial (HIGH or LOW, inputs may not float)  
 Z = High Impedance

## Functional Description

The 74ALVC162244 contains sixteen non-inverting buffers with 3-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of each other. The control pins may be shorted together to obtain full 16-bit operation. The 3-STATE out-

puts are controlled by an Output Enable ( $\overline{OE}_n$ ) input. When  $\overline{OE}_n$  is LOW, the outputs are in the 2-state mode. When  $\overline{OE}_n$  is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the inputs.

## Logic Diagram



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Absolute Maximum Ratings (Note 4)		Recommended Operating Conditions (Note 6)	
Supply Voltage ( $V_{CC}$ )	-0.5V to +4.6V	Power Supply	
DC Input Voltage ( $V_I$ )	-0.5V to 4.6V	Operating	1.65V to 3.6V
Output Voltage ( $V_O$ ) (Note 5)	-0.5V to $V_{CC} + 0.5V$	Input Voltage	0V to $V_{CC}$
DC Input Diode Current ( $I_{IK}$ )		Output Voltage ( $V_O$ )	0V to $V_{CC}$
$V_I < 0V$	-50 mA	Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
DC Output Diode Current ( $I_{OK}$ )		Minimum Input Edge Rate ( $\Delta t/\Delta V$ )	
$V_O < 0V$	-50 mA	$V_{IN} = 0.8V$ to $2.0V$ , $V_{CC} = 3.0V$	10 ns/V
DC Output Source/Sink Current		<b>Note 4:</b> The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.	
( $I_{OH}/I_{OL}$ )	$\pm 50$ mA	<b>Note 5:</b> $I_O$ Absolute Maximum Rating must be observed.	
DC $V_{CC}$ or GND Current per		<b>Note 6:</b> Floating or unused control inputs must be held HIGH or LOW.	
Supply Pin ( $I_{CC}$ or GND)	$\pm 100$ mA		
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C		

### DC Electrical Characteristics

Symbol	Parameter	Conditions	$V_{CC}$ (V)	Min	Max	Units
$V_{IH}$	HIGH Level Input Voltage		1.65 - 1.95 2.3 - 2.7 2.7 - 3.6	$0.65 \times V_{CC}$ 1.7 2.0		V
$V_{IL}$	LOW Level Input Voltage		1.65 - 1.95 2.3 - 2.7 2.7 - 3.6		$0.35 \times V_{CC}$ 0.7 0.8	V
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$ $I_{OH} = -2 \text{ mA}$ $I_{OH} = -4 \text{ mA}$ $I_{OH} = -6 \text{ mA}$ $I_{OH} = -8 \text{ mA}$ $I_{OH} = -12 \text{ mA}$	1.65 - 3.6 1.65 2.3 2.3 3 2.7 3.0	$V_{CC} - 0.2$ 1.2 1.9 1.7 2.4 2 2		V
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100 \mu A$ $I_{OL} = 2 \text{ mA}$ $I_{OL} = 4 \text{ mA}$ $I_{OL} = 6 \text{ mA}$ $I_{OL} = 8 \text{ mA}$ $I_{OL} = 12 \text{ mA}$	1.65 - 3.6 1.65 2.3 2.3 3 2.7 3		0.2 0.45 0.4 0.55 0.55 0.6 0.8	V
$I_I$	Input Leakage Current	$0 \leq V_I \leq 3.6V$	3.6		$\pm 5.0$	$\mu A$
$I_{OZ}$	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$	3.6		$\pm 10$	$\mu A$
$I_{CC}$	Quiescent Supply Current	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6		40	$\mu A$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	$V_{IH} = V_{CC} - 0.6V$	3 - 3.6		750	$\mu A$

AC Electrical Characteristics										
Symbol	Parameter	T <sub>A</sub> = -40°C to +85°C, R <sub>L</sub> = 500Ω								Units
		C <sub>L</sub> = 50 pF				C <sub>L</sub> = 30 pF				
		V <sub>CC</sub> = 3.3V ± 0.3V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 2.5V ± 0.2V		V <sub>CC</sub> = 1.8V ± 0.15V		
		Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay	1.3	3.8	1.5	4.3	1.0	3.8	1.5	7.6	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time	1.3	4.3	1.5	5.6	1.0	5.1	1.5	9.8	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Output Disable Time	1.3	4.1	1.5	4.5	1.0	4.0	1.5	7.2	ns
Capacitance										
Symbol	Parameter	Conditions	T <sub>A</sub> = +25°C		Units					
			V <sub>CC</sub>	Typical						
C <sub>IN</sub>	Input Capacitance	V <sub>I</sub> = 0V or V <sub>CC</sub>	3.3	6	pF					
C <sub>OUT</sub>	Output Capacitance	V <sub>I</sub> = 0V or V <sub>CC</sub>	3.3	7	pF					
C <sub>PD</sub>	Power Dissipation Capacitance	Outputs Enabled	f = 10 MHz, C <sub>L</sub> = 50 pF	3.3	20	pF				
				2.5	20					

## AC Loading and Waveforms

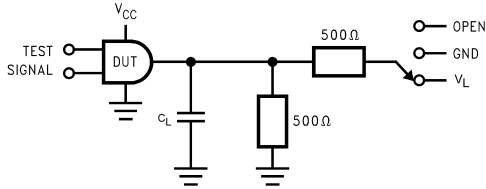


FIGURE 1. AC Test Circuit

TABLE 1. Values for Figure 1

TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	$V_L$
$t_{PZH}$ , $t_{PHZ}$	GND

TABLE 2. Variable Matrix  
(Input Characteristics:  $f = t_r = t_f = 2\text{ns}$ ;  $Z_0 = 50\Omega$ )

Symbol	$V_{CC}$			
	$3.3\text{V} \pm 0.3\text{V}$	2.7V	$2.5\text{V} \pm 0.2\text{V}$	$1.8\text{V} \pm 0.15\text{V}$
$V_{mi}$	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_{mo}$	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_X$	$V_{OL} + 0.3\text{V}$	$V_{OL} + 0.3\text{V}$	$V_{OL} + 0.15\text{V}$	$V_{OL} + 0.15\text{V}$
$V_Y$	$V_{OH} - 0.3\text{V}$	$V_{OH} - 0.3\text{V}$	$V_{OH} - 0.15\text{V}$	$V_{OH} - 0.15\text{V}$
$V_L$	6V	6V	$V_{CC} * 2$	$V_{CC} * 2$

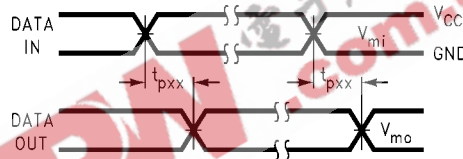


FIGURE 2. Waveform for Inverting and Non-Inverting Functions

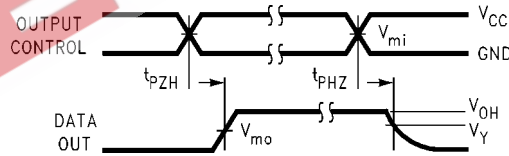


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

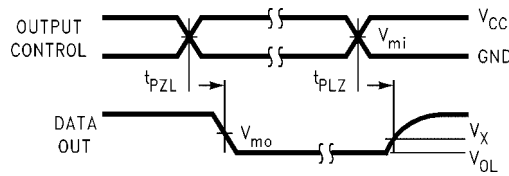
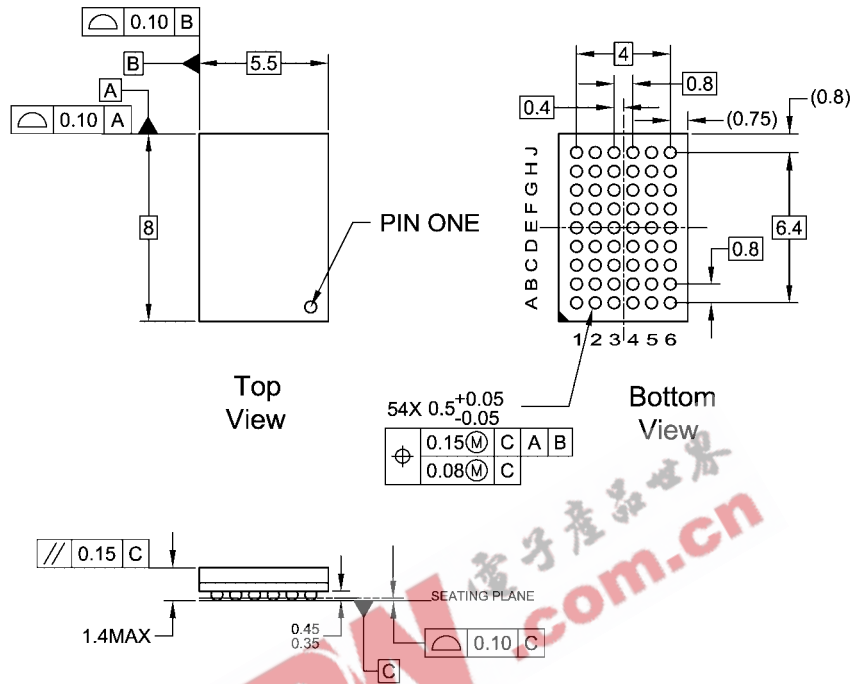


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

**Physical Dimensions** inches (millimeters) unless otherwise noted



**NOTES:**

- A. THIS PACKAGE CONFORMS TO JEDEC M0-205
- B. ALL DIMENSIONS IN MILLIMETERS
- C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)  
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
- D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

**54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide  
Package Number BGA54A**

### Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

12.50±0.10  
0.40 TYP  
8.10  
4.05  
6.10±0.10  
1  
6  
19  
24  
30  
43  
48  
PIN #1 IDENT.  
ALL LEAD TIPS  
0.2 C B A  
ALL LEAD TIPS  
LAND PATTERN RECOMMENDATION  
0.30  
0.50  
2.30  
1  
6  
19  
24  
4.60  
9.20  
0.09-0.20  
SEE DETAIL A  
0.90±0.15  
0.10  
1.2 MAX  
0.50  
0.17-0.27  
0.10±0.05  
0.1 C  
ALL LEAD TIPS  
0.13 M A B C S  
DIMENSIONS ARE IN MILLIMETERS  
NOTES:  
A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.  
B. DIMENSIONS ARE IN MILLIMETERS.  
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.  
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.  
MTD48RevB1  
DETAIL A  
12.00° TOP & BOTTOM  
R0.16  
R0.31  
GAGE PLANE  
1.25  
SEATING PLANE  
0°-8°  
0.60±0.10  
1.00

**48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48**

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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