

74LVT32374 • 74LVTH32374

Low Voltage 32-Bit D-Type Flip-Flop with 3-STATE Outputs

General Description

The LVT32374 and LVTH32374 contain thirty-two non-inverting D-type flip-flops with 3-STATE outputs and are intended for bus oriented applications. The device is byte controlled. A buffered clock (CP) and Output Enable (\overline{OE}) are common to each byte and can be shorted together for full 32-bit operation.

The LVTH32374 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These flip-flops are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT32374 and LVTH32374 are fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH32374)
- Also available without bushold feature (74LVT32374)
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- ESD performance:
 - Human-body model > 2000V
 - Machine model > 200V
 - Charged-device model > 1000V
- Packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

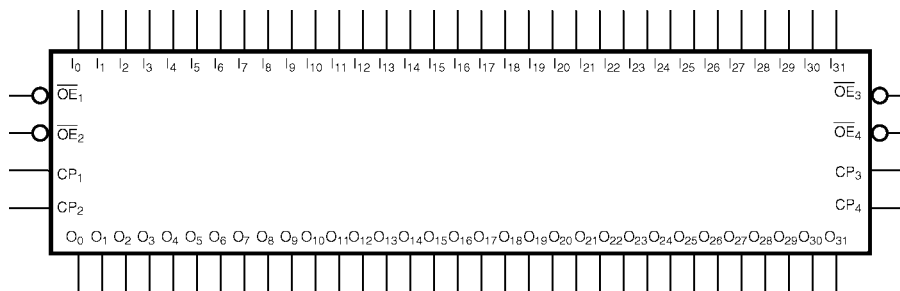
Ordering Code:

Order Number	Package Number	Package Description
74LVT32374G (Note 1)(Note 2)	BGA96A (Preliminary)	96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
74LVTH32374G (Note 1)(Note 2)	BGA96A	96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide

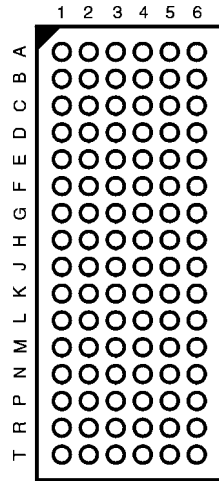
Note 1: Ordering code "G" indicates Trays.

Note 2: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



(Top Thru View)

Pin Descriptions

Pin Names	Description
\overline{OE}_n	Output Enable Input (Active LOW)
CP_n	Clock Pulse Input
I_0-I_{31}	Inputs
O_0-O_{31}	3-STATE Outputs

FBGA Pin Assignments

	1	2	3	4	5	6
A	O_1	O_0	\overline{OE}_1	CP_1	I_0	I_1
B	O_3	O_2	GND	GND	I_2	I_3
C	O_5	O_4	V_{CC1}	V_{CC1}	I_4	I_5
D	O_7	O_6	GND	GND	I_6	I_7
E	O_9	O_8	GND	GND	I_8	I_9
F	O_{11}	O_{10}	V_{CC1}	V_{CC1}	I_{10}	I_{11}
G	O_{13}	O_{12}	GND	GND	I_{12}	I_{13}
H	O_{14}	O_{15}	\overline{OE}_2	CP_2	I_{15}	I_{14}
J	O_{17}	O_{16}	\overline{OE}_3	CP_3	I_{16}	I_{17}
K	O_{19}	O_{18}	GND	GND	I_{18}	I_{19}
L	O_{21}	O_{20}	V_{CC2}	V_{CC2}	I_{20}	I_{21}
M	O_{23}	O_{22}	GND	GND	I_{22}	I_{23}
N	O_{25}	O_{24}	GND	GND	I_{24}	I_{25}
P	O_{27}	O_{26}	V_{CC2}	V_{CC2}	I_{26}	I_{27}
R	O_{29}	O_{28}	GND	GND	I_{28}	I_{29}
T	O_{30}	O_{31}	\overline{OE}_4	CP_4	I_{31}	I_{30}

Functional Description

The LVT32374 and LVTH32374 consist of thirty-two edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 32-bit operation. Each byte has a buffered clock and buffered Output Enable common to all flip-flops within that byte. The description which follows applies to each byte. Each flip-flop will store the state of their individual D-type inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP_n) transition. With the Output Enable (\overline{OE}_n) LOW, the contents of the flip-flops are available at the outputs. When \overline{OE}_n is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE}_n input does not affect the state of the flip-flops.

Truth Tables

Inputs			Outputs
CP_1	\overline{OE}_1	I_0-I_7	O_0-O_7
↗	L	H	H
↗	L	L	L
L	L	X	O_0
X	H	X	Z

Inputs			Outputs
CP_2	\overline{OE}_2	I_8-I_{15}	O_8-O_{15}
↗	L	H	H
↗	L	L	L
L	L	X	O_0
X	H	X	Z

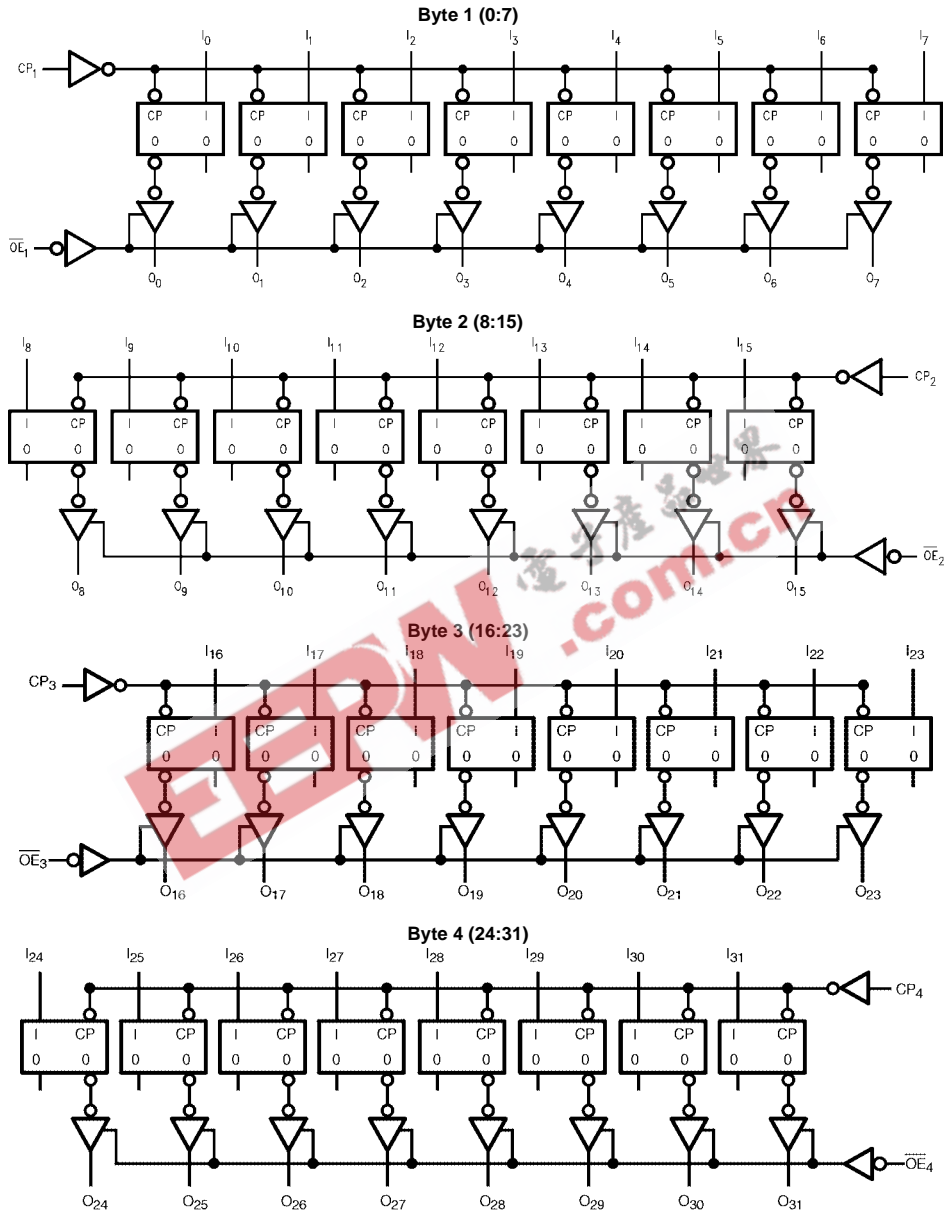
Inputs			Outputs
CP_3	\overline{OE}_3	$I_{16}-I_{23}$	$O_{16}-O_{23}$
↗	L	H	H
↗	L	L	L
L	L	X	O_0
X	H	X	Z

Inputs			Outputs
CP_4	\overline{OE}_4	$I_{24}-I_{31}$	$O_{24}-O_{31}$
↗	L	H	H
↗	L	L	L
L	L	X	O_0
X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Z = HIGH Impedance
 O_0 = Previous O_0 before HIGH-to-LOW of CP

Logic Diagrams



V_{CC1} is associated with Bytes 1 and 2.

V_{CC2} is associated with Bytes 3 and 4.

Note: Please note that these diagrams are provided for the understanding of logic operation and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 3)

Symbol	Parameter	Value	Conditions	Units
V _{CC}	Supply Voltage	-0.5 to +4.6		V
V _I	DC Input Voltage	-0.5 to +7.0		V
V _O	DC Output Voltage	-0.5 to +7.0	Output in 3-STATE	V
		-0.5 to +7.0	Output in HIGH or LOW State (Note 4)	
I _{IK}	DC Input Diode Current	-50	V _I < GND	mA
I _{OK}	DC Output Diode Current	-50	V _O < GND	mA
I _O	DC Output Current	64	V _O > V _{CC} Output at HIGH State	mA
		128	V _O > V _{CC} Output at LOW State	
I _{CC}	DC Supply Current per Supply Pin	±64		mA
I _{GND}	DC Ground Current per Ground Pin	±128		mA
T _{STG}	Storage Temperature	-65 to +150		°C

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V _{CC}	Supply Voltage	2.7	3.6	V
V _I	Input Voltage	0	5.5	V
I _{OH}	HIGH Level Output Current		32	mA
I _{OL}	LOW Level Output Current		64	mA
T _A	Free-Air Operating Temperature	-40	85	°C
Δt/ΔV	Input Edge Rate, V _{IN} = 0.8V–2.0V, V _{CC} = 3.0V	0	10	ns/V

Note 3: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

Note 4: I_O Absolute Maximum Rating must be observed.

DC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	T _A = -40°C to +85°C		Units	Conditions	
			Min	Max			
V _{IK}	Input Clamp Diode Voltage	2.7		-1.2	V	I _I = -18 mA	
V _{IH}	Input HIGH Voltage	2.7–3.6	2.0		V	V _O ≤ 0.1V or	
V _{IL}	Input LOW Voltage	2.7–3.6		0.8	V	V _O ≥ V _{CC} - 0.1V	
V _{OH}	Output HIGH Voltage	2.7–3.6	V _{CC} - 0.2		V	I _{OH} = -100 μA	
		2.7	2.4	I _{OH} = -8 mA			
		3.0	2.0	I _{OH} = -32 mA			
V _{OL}	Output LOW Voltage	2.7		0.2	V	I _{OL} = 100 μA	
		2.7		0.5		I _{OL} = 24 mA	
		3.0		0.4		I _{OL} = 16 mA	
		3.0		0.5		I _{OL} = 32 mA	
		3.0		0.55		I _{OL} = 64 mA	
I _{I(HOLD)} (Note 5)	Bushold Input Minimum Drive	3.0	75		μA	V _I = 0.8V	
			-75			V _I = 2.0V	
I _{I(OD)} (Note 5)	Bushold Input Over-Drive Current to Change State	3.0	500		μA	(Note 6)	
			-500			(Note 7)	
I _I	Input Current	3.6		10	μA	V _I = 5.5V	
		Control Pins	3.6			±1	V _I = 0V or V _{CC}
			Data Pins	3.6			-5
				1		V _I = V _{CC}	
I _{OFF}	Power Off Leakage Current	0		±100	μA	0V ≤ V _I or V _O ≤ 5.5V	
I _{PU/PD}	Power Up/Down 3-STATE Output Current	0–1.5V		±100	μA	V _O = 0.5V to 3.0V V _I = GND or V _{CC}	
I _{OZL}	3-STATE Output Leakage Current	3.6		-5	μA	V _O = 0.5V	
I _{OZH}	3-STATE Output Leakage Current	3.6		5	μA	V _O = 3.0V	
I _{OZH+}	3-STATE Output Leakage Current	3.6		10	μA	V _{CC} < V _O ≤ 5.5V	

DC Electrical Characteristics (Continued)

Symbol	Parameter	V _{CC} (V)	T _A = -40°C to +85°C		Units	Conditions
			Min	Max		
I _{CCH}	Power Supply Current (V _{CC1} or V _{CC2})	3.6		0.19	mA	Outputs HIGH
I _{CCL}	Power Supply Current (V _{CC1} or V _{CC2})	3.6		5	mA	Outputs LOW
I _{CCZ}	Power Supply Current (V _{CC1} or V _{CC2})	3.6		0.19	mA	Outputs Disabled
I _{CCZ+}	Power Supply Current (V _{CC1} or V _{CC2})	3.6		0.19	mA	V _{CC} ≤ V _O ≤ 5.5V, Outputs Disabled
ΔI _{CC}	Increase in Power Supply Current (V _{CC1} or V _{CC2}) (Note 8)	3.6		0.2	mA	One Input at V _{CC} - 0.6V Other Inputs at V _{CC} or GND

Note 5: Applies to bushold version only (74LVTH32374).

Note 6: An external driver must sink at least the specified current to switch from LOW-to-HIGH.

Note 7: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 8: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics (Note 9)

Symbol	Parameter	V _{CC} (V)	T _A = 25°C			Units	Conditions C _L = 50 pF, R _L = 500Ω
			Min	Typ	Max		
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3		0.8		V	(Note 10)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3		-0.8		V	(Note 10)

Note 9: Characterized in SSOP package. Guaranteed parameter, but not tested.

Note 10: Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

Symbol	Parameter	T _A = -40°C to +85°C, C _L = 50 pF, R _L = 500Ω				Units
		V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.7V		
		Min	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	160		160		MHz
t _{PHL}	Propagation Delay	1.9	4.3	1.9	4.6	ns
t _{PLH}	CP to O _n	1.6	4.5	1.6	5.2	ns
t _{PZL}	Output Enable Time	1.3	4.4	1.3	5.0	ns
t _{PZH}		1.0	4.5	1.0	5.4	ns
t _{PLZ}	Output Disable Time	1.5	4.6	1.5	4.8	ns
t _{PHZ}		2.0	5.0	2.0	5.4	ns
t _S	Setup Time	1.8		2.0		ns
t _H	Hold Time	0.8		0.1		ns
t _W	Pulse Width	3.0		3.0		ns

Capacitance (Note 11)

Symbol	Parameter	Conditions	Typical	Units
C _{IN}	Input Capacitance	V _{CC} = OPEN, V _I = 0V or V _{CC}	4	pF
C _{OUT}	Output Capacitance	V _{CC} = 3.0V, V _O = 0V or V _{CC}	8	pF

Note 11: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

Physical Dimensions

inches (millimeters) unless otherwise noted

Top View

Bottom View

SEATING PLANE

NOTES:

- A. THIS PACKAGE CONFORMS TO JEDEC M0-205
- B. ALL DIMENSIONS IN MILLIMETERS
- C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
 .35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
- D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA96ArevE

**96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC M0-205, 5.5mm Wide
 Package Number BGA96A**

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