

# DATA SHEET

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## 74LVT2245

3.3V Octal transceiver with 30Ω  
termination resistors (3-State)

Product specification  
Supersedes data of 1996 Mar 11  
IC23 Data Handbook

1998 Feb 19

# 3.3V Octal transceiver with 30Ω termination resistors (3-State)

# 74LVT2245

## FEATURES

- 30Ω output termination resistors
- Octal bidirectional bus interface
- 3-State buffers
- Output capability: +12mA/-12mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

## DESCRIPTION

The LVT2245 is a high-performance BiCMOS product designed for  $V_{CC}$  operation at 3.3V.

This device is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable (OE) input for easy cascading and a Direction (DIR) input for direction control.

The 74LVT2245 is designed with 30Ω series resistance in both the High and Low states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

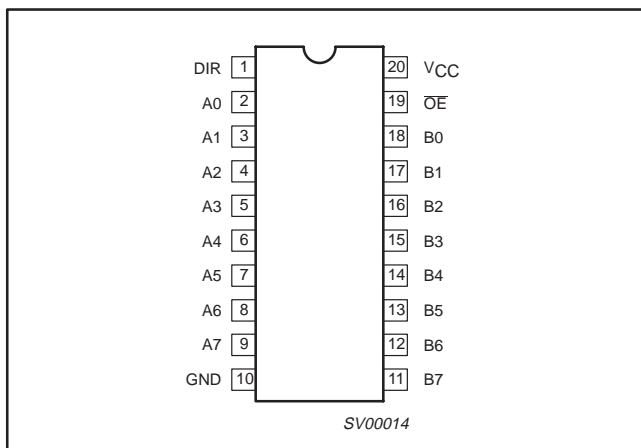
## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}C$ ; $GND = 0V$	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay An to Bn or Bn to An	$C_L = 50pF$ ; $V_{CC} = 3.3V$	3.2 3.1	ns
$C_{IN}$	Input capacitance DIR, OE	$V_I = 0V$ or 3.0V	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O} = 0V$ or 3.0V	10	pF
$I_{CCZ}$	Total supply current	Outputs disabled; $V_{CC} = 3.6V$	0.13	mA

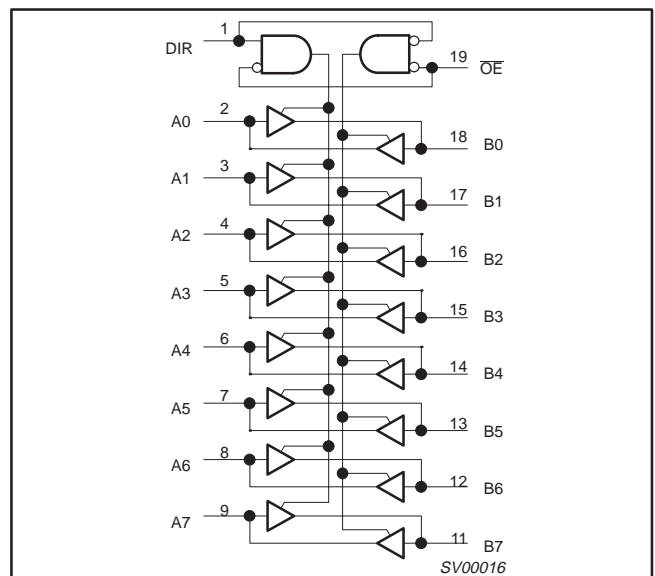
## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic SO	-40°C to +85°C	74LVT2245 D	74LVT2245 D	SOT163-1
20-Pin Plastic SSOP	-40°C to +85°C	74LVT2245 DB	74LVT2245 DB	SOT339-1
20-Pin Plastic TSSOP	-40°C to +85°C	74LVT2245 PW	7LVT2245PW DH	SOT360-1

## PIN CONFIGURATION



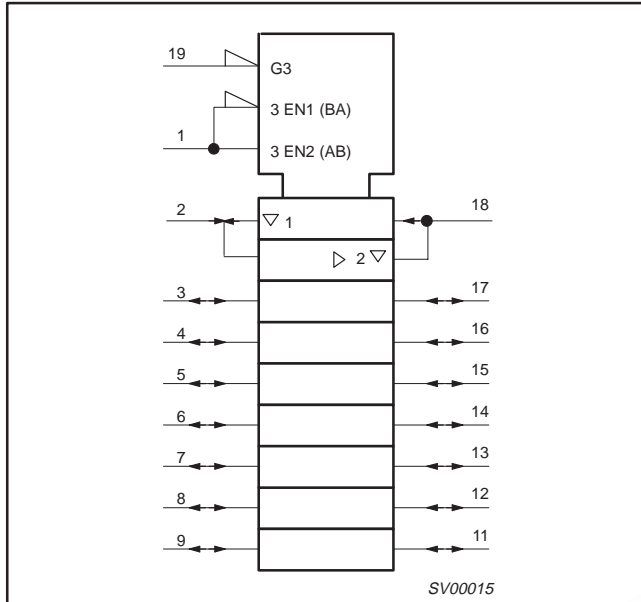
## LOGIC SYMBOL



# 3.3V Octal transceiver with 30Ω termination resistors (3-State)

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## LOGIC SYMBOL (IEEE/IEC)

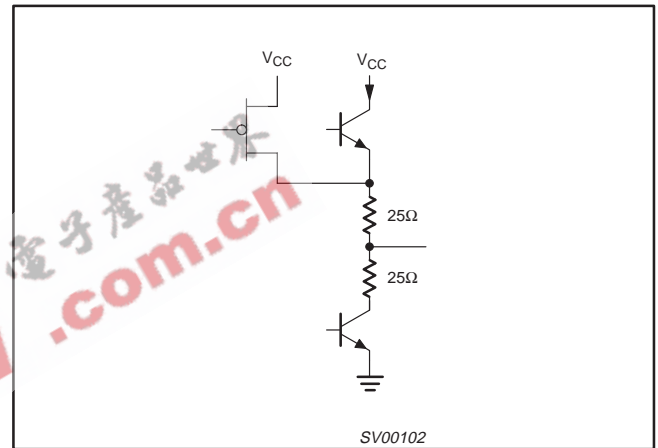


## FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
OE <sub>n</sub>	DIR	A <sub>n</sub>	B <sub>n</sub>
L	L	A <sub>n</sub> = B <sub>n</sub>	Inputs
L	H	Inputs	B <sub>n</sub> = A <sub>n</sub>
H	X	Z	Z

H = High voltage level  
 L = Low voltage level  
 X = Don't care  
 Z = High impedance "Off" state

## SCHEMATIC OF EACH OUTPUT



## PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	DIR	Direction control input
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs/outputs (A side)
18, 17, 16, 15, 14, 13, 12, 11	B0 – B7	Data inputs/outputs (B side)
19	OE	Output enable input (active-Low)
10	GND	Ground (0V)
20	V <sub>CC</sub>	Positive supply voltage

## ABSOLUTE MAXIMUM RATINGS<sup>1,2</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		-0.5 to +4.6	V
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0	-50	mA
V <sub>I</sub>	DC input voltage <sup>3</sup>		-0.5 to +7.0	V
I <sub>OK</sub>	DC output diode current	V <sub>O</sub> < 0	-50	mA
V <sub>OUT</sub>	DC output voltage <sup>3</sup>	Output in Off or High state	-0.5 to +7.0	V
I <sub>OUT</sub>	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T <sub>stg</sub>	Storage temperature range		-65 to +150	°C

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

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### RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
$V_{CC}$	DC supply voltage	2.7	3.6	V
$V_I$	Input voltage	0	5.5	V
$V_{IH}$	High-level input voltage	2.0		V
$V_{IL}$	Input voltage		0.8	V
$I_{OH}$	High-level output current		-12	mA
$I_{OL}$	Low-level output current		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
$T_{amb}$	Operating free-air temperature range	-40	+85	°C

### DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
$V_{IK}$	Input clamp voltage	$V_{CC} = 2.7V; I_{IK} = -18mA$		-0.9	-1.2	V
$V_{OH}$	High-level output voltage	$V_{CC} = 3.0V; I_{OH} = -12mA$	2.0	2.2		V
$V_{OL}$	Low-level output voltage	$V_{CC} = 3.0V; I_{OL} = 12mA$			0.8	V
$I_I$	Input leakage current	$V_{CC} = 0$ or $3.6V; V_I = 5.5V$	Control pins	1	10	$\mu A$
		$V_{CC} = 3.6V; V_I = V_{CC}$ or GND		$\pm 0.1$	$\pm 1$	
		$V_{CC} = 3.6V; V_I = 5.5V$	I/O Data pins <sup>4</sup>	1	20	
		$V_{CC} = 3.6V; V_I = V_{CC}$		0.1	1	
		$V_{CC} = 3.6V; V_I = 0$		-1	-5	
$I_{OFF}$	Output off current	$V_{CC} = 0V; V_I$ or $V_O = 0$ to 4.5V		1	$\pm 100$	$\mu A$
$I_{HOLD}$	Bus Hold current A inputs <sup>6</sup>	$V_{CC} = 3V; V_I = 0.8V$	75	150		$\mu A$
		$V_{CC} = 3V; V_I = 2.0V$	-75	-150		
		$V_{CC} = 0V$ to $3.6V; V_{CC} = 3.6V$	$\pm 500$			
$I_{EX}$	Current into an output in the High state when $V_O > V_{CC}$	$V_O = 5.5V; V_{CC} = 3.0V$		60	125	$\mu A$
$I_{PU/PD}$	Power up/down 3-State output current <sup>3</sup>	$V_{CC} \leq 1.2V; V_O = 0.5V$ to $V_{CC}; V_I = GND$ or $V_{CC}; OE/OE = Don't\ care$		15	$\pm 100$	$\mu A$
$I_{CCH}$	Quiescent supply current	$V_{CC} = 3.6V; \text{Outputs High}, V_I = GND$ or $V_{CC}, I_O = 0$		0.13	0.19	mA
$I_{CCL}$		$V_{CC} = 3.6V; \text{Outputs Low}, V_I = GND$ or $V_{CC}, I_O = 0$		3	12	
$I_{CCZ}$		$V_{CC} = 3.6V; \text{Outputs Disabled}; V_I = GND$ or $V_{CC}, I_O = 0^5$		0.13	0.19	
$\Delta I_{CC}$	Additional supply current per input pin <sup>3</sup>	$V_{CC} = 3V$ to $3.6V; \text{One input at } V_{CC}-0.6V, \text{ Other inputs at } V_{CC}$ or GND		0.1	0.2	mA

#### NOTES:

- All typical values are at  $V_{CC} = 3.3V$  and  $T_{amb} = 25^\circ C$ .
- This is the increase in supply current for each input at the specified voltage level other than  $V_{CC}$  or GND
- This parameter is valid for any  $V_{CC}$  between 0V and 1.2V with a transition time of up to 10msec. From  $V_{CC} = 1.2V$  to  $V_{CC} = 3.3V \pm 0.3V$  a transition time of 100 $\mu$ sec is permitted. This parameter is valid for  $T_{amb} = +25^\circ C$  only.
- Unused pins at  $V_{CC}$  or GND.
- $I_{CCZ}$  is measured with outputs pulled up to  $V_{CC}$  or down to GND
- This is the bus hold overdrive current required to force the input to the opposite logic state.

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## AC CHARACTERISTICS

GND = 0V;  $t_R = t_F = 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ;  $R_L = 500\Omega$ ;  $T_{\text{amb}} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

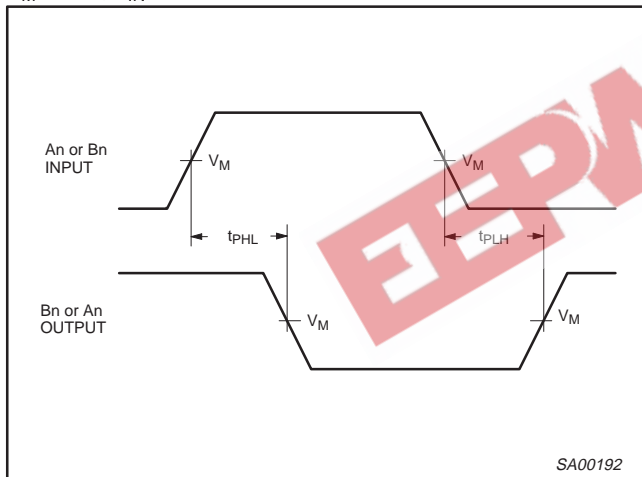
SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			$V_{CC} = 3.3\text{V} + 0.3\text{V}$			$V_{CC} = 2.7\text{V}$	
			MIN	TYP	MAX	MAX	
$t_{PLH}$ $t_{PHL}$	Propagation delay An to Bn or Bn to An	1	1.0 1.0	3.2 3.1	4.6 4.5	5.3 4.9	ns
$t_{PZH}$ $t_{PZL}$	Output enable time to High and Low level	2	1.1 1.5	4.5 4.3	7.0 6.5	9.1 7.6	ns
$t_{PHZ}$ $t_{PLZ}$	Output disable time from High and Low Level	2	2.2 2.0	3.7 3.6	5.2 5.0	5.6 5.0	ns

**NOTE:**

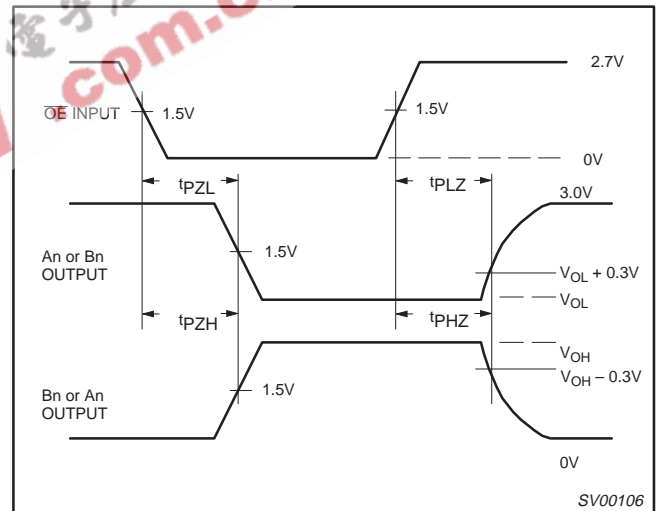
- All typical values are at  $V_{CC} = 3.3\text{V}$  and  $T_{\text{amb}} = 25^\circ\text{C}$ .

## AC WAVEFORMS

$V_M = 1.5\text{V}$ ,  $V_{IN} = \text{GND}$  to  $2.7\text{V}$



Waveform 1. Input (An or Bn) to Output (Bn or An) Propagation Delays



Waveform 2. 3-State Output Enable and Disable Times

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## TEST CIRCUIT AND WAVEFORMS

Test Circuit for 3-State Outputs

$V_M = 1.5V$   
Input Pulse Definition

**SWITCH POSITION**

TEST	SWITCH
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6V
$t_{PHZ}/t_{PZH}$	GND

**DEFINITIONS**

$R_L$  = Load resistor; see AC CHARACTERISTICS for value.

$C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

$R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	$t_W$	$t_R$	$t_F$
74LVT	2.7V	$\leq 10MHz$	500ns	$\leq 2.5ns$	$\leq 2.5ns$

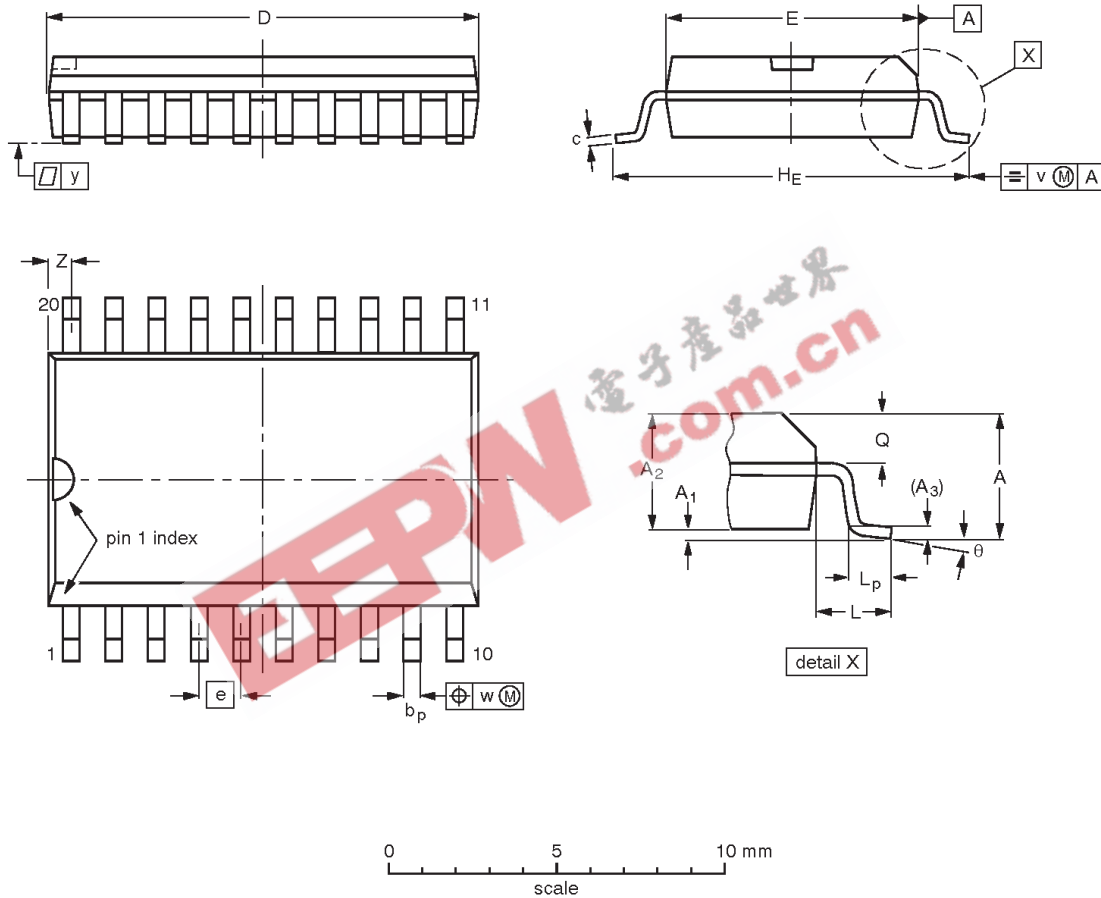
SV00092

3.3V Octal transceiver with 30Ω termination resistors (3-State)

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

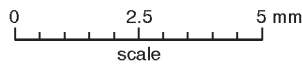
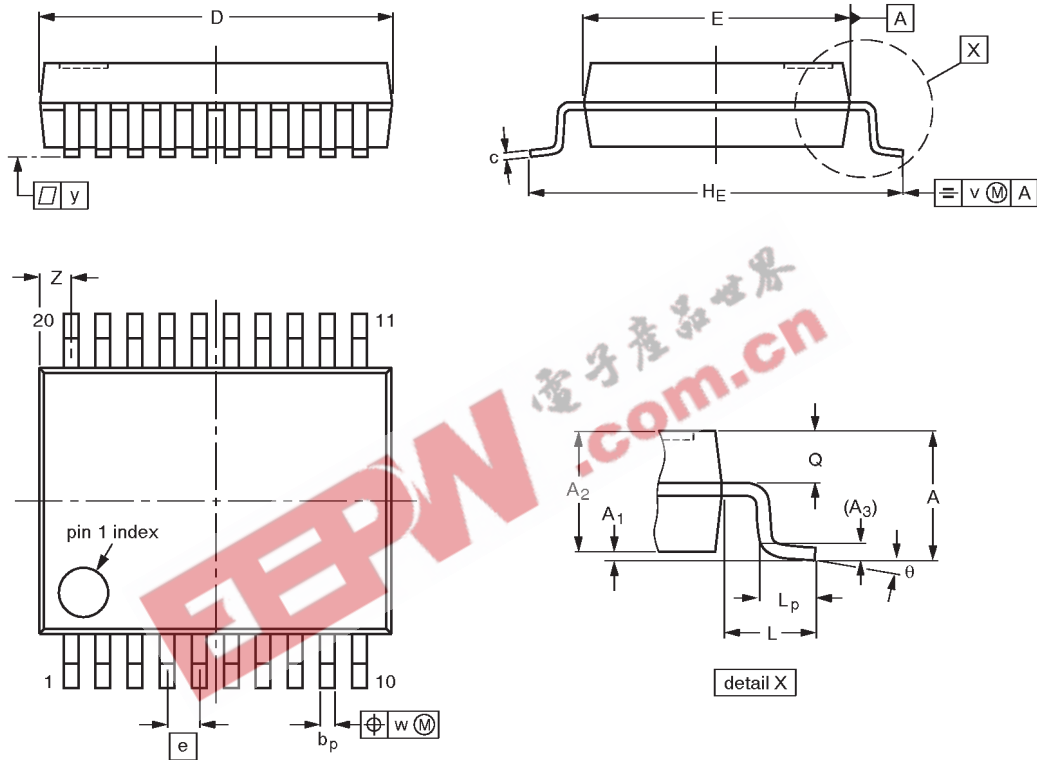
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				92-11-17 95-01-24

3.3V Octal transceiver with 30Ω termination resistors (3-State)

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SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				93-09-08- 95-02-04

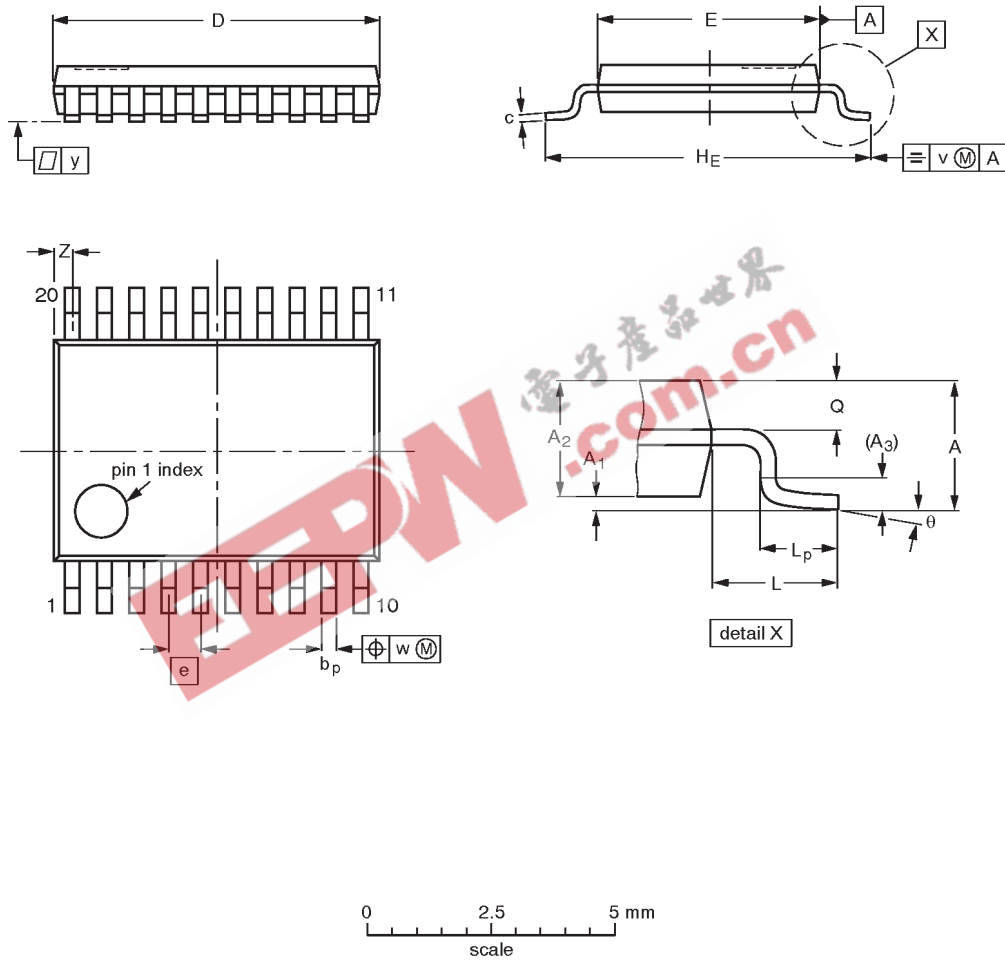


3.3V Octal transceiver with 30Ω termination resistors (3-State)

74LVT2245

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				93-06-16 95-02-04

# 3.3V Octal transceiver with 30Ω termination resistors (3-State)

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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