# SN74ALVCH32245
# 32-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES282 – OCTOBER 1999

- **Member of the Texas Instruments *Widebus+*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**
- **Packaged in Plastic Fine-Pitch Ball Grid Array Package**

## description

This 32-bit noninverting bus transceiver is designed for 1.65-V to 3.6-V $V_{CC}$ operation.

The SN74ALVCH32245 is designed for asynchronous communication between data buses. The control-function implementation minimizes external timing requirements.

This device can be used as four 8-bit transceivers, two 16-bit transceivers, or one 32-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

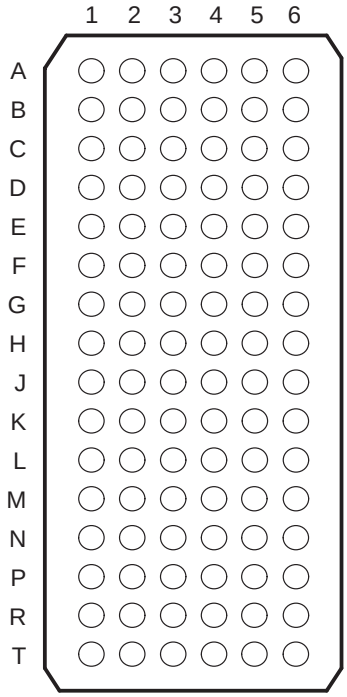
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH32245 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each 8-bit section)**

| INPUTS | | OPERATION |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

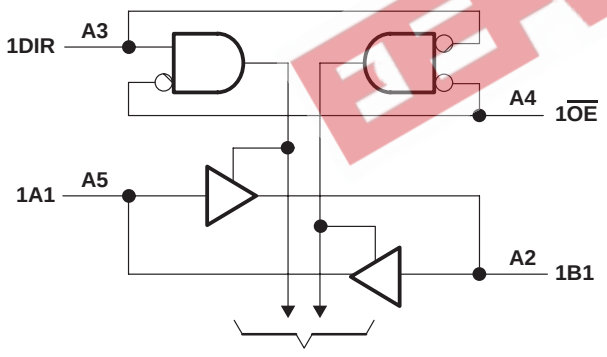
GKE PACKAGE
(TOP VIEW)



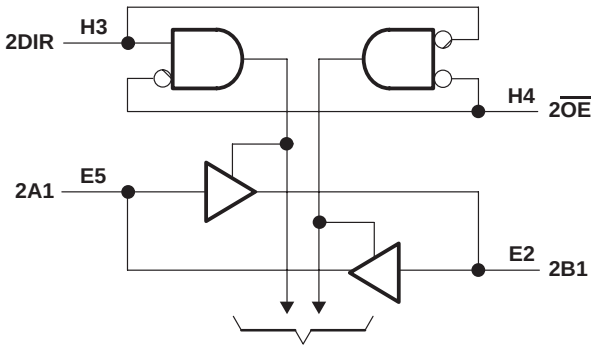

## terminal assignments

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| A | 1B2 | 1B1 | 1DIR | $1\overline{OE}$ | 1A1 | 1A2 |
| B | 1B4 | 1B3 | GND | GND | 1A3 | 1A4 |
| C | 1B6 | 1B5 | $V_{CC}$ | $V_{CC}$ | 1A5 | 1A6 |
| D | 1B8 | 1B7 | GND | GND | 1A7 | 1A8 |
| E | 2B2 | 2B1 | GND | GND | 2A1 | 2A2 |
| F | 2B4 | 2B3 | $V_{CC}$ | $V_{CC}$ | 2A3 | 2A4 |
| G | 2B6 | 2B5 | GND | GND | 2A5 | 2A6 |
| H | 2B8 | 2B7 | 2DIR | $2\overline{OE}$ | 2A7 | 2A8 |
| J | 3B2 | 3B1 | 3DIR | $3\overline{OE}$ | 3A1 | 3A2 |
| K | 3B4 | 3B3 | GND | GND | 3A3 | 3A4 |
| L | 3B6 | 3B5 | $V_{CC}$ | $V_{CC}$ | 3A5 | 3A6 |
| M | 3B8 | 3B7 | GND | GND | 3A7 | 3A8 |
| N | 4B2 | 4B1 | GND | GND | 4A1 | 4A2 |
| P | 4B4 | 4B3 | $V_{CC}$ | $V_{CC}$ | 4A3 | 4A4 |
| R | 4B6 | 4B5 | GND | GND | 4A5 | 4A6 |
| T | 4B7 | 4B8 | 4DIR | $4\overline{OE}$ | 4A8 | 4A7 |

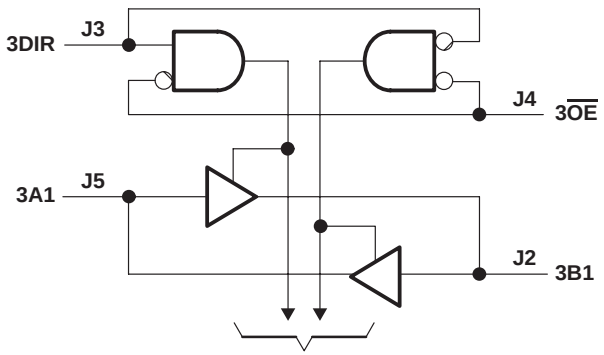
## logic diagram (positive logic)




To Seven Other Channels




To Seven Other Channels

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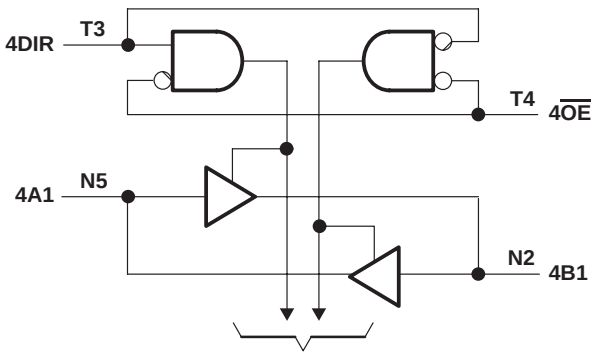



To Seven Other Channels

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 4.6 V
Input voltage range, $V_I$: Except I/O ports (see Note 1) . . . . . –0.5 V to 4.6 V
I/O ports (see Notes 1 and 2) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Output-voltage range, $V_O$ (see Notes 1 and 2) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –50 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) . . . . . –50 mA
Continuous output current, $I_O$ . . . . . ±50 mA
Continuous current through each $V_{CC}$ or GND . . . . . ±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3) . . . . . 40°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions (see Note 4)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 1.65 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | 0.65 × $V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | | 0.35 × $V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 1.65 V | | –4 | mA |
| | | $V_{CC}$ = 2.3 V | | –8 | |
| | | $V_{CC}$ = 2.7 V | | –12 | |
| | | $V_{CC}$ = 3 V | | –24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65 V | | 4 | mA |
| | | $V_{CC}$ = 2.3 V | | 8 | |
| | | $V_{CC}$ = 2.7 V | | 12 | |
| | | $V_{CC}$ = 3 V | | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

NOTE 4: All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $I_{OH}$ = –100 µA | 1.65 V to 3.6 V | $V_{CC}$–0.2 | | | V |
| | | $I_{OH}$ = –4 mA | 1.65 V | 1.2 | | | |
| | | $I_{OH}$ = –8 mA | 2.3 V | 1.7 | | | |
| | | $I_{OH}$ = –12 mA | 2.7 V | 2.2 | | | |
| | | | 3 V | 2.4 | | | |
| | | $I_{OH}$ = –24 mA | 3 V | 2.2 | | | |
| $V_{OL}$ | | $I_{OL}$ = 100 µA | 1.65 V to 3.6 V | | | 0.2 | V |
| | | $I_{OL}$ = 4 mA | 1.65 V | | | 0.45 | |
| | | $I_{OL}$ = 8 mA | 2.3 V | | | 0.7 | |
| | | $I_{OL}$ = 12 mA | 2.7 V | | | 0.4 | |
| | | $I_{OL}$ = 24 mA | 3 V | | | 0.55 | |
| $I_I$ | | $V_I$ = $V_{CC}$ or GND | 3.6 V | | | ±5 | µA |
| $I_{I(hold)}$ | | $V_I$ = 0.58 V | 1.65 V | 25 | | | µA |
| | | $V_I$ = 1.07 V | 1.65 V | –25 | | | |
| | | $V_I$ = 0.7 V | 2.3 V | 45 | | | |
| | | $V_I$ = 1.7 V | 2.3 V | –45 | | | |
| | | $V_I$ = 0.8 V | 3 V | 75 | | | |
| | | $V_I$ = 2 V | 3 V | –75 | | | |
| | | $V_I$ = 0 to 3.6 V‡ | 3.6 V | | | ±500 | |
| $I_{OZ}$§ | | $V_O$ = $V_{CC}$ or GND | 3.6 V | | | ±10 | µA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 3.6 V | | | 40 | µA |
| $\Delta I_{CC}$ | | One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | 3 V to 3.6 V | | | 750 | µA |
| $C_i$ | Control inputs | $V_I$ = $V_{CC}$ or GND | 3.3 V | | 4 | | pF |
| $C_{io}$ | A or B ports | $V_O$ = $V_{CC}$ or GND | 3.3 V | | 8 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
§ For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.

## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A or B | B or A | ¶ | ¶ | 1 | 3.7 | | 3.6 | 1 | 3 | ns |
| $t_{en}$ | $\overline{OE}$ | A or B | ¶ | ¶ | 1 | 5.7 | | 5.4 | 1 | 4.4 | ns |
| $t_{dis}$ | $\overline{OE}$ | A or B | ¶ | ¶ | 1 | 5.2 | | 4.6 | 1 | 4.1 | ns |

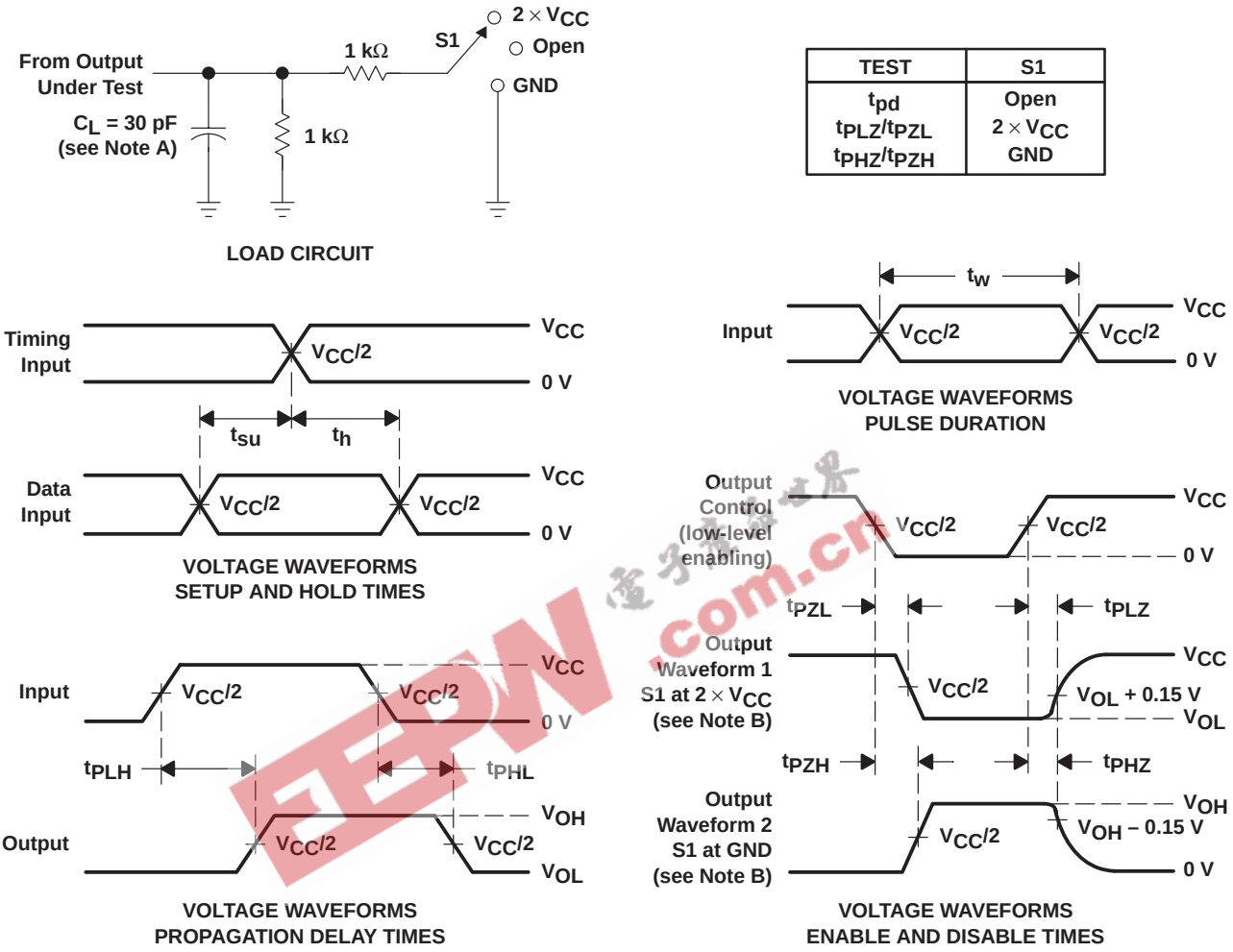
¶ This information was not available at the time of publication.

## operating characteristics, $T_A$ = 25° C

| PARAMETER | | | TEST CONDITIONS | $V_{CC}$ = 1.8 V | $V_{CC}$ = 2.5 V | $V_{CC}$ = 3.3 V | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | TYP | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance | Outputs enabled | $C_L$ = 50 pF, f = 10 MHz | ¶ | 22 | 29 | pF |
| | | Outputs disabled | | ¶ | 4 | 5 | |

¶ This information was not available at the time of publication.

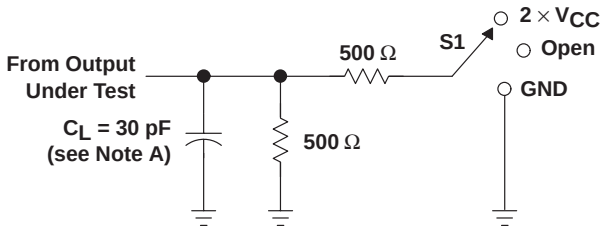
## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 1.8 V ± 0.15 V




NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

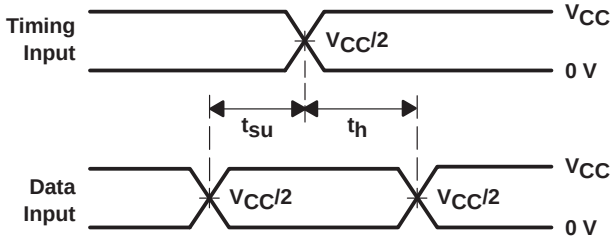
**Figure 1. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 2.5 V ± 0.2 V

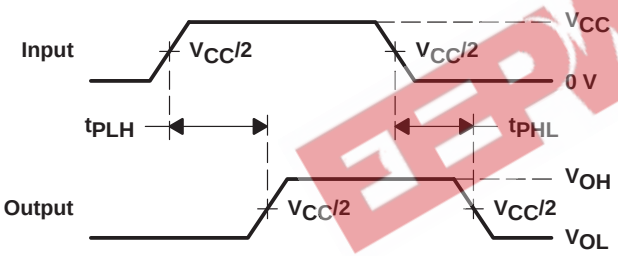



| TEST | S1 |
|---|---|
| $t_{pd}$<br>$t_{PLZ}/t_{PZL}$<br>$t_{PHZ}/t_{PZH}$ | Open<br>2 × $V_{CC}$<br>GND |

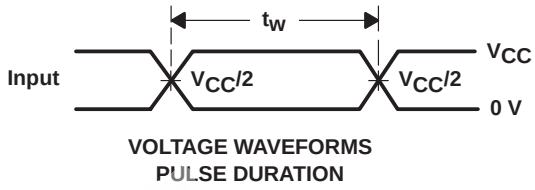
LOAD CIRCUIT



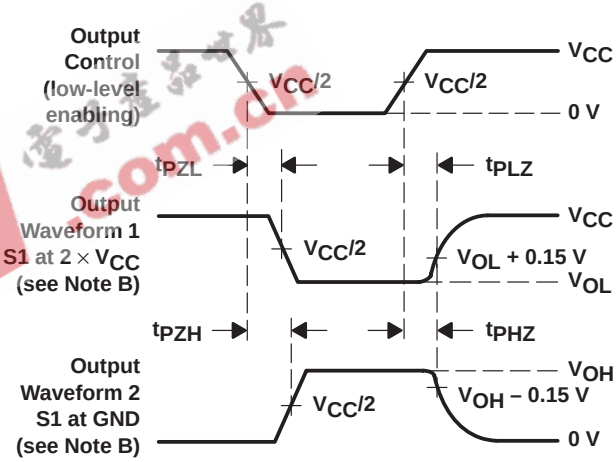

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
PULSE DURATION

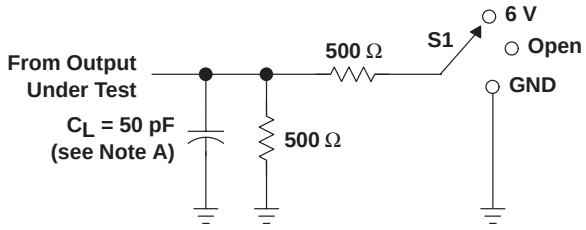



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

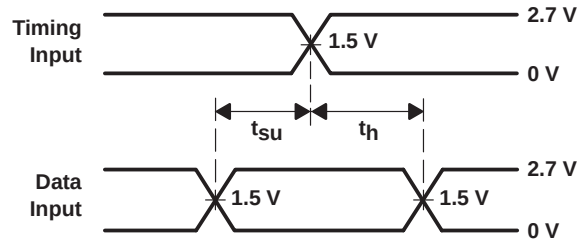
**Figure 2. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 2.7 V AND 3.3 V ± 0.3 V

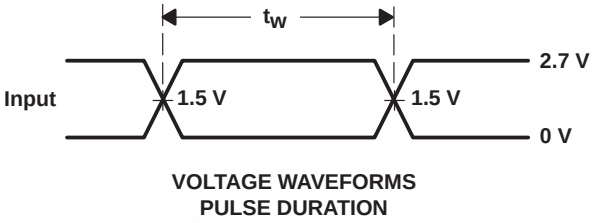



LOAD CIRCUIT

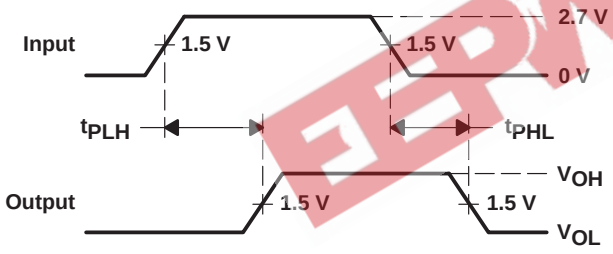
| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V |
| $t_{PHZ}/t_{PZH}$ | GND |



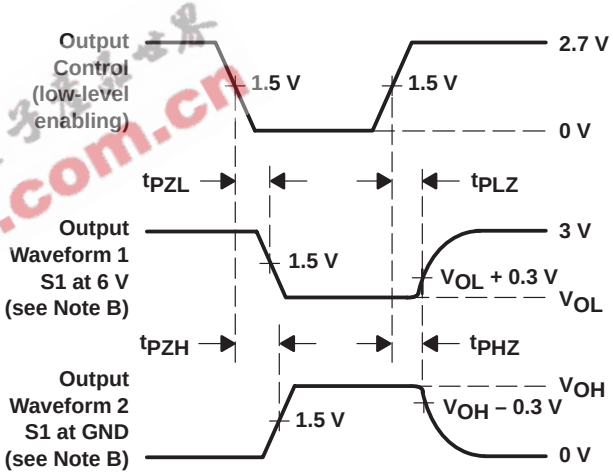

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

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G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 3. Load Circuit and Voltage Waveforms**

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