

## 74F564 Octal D-Type Flip-Flop with 3-STATE Outputs

### General Description

The 74F564 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ( $\overline{OE}$ ). The information presented to the D inputs is sorted in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

This device is functionally identical to the 74F574, but has inverted outputs.

### Features

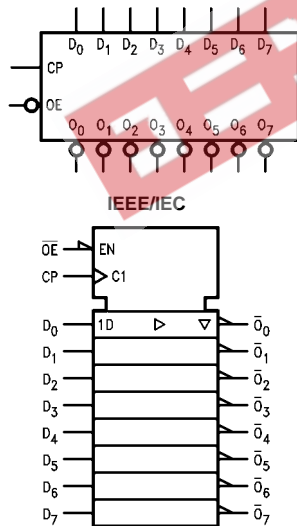
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 74F574
- 3-STATE outputs for bus-oriented applications

### Ordering Code:

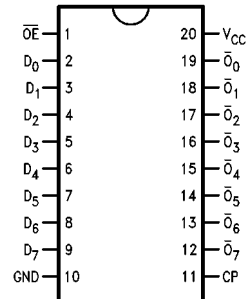
Order Number	Package Number	Package Description
74F564SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F564PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbols



### Connection Diagram



## Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$D_0$ – $D_7$	Data Inputs	1.0/1.0	20 $\mu$ A/–0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/–0.6 mA
$\overline{OE}$	3-STATE Output Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/–0.6 mA
$\overline{O}_0$ – $\overline{O}_7$	3-STATE Outputs	150/40 (33.3)	–3 mA/24 mA (20 mA)

## Functional Description

The 74F564 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

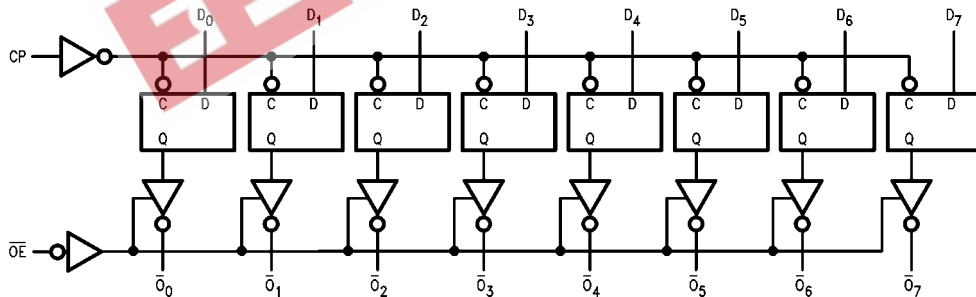
## Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	↗	L	H	Z	Load
H	↗	H	L	Z	Load
L	↗	L	H	H	Data Available
L	↗	H	L	L	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

Z = High Impedance  
↗ = LOW-to-HIGH Transition  
NC = No Change

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

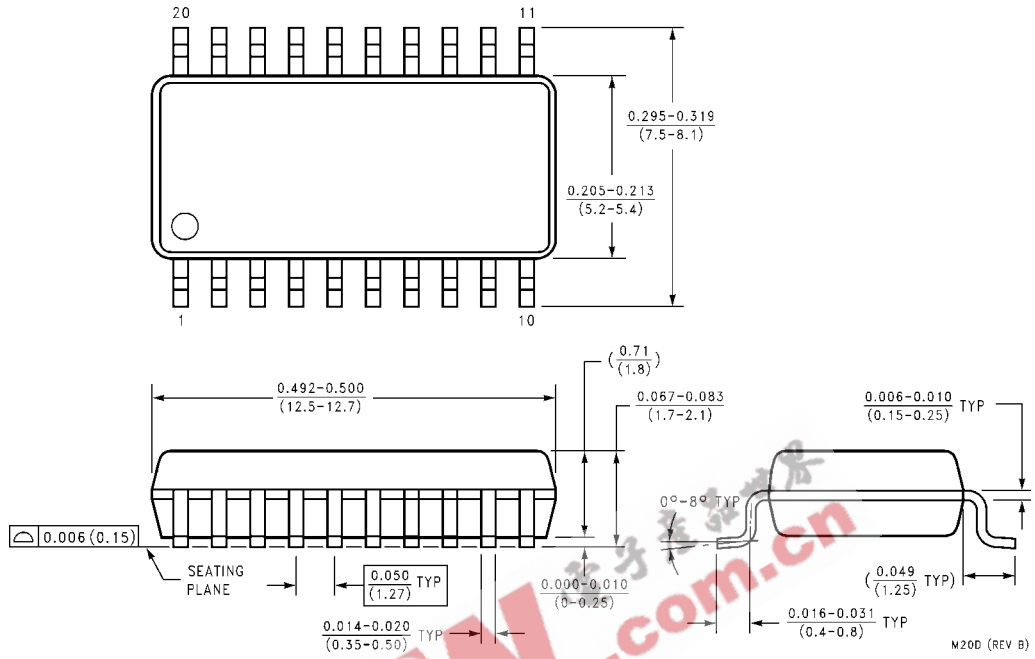
**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA
		10% V <sub>CC</sub>	2.4	I <sub>OH</sub> = -3 mA			
		5% V <sub>CC</sub>	2.7	I <sub>OH</sub> = -1 mA			
		5% V <sub>CC</sub>	2.7	I <sub>OH</sub> = -3 mA			
V <sub>OL</sub>	Output LOW Voltage			0.5	V	Min	I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			-50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	-60		-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCZ</sub>	Power Supply Current		55	86	mA	Max	V <sub>O</sub> = HIGH Z

AC Electrical Characteristics							
Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		Units
		Min	Typ	Max	Min	Max	
t <sub>MAX</sub>	Maximum Clock Frequency	100			70		MHz
t <sub>PLH</sub>	Propagation Delay	2.5	5.2	8.5	2.5	8.5	ns
t <sub>PHL</sub>	CP to $\bar{O}_n$	2.5	5.9	8.5	2.5	8.5	
t <sub>PZH</sub>	Output Enable Time	3.0	5.6	9.0	2.5	10.0	ns
t <sub>PZL</sub>		3.0	6.2	9.0	2.5	10.0	
t <sub>PHZ</sub>	Output Disable Time	1.5	3.4	5.5	1.5	6.5	
t <sub>PLZ</sub>		1.5	2.7	5.5	1.5	6.5	
AC Operating Requirements							
Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V		T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V		Units	
		Min	Max	Min	Max		
t <sub>S(H)</sub>	Setup Time, HIGH or LOW	2.0		2.0		ns	
t <sub>S(L)</sub>	D <sub>n</sub> to CP	2.5		2.5			
t <sub>H(H)</sub>	Hold Time, HIGH or LOW	2.0		2.0			
t <sub>H(L)</sub>	D <sub>n</sub> to CP	2.0		2.0			
t <sub>W(H)</sub>	CP Pulse Width	5.0		5.0		ns	
t <sub>W(L)</sub>	HIGH or LOW	5.0		5.0			

**Physical Dimensions** inches (millimeters) unless otherwise noted



**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M20D**

M20D (REV B)

