DATA SHEET

74F646, 74F646A
Octal transceiver/register, non-inverting (3-State)

74F648, 74F648A
Octal transceiver/register, inverting (3-State)

Product specification

1990 Sep 25

IC15 Data Handbook

Philips Semiconductors

PHILIPS

FEATURES

- Combines 74F245 and two 74F374 type functions in one chip
- High impedance base inputs for reduced loading (70µA in high and low states)
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Choice of non-inverting and inverting data paths
- Controlled ramp outputs for 74F646A/74F648A
- 3-state outputs
- 300 mil wide 24-pin slim dip package

DESCRIPTION

The 74F646/74F646A and 74F648/74F648A transceivers/registers consist of bus transceiver circuits with 3–state outputs, D–type flip–flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes high. Output enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

The select (SAB, SBA) pins determine whether data is stored or transferred through the device in real–time. The DIR determines which bus will receive data when the $\overline{OE}$ is active low. In the isolation mode ($\overline{OE}$ = high), data from bus A may be stored in the B register and/or data from bus B may be stored in the A register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B may be driven at a time.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F646/74F648	115MHz	140mA
74F646A/74F648A	185MHz	105mA

ORDERING INFORMATION

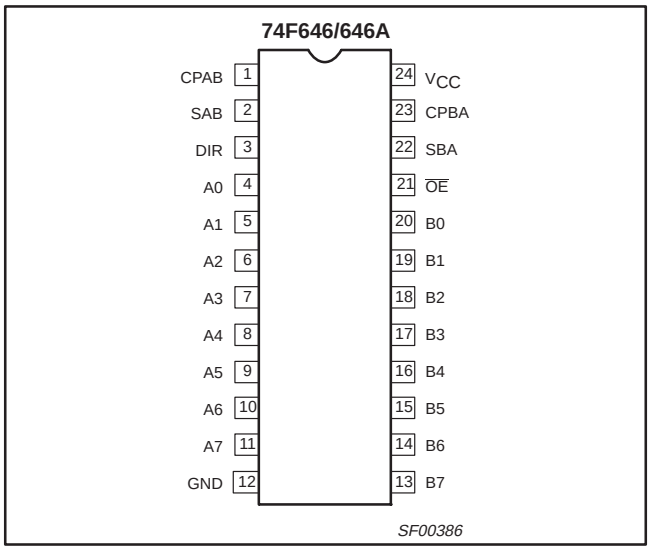
DESCRIPTION	ORDER CODE COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
24–pin plastic slim DIP (300mil)	N74F646N, N74F646AN, N74F648N, N74F648AN	SOT222-1
24–pin plastic SOL	N74F646D, N74F646AD, N74F648D, N74F648AD	SOT137-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

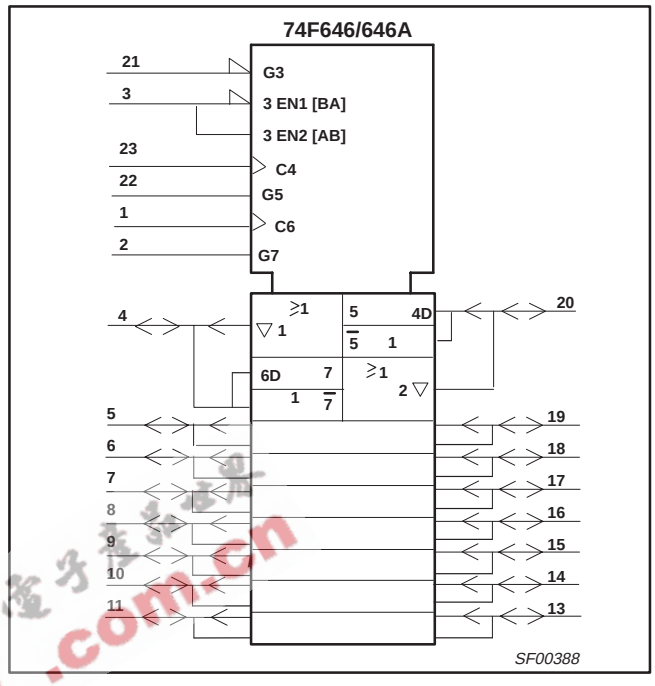
PINS	DESCRIPTION	74F (U.L.) HIGH/ LOW	LOAD VALUE HIGH/ LOW
A0 – A7, B0 – B7	A and B inputs	3.5/0.116	70µA/70µA
CPAB	A–to–B clock input	1.0/0.033	20µA/20µA
CPBA	B–to–A clock input	1.0/0.033	20µA/20µA
SAB	A–to–B select input	1.0/0.033	20µA/20µA
SBA	B–to–A select input	1.0/0.033	20µA/20µA
DIR	Data flow directional control enable input	1.0/0.033	20µA/20µA
$\overline{OE}$	Output enable input	1.0/0.033	20µA/20µA
A0 – A7, B0 – B7	A, B outputs for N74F646A/N74F648A	750/80	15mA/48mA
A0 – A7, B0 – B7	A, B outputs for N74F646/N74F648	750/106.7	15mA/64mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

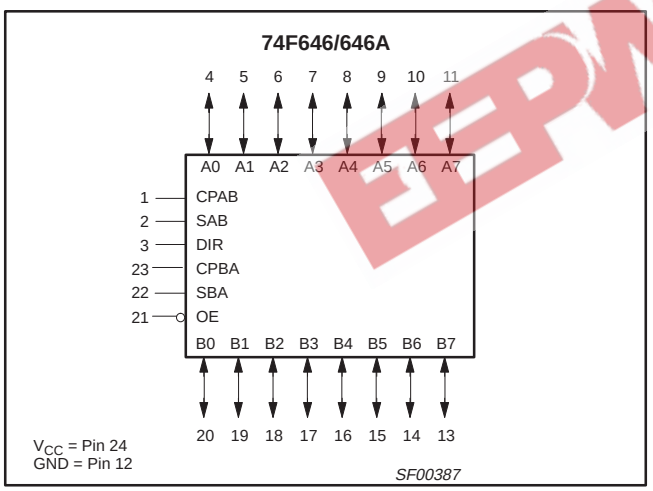
PIN CONFIGURATION



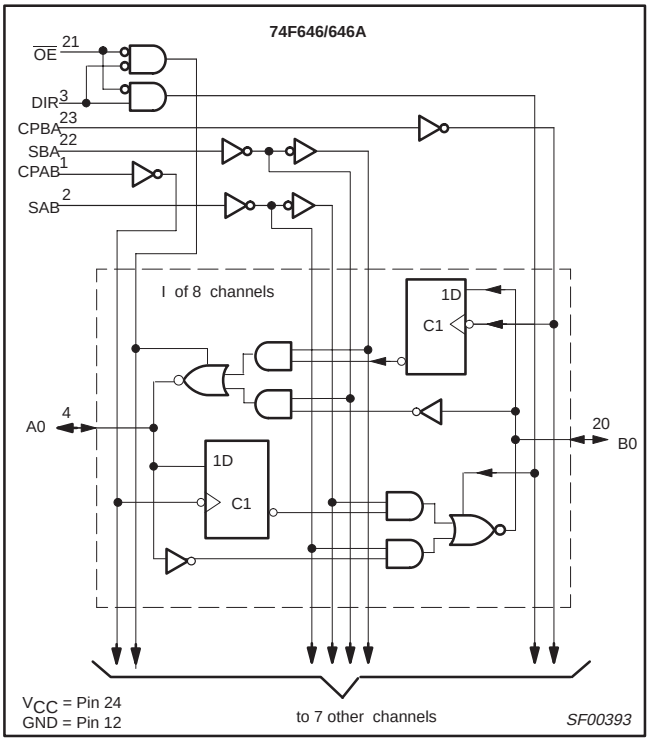
IEC/IEEE SYMBOL



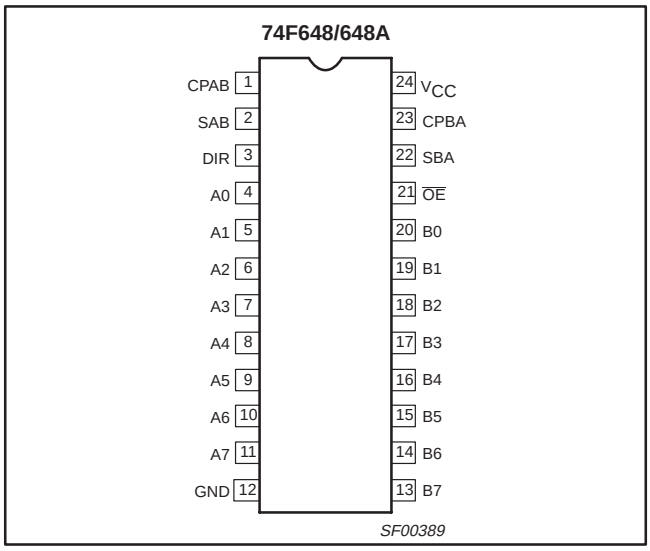
LOGIC SYMBOL



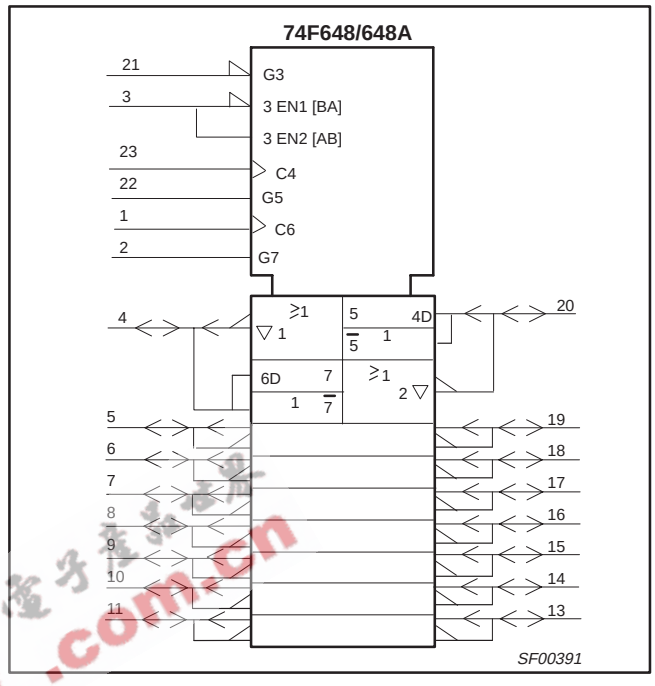
LOGIC DIAGRAM



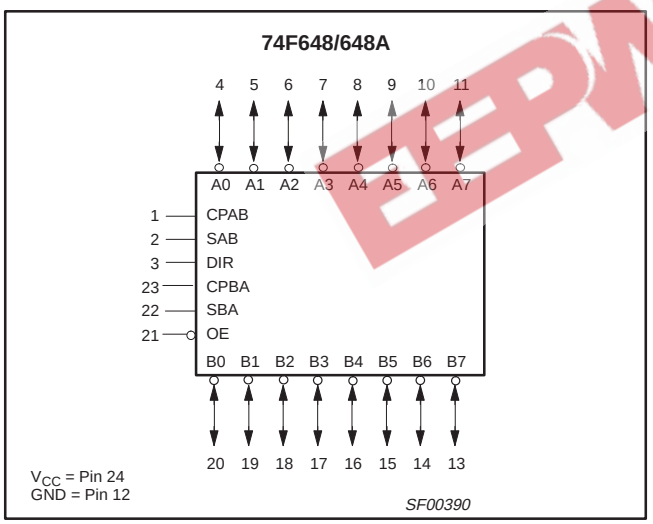
PIN CONFIGURATION



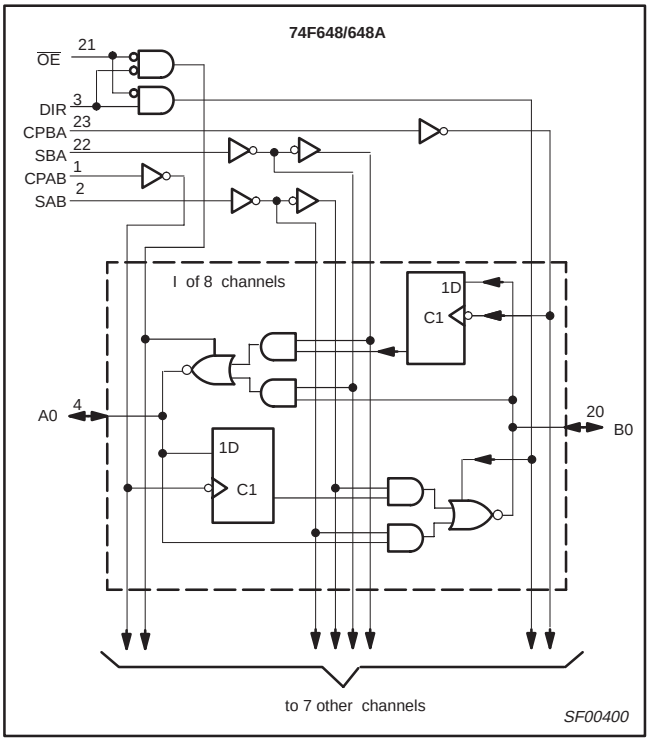
IEC/IEEE SYMBOL



LOGIC SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE	
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	An	Bn	74F646/74F646A	74F648/74F648A
X	X	↑	X	X	X	Input	Unspecified*	Store A, B unspecified*	Store A, B unspecified*
X	X	X	↑	X	X	Unspecified*	Input	Store B, A unspecified*	Store B, A unspecified*
H	X	↑	↑	X	X	Input	Input	Store A and B data	Store A and B data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real time B data to A bus	Real time $\overline{B}$ data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus	Stored $\overline{B}$ data to A bus
L	H	X	X	L	X	Input	Output	Real time A data to B bus	Real time $\overline{A}$ data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus	Stored $\overline{A}$ data to B bus

NOTES:
1. H = High–voltage level
2. L = Low–voltage level
3. X = Don't care
4. ↑ = Low–to–high clock transition
5. * = The data output function may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low–to–high transition of the clock.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

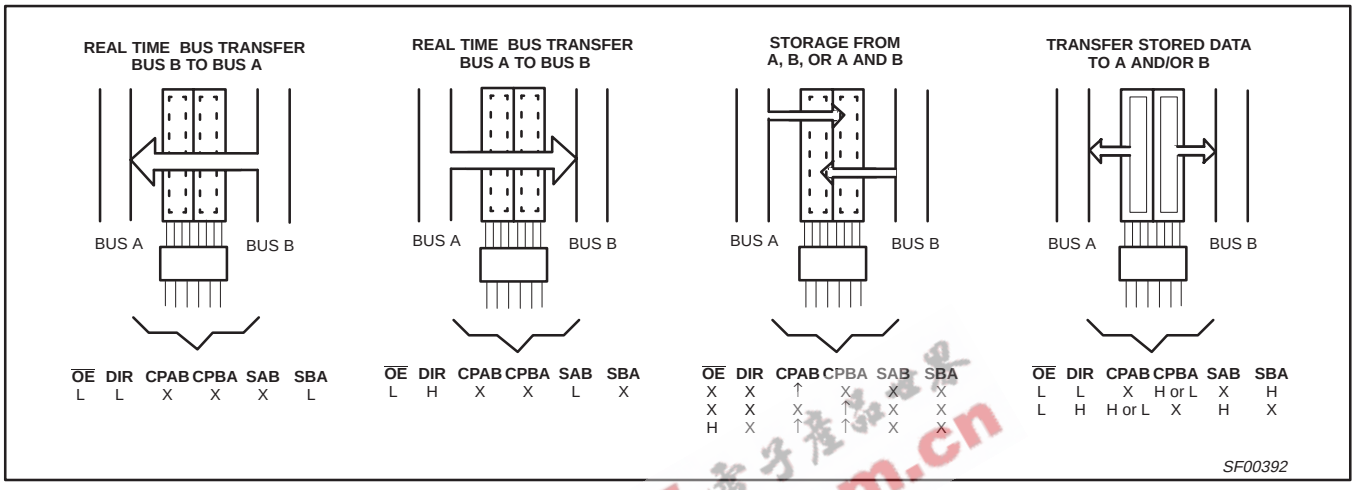
SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	74F646A, 74F648A	72	mA
		74F646, 74F648	128	mA
T_{amb}	Operating free air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current				–15	mA
I_{OL}	Low–level output current	74F646A, 74F648A			48	mA
		74F646, 74F648			64	mA
T_{amb}	Operating free air temperature range		0		+70	°C

The following examples demonstrate the four fundamental bus–management functions that can be performed with the 74F646/646A and 74F648/648A. The select pins determine whether data is stored or transferred through the device in real time. The output enable pins determine the direction of the data flow.

BUS MANAGEMENT FUNCTIONS



DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = –15mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	All	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		0.38	0.55	V
		74F646/74F648 only		I_{OL} = 64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A0–A7, B0–B7	V_{CC} = MAX, V_I = 5.5V					1	mA
I_{IH}	High–level input current	$\overline{OE}$, DIR, CPAB, CPBA, SAB, SBA	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{OZH} + I_{IH}	Off–state output current, high–level voltage applied	A0 – A7, B0 –B7	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{OZL} + I_{IL}	Off–state output current, low–level voltage applied		V_{CC} = MAX, V_O = 0.5V					–70	µA
I_{OS}	Short–circuit output current[3]	74F646, 74F648	V_{CC} = MAX			-100		-225	mA
I_O	Output current[4]	74F646A, 74F648A	V_{CC} = MAX, V_0 = 2.25V			-60		-150	mA
I_{CC}	Supply current (total)	74F646, 74F648	I_{CCH}	V_{CC} = MAX			125	165	mA
			I_{CCL}				160	210	mA
			I_{CCZ}				135	160	mA
		74F646A, 74F648A	I_{CCH}	V_{CC} = MAX			100	145	mA
			I_{CCL}				110	155	mA
			I_{CCZ}				105	155	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type. Unless otherwise specified, V_X = V_{CC} for all test conditions.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_O is tested under conditions that produce current approximately one half of the true short–circuit output current (I_{OS}).

AC ELECTRICAL CHARACTERISTICS FOR 74F646

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	100	115		90		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to An or Bn	Waveform 1	5.5 5.5	7.5 8.0	10.0 10.0	5.0 5.0	11.5 11.0	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	Waveform 2	4.0 4.0	6.0 6.5	9.0 8.0	4.0 4.0	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to An or Bn	Waveform 2, 3	5.0 5.0	7.0 6.5	8.5 8.5	4.5 4.5	10.5 9.5	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	5.0 6.5	7.0 8.5	10.0 11.0	4.5 6.0	11.0 12.5	ns
t_{PZH} t_{PZL}	Output enable time DIR to An or Bn	Waveform 5 Waveform 6	4.5 6.0	6.5 8.5	9.0 11.0	4.0 5.5	10.0 12.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	6.5 6.5	9.0 9.0	11.5 11.5	6.0 6.0	12.5 13.5	ns
t_{PHZ} t_{PLZ}	Output disable time DIR to An or Bn	Waveform 5 Waveform 6	5.5 5.5	8.5 8.5	11.0 11.0	4.5 5.0	13.0 12.5	ns

AC SETUP REQUIREMENTS FOR 74F646

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low An or Bn to CPAB or CPBA	Waveform 4	4.5 4.5			5.0 5.0		ns
t_h (H) t_h (L)	Hold time, high or low An or Bn to CPAB or CPBA	Waveform 4	0 0			0 0		ns
t_w (H) t_w (L)	Pulse width, high or low CPAB or CPBA	Waveform 1	4.0 6.0			4.0 6.0		ns

AC ELECTRICAL CHARACTERISTICS FOR 74F648

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	100	115		90		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to An or Bn	Waveform 1	5.0 5.0	7.0 7.5	9.5 9.5	4.5 4.5	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	Waveform 3	3.0 4.0	6.0 6.0	8.5 8.5	2.5 3.5	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to An or Bn	Waveform 2,3	4.5 4.5	7.0 6.5	8.5 8.5	4.5 4.5	10.5 9.5	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	4.5 6.0	7.0 8.5	10.0 11.0	4.5 5.5	11.0 12.5	ns
t_{PZH} t_{PZL}	Output enable time DIR to An or Bn	Waveform 5 Waveform 6	4.5 6.0	7.0 8.5	10.0 11.0	4.0 5.5	11.0 12.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	6.0 6.0	9.0 8.5	11.5 12.0	6.0 6.0	12.5 13.5	ns
t_{PHZ} t_{PLZ}	Output disable time DIR to An or Bn	Waveform 5 Waveform 6	5.0 5.0	9.0 9.0	12.5 12.5	4.5 5.0	14.0 14.0	ns

AC SETUP REQUIREMENTS FOR 74F648

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low An or Bn to CPAB or CPBA	Waveform 4	4.0 4.0			5.0 5.0		ns
t_h (H) t_h (L)	Hold time, high or low An or Bn to CPAB or CPBA	Waveform 4	0 0			0 0		ns
t_w (H) t_w (L)	Pulse width, high or low CPAB or CPBA	Waveform 1	3.5 6.5			4.0 7.0		ns

AC ELECTRICAL CHARACTERISTICS FOR 74F646A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	165	185		150		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to An or Bn	Waveform 1	5.5 4.5	7.0 7.0	10.5 9.5	4.5 4.0	11.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	Waveform 2	4.0 2.0	6.0 5.0	9.0 8.0	3.5 2.0	10.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to An or Bn	Waveform 2, 3	4.5 3.5	6.5 8.0	9.5 10.0	4.0 3.0	10.0 11.5	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	3.0 3.0	5.5 5.5	9.0 10.0	2.5 2.5	10.0 10.5	ns
t_{PZH} t_{PZL}	Output enable time DIR to An or Bn	Waveform 5 Waveform 6	3.0 3.5	5.0 6.0	8.0 8.5	3.0 3.0	8.5 9.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	1.5 2.5	4.0 5.5	6.5 8.0	1.0 2.0	8.0 9.5	ns
t_{PHZ} t_{PLZ}	Output disable time DIR to An or Bn	Waveform 5 Waveform 6	2.0 3.0	4.5 5.0	7.5 8.0	1.5 2.0	8.5 8.5	ns

AC SETUP REQUIREMENTS FOR 74F646A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low An or Bn to CPAB or CPBA	Waveform 4	3.5 4.0			4.0 4.5		ns
t_h (H) t_h (L)	Hold time, high or low An or Bn to CPAB or CPBA	Waveform 4	0 0			0 0		ns
t_w (H) t_w (L)	Pulse width, high or low CPAB or CPBA	Waveform 1	3.5 3.5			4.5 4.0		ns

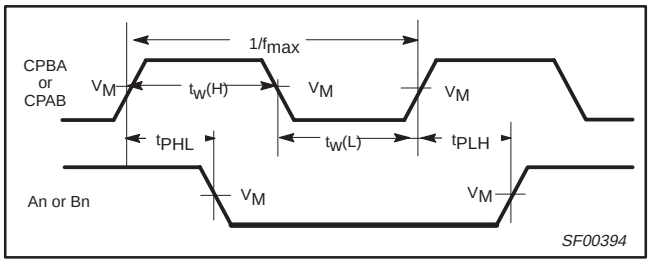
AC ELECTRICAL CHARACTERISTICS FOR 74F648A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	160	185		135		ns
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to An or Bn	Waveform 1	5.0 5.5	7.0 7.5	9.5 10.0	4.5 4.5	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	Waveform 3	2.5 4.0	4.5 6.0	7.5 8.5	2.0 4.0	8.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to An or Bn	Waveform 2, 3	4.0 4.5	7.0 7.0	9.5 9.5	3.5 4.5	11.5 10.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	3.5 4.5	6.5 6.5	10.0 10.0	3.5 4.0	11.0 11.5	ns
t_{PZH} t_{PZL}	Output enable time DIR to An or Bn	Waveform 5 Waveform 6	3.5 4.0	5.5 6.5	8.5 9.5	3.0 4.0	9.0 10.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	2.5 4.0	4.0 6.5	6.5 9.0	2.0 3.5	8.0 10.0	ns
t_{PHZ} t_{PLZ}	Output disable time DIR to An or Bn	Waveform 5 Waveform 6	2.5 2.5	5.0 5.0	8.5 8.0	2.0 3.5	9.0 9.0	ns

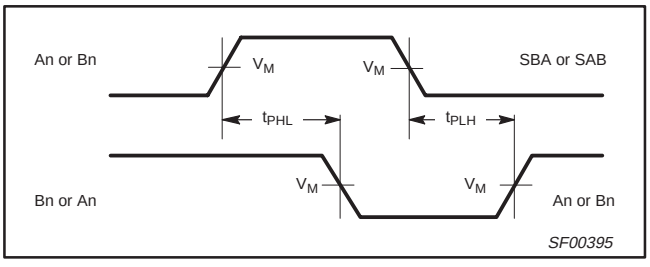
AC SETUP REQUIREMENTS FOR 74F648A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low An or Bn to CPAB or CPBA	Waveform 4	4.0 4.0			4.5 4.5		ns
t_h (H) t_h (L)	Hold time, high or low An or Bn to CPAB or CPBA	Waveform 4	0 0			0 0		ns
t_w (H) t_w (L)	Pulse width, high or low CPAB or CPBA	Waveform 1	3.5 3.5			4.0 3.5		ns

AC WAVEFORMS

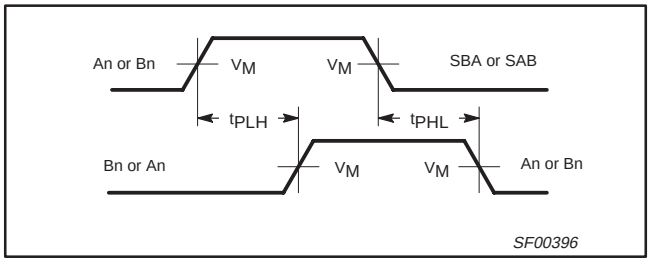


Waveform 1. Propagation delay for clock input to output clock pulse width, and maximum clock frequency

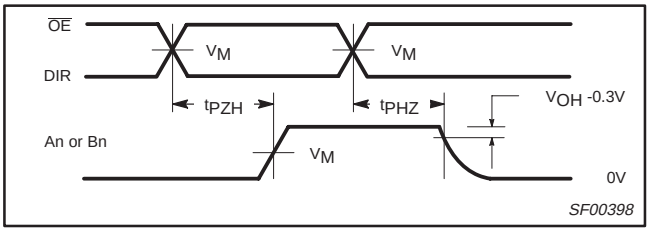


Waveform 2. Propagation delay for An to Bn or Bn to An and SAB or SBA to An or Bn

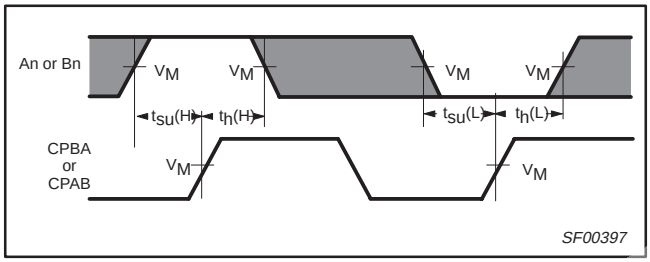
AC WAVEFORMS (Continued)



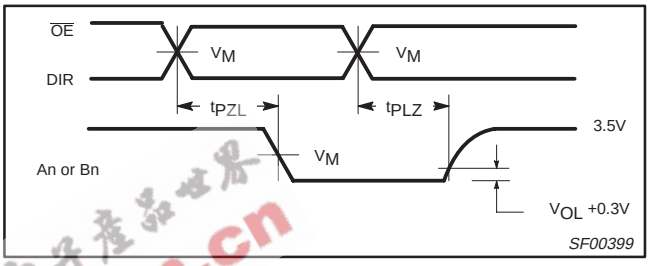
Waveform 3. Propagation delay for An to Bn or Bn to An and SAB or SBA to An or Bn



Waveform 5. 3-state output enable time to high level and output disable time from high level



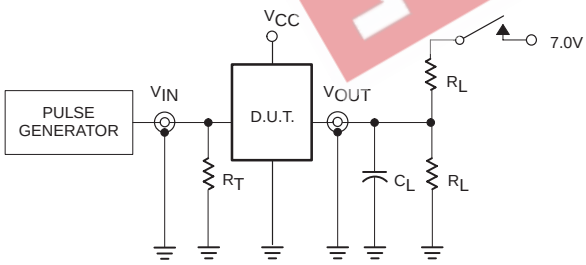
Waveform 4. Data setup time and hold times



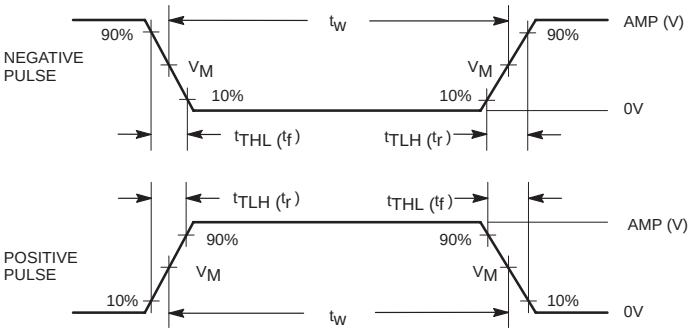
Waveform 6. 3-state output enable time to low level and output disable time from low level

NOTES:
1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for Open Collector Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

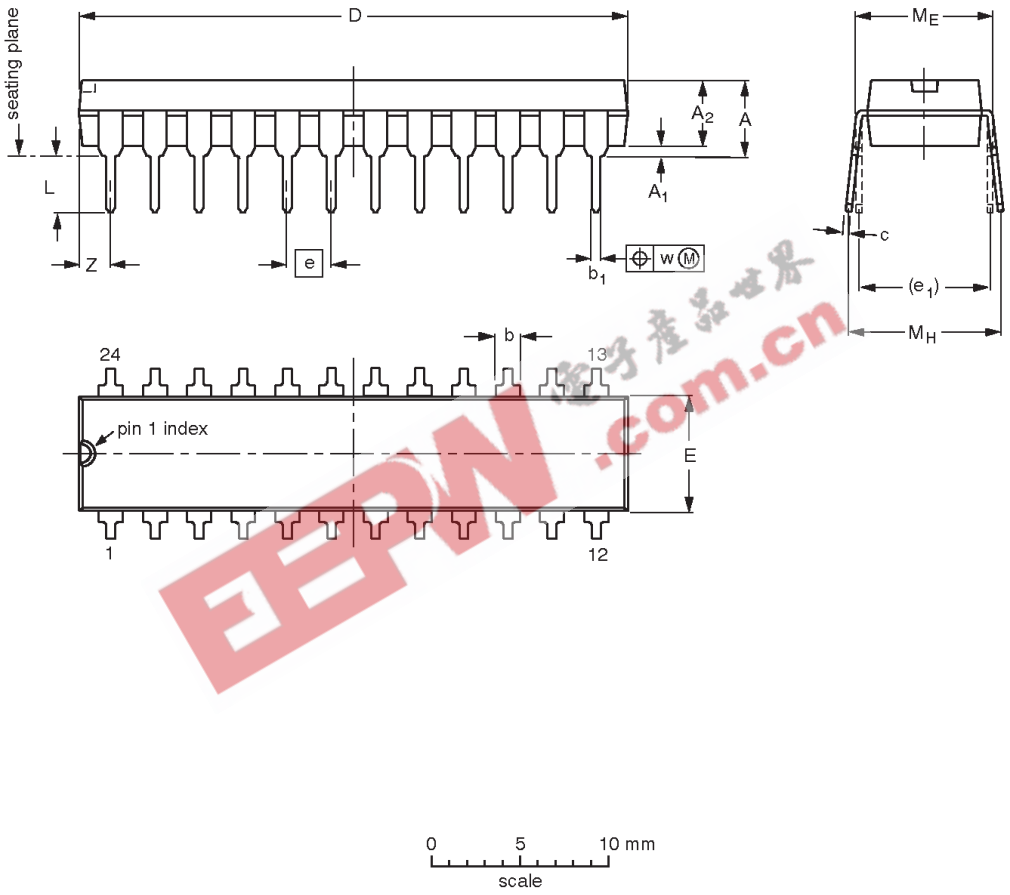
DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

DIP24: plastic dual in-line package; 24 leads (300 mil) SOT222-1



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

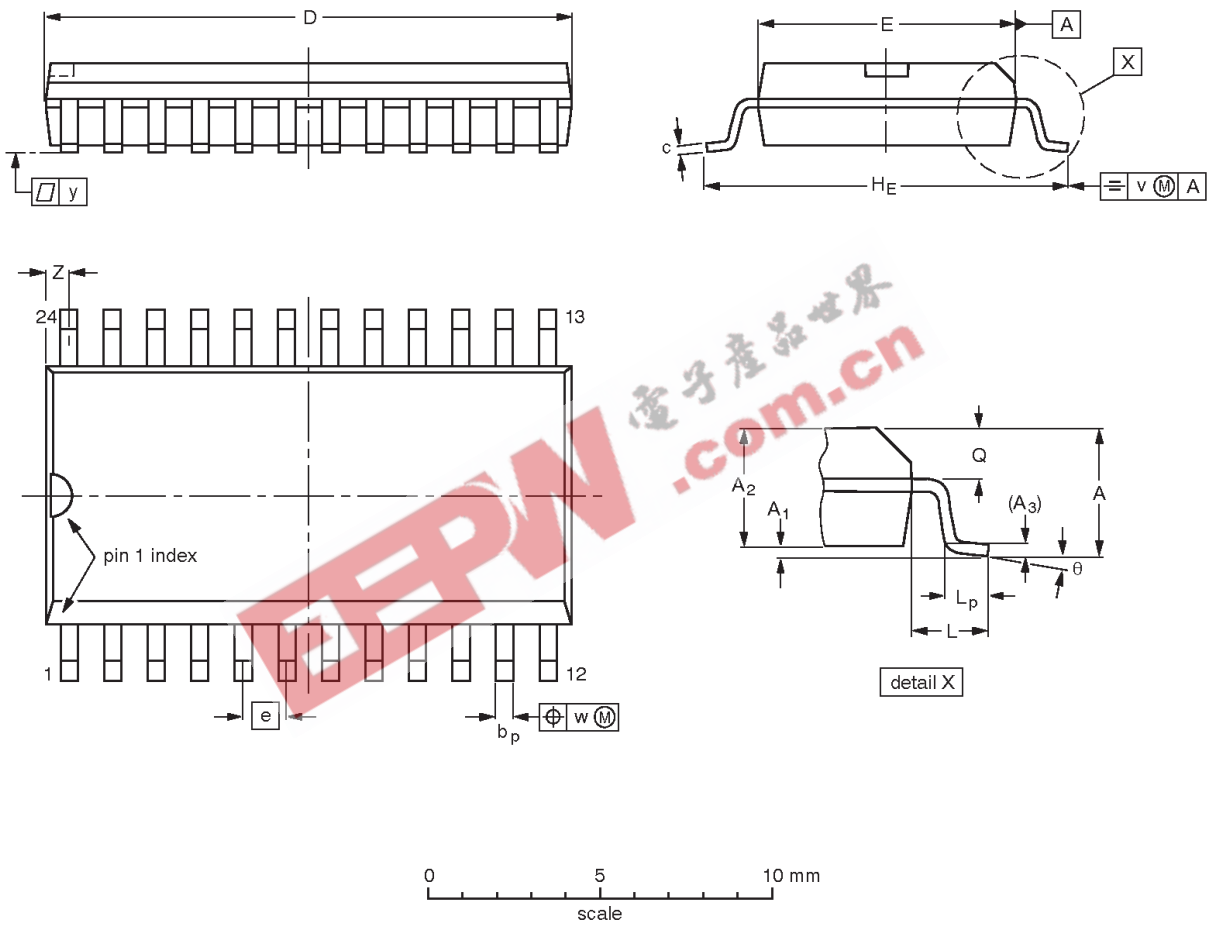
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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