54ACT16827, 74ACT16827 20-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCAS163A - JUNE 1990 - REVISED APRIL 1996

56 10E2

55 1A1

54 1A2

53 GND

52 1A3 51 A14

54ACT16827 ... WD PACKAGE 74ACT16827 ... DL PACKAGE (TOP VIEW)

10E1

1Y1 🛛 2

1Y2 🛛 3

GND 🛛 4

1Y3 5

1Y4 🛛 6

1

Members of the Texas Instruments
<i>Widebus</i> ™ Family

- Inputs Are TTL-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- *EPIC*[™] (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings

description

The 'ACT16827 are noninverting 20-bit buffers composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable ($1\overline{OE1}$ and $1\overline{OE2}$ or $2\overline{OE1}$ and $2\overline{OE2}$) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

The 74ACT16827 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printedcircuit-board area.

V _{CC}	7	50	V _{CC}
1Y5 [8	49	1A5
1Y6 🛛	9	48	1A6
1Y7 🛛	10	47	1A7
GND [11	46	GND
1Y8 _	12	45	1A8
1Y9 🛛	13	44 D	1A9
1Y10	14	43	1A10
2Y1	15	42	2A1
2Y2	16	41	2A2
2Y3	17	40	2A3
🌒 👘 🚺 GND 🛽	18	39	GND
2Y4	19	38	2A4
2Y5 🛛	20	37	2A5
2Y6	21	36	2A6
V _{CC}	22	35	V _{CC}
2Y7 [23	34	2A7
2Y8	24	33	2A8
GND	25	32	GND
2Y9 [26	31	2A9
2Y10	27	30	2A10
20E1	28	29	20E2

The 54ACT16827 is characterized for operation over the full military temperature range of -55° C to 125° C. The 74ACT16827 is characterized for operation from -40° C to 85° C.

	(each 8-bit section)								
I		OUTPUT							
	OE1	OE2	Α	Y					
	L	L	L	L					
	L	L	Н	н					
	Н	Х	Х	Z					
	Х	Н	Х	Z					



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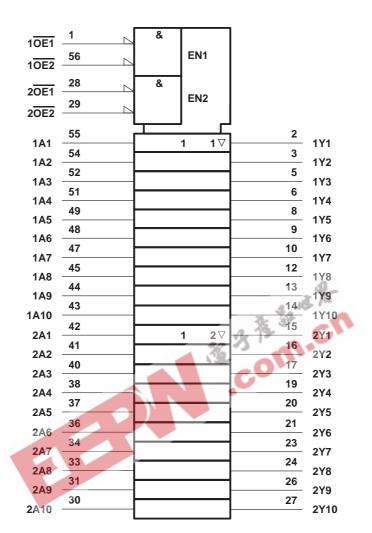
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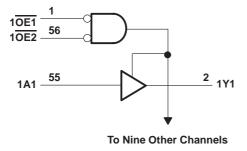
54ACT16827, 74ACT16827 20-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS SCAS163A – JUNE 1990 – REVISED APRIL 1996

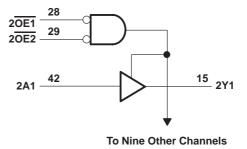
logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)







absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage range, V _{CC} –0.5 V to 7 V
Input voltage range, V _I (see Note 1) –0.5 V to V _{CC} + 0.5 V
Output voltage range, V_O (see Note 1) -0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ±50 mA
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$
Continuous current through V _{CC} or GND ±500 mA
Maximum package power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 2): DL package 1.4 W
Storage temperature range, T _{stg} –65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The maximum package power dissipation is calculated using a junction temperature of 150 °C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

			54ACT16827		54ACT16827			UNIT
			MIN	NOM MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	. 1	4.5	5 5. 5	4.5	5	5.5	V
VIH	High-level input voltage	5	2	2	2			V
VIL	Low-level input voltage	_		0.8			0.8	V
VI	Input voltage	9	0	Vcc	0		VCC	V
Vo	Output voltage		0	Vcc	0		V _{CC}	V
ЮН	High-level output current			5 –24			-24	mA
IOL	Low-level output current		0	24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	0		10	ns/V
ТĄ	Operating free-air temperature		-55	125	-40		85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vaa	T _A = 25°C			54ACT16827		74ACT16827		UNIT
PARAMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
		4.5 V	4.4			4.4		4.4		
	I _{OH} = -50 μA	5.5 V	5.4			5.4		5.4		
VOH	I _{OH} = -24 mA	4.5 V	3.94			3.8		3.8		V
	OH = -24 mA	5.5 V	4.94			4.8		4.8		
	I _{OH} = -75 mA [†]	5.5 V				3.85		3.85		
		4.5 V			0.1		0.1		0.1	
	l _{OL} = 50 μA	5.5 V			0.1		0.1		0.1	
VOL	lot = 24 mA	4.5 V			0.36		0.44		0.44	V
	I _{OL} = 24 mA	5.5 V			0.36	Č,	0.44		0.44	
	$I_{OL} = 75 \text{ mA}^{\dagger}$	5.5 V				201	1.65		1.65	
lj	$V_I = V_{CC}$ or GND	5.5 V			±0.1	540	±1		±1	μA
IOZ	$V_{O} = V_{CC}$ or GND	5.5 V			±0.5		±5		±5	μA
ICC	$V_{I} = V_{CC} \text{ or } GND, \qquad I_{O} = 0$	5.5 V			8	1	80		80	μA
∆I _{CC} ‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V		、花	0.9	25	1		1	mA
Ci	VI = V _{CC} or GND	5 V	38-	4.5	-					pF
Co	$V_{O} = V_{CC} \text{ or } GND$	5 V	Car	16						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡]This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	T _A = 25°C			54ACT16827		74ACT16827		UNIT
FARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
^t PLH		v	3.6	7.4	9.8	3.6	41	3.6	11	ns
^t PHL	A	r	2.8	7.4	9.8	2.8	10.8	2.8	10.8	115
^t PZH	6	v	3	7.9	10.4	3	Q 11.7	3	11.7	ns
^t PZL	ŌĒ	T	4	9.6	12.4	4	14	4	14	115
^t PHZ	05	v	5.8	9.1	11.3	5.8	12.4	5.8	12.4	200
^t PLZ	ŌĒ		5.3	8.5	10.5	5.3	11.5	5.3	11.5	ns

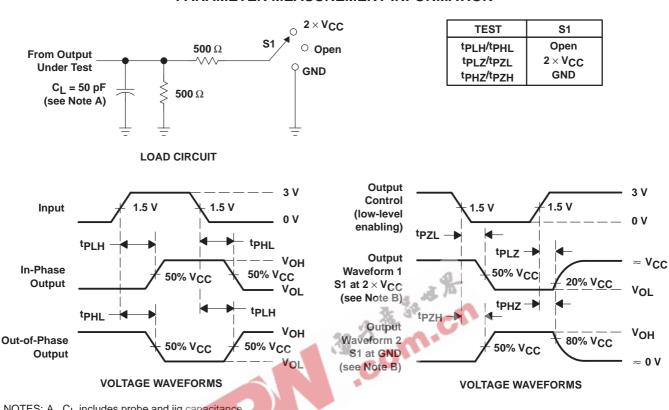
operating characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER				TEST CONDITIONS		
		Devuer disainstian conscitance	Outputs enabled	$C_{1} = 50 \text{ pc}$	f = 1 MHz	41	
C _{pd}	Power dissipation capacitance	Outputs disabled	C _L = 50 pF,	f = 1 MHz	10	pF	

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PARAMETER MEASUREMENT INFORMATION

NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_O = 50 Ω , t_f = 3 ns, t_f = 3 ns.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



3-May-2005

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74ACT16827DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ACT16827DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

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OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. **TBD:** The Pb-Free/Green conversion plan has not been defined.

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⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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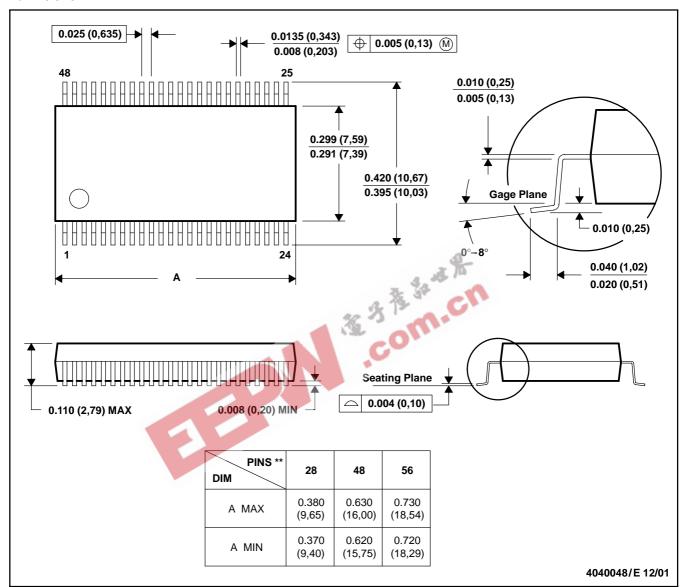
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MECHANICAL DATA

MSSO001C - JANUARY 1995 - REVISED DECEMBER 2001

PLASTIC SMALL-OUTLINE PACKAGE

DL (R-PDSO-G**) 48 PINS SHOWN



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MO-118

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